ECE 381 – Microcontrollers

Lecture 2
GPIO

SOUTHERN ILLINOIS UNIVERSITY
EDWARDSVILLE

Simple Example - GPIO

- Lab 2 – Part 1
  - Detect low-to-high on Port 3[4] or 3[5]
  - Toggle LED1 or LED2 on Digi-Designer
  - Don’t forget about debouncing your switch!

Digital I/O Ports

- Drive Mode Register (Data Direction Register)
  - What gets written to register determines port data direction
  - Some uCs are binary (ie. 0 is input, 1 is output, so 0xF0 would make upper 4 outputs lower 4 inputs)
  - The PSoC5 has 8 Drive Modes (PRTxDM0, PRTxDM1, PRTxDM2 registers)
- Data Register
  - Read from data register tells current value (both input & output pins)
  - Write to data register changes output pins
  - NOTE: On PSoC5, if pin(s) are HW driven, writing to DR has no effect
- Masking
  - If interested in only one specific bit, need a bit mask
  - Example, Output a 1 on bit 6 of Port1:
    - Bit6Mask = 0x40;
    - PRT1DR |= Bit6Mask;
  - Example, Check bit 0 on Port0
    - bit2 = PRT0DR & 0x01;
    - If (bit2 != 0) … else ...

Polling

- The programming equivalent of waiting for UPS to deliver a package
  - Keep looking out the window “Did I see them?”
  - Every time I hear a truck “Is it UPS?”
- Example: Wait for Port0 bit 3 to change value:

```
while (1) {
    if (PRT0DR & 0x04)
    DoRoutine();
}
```

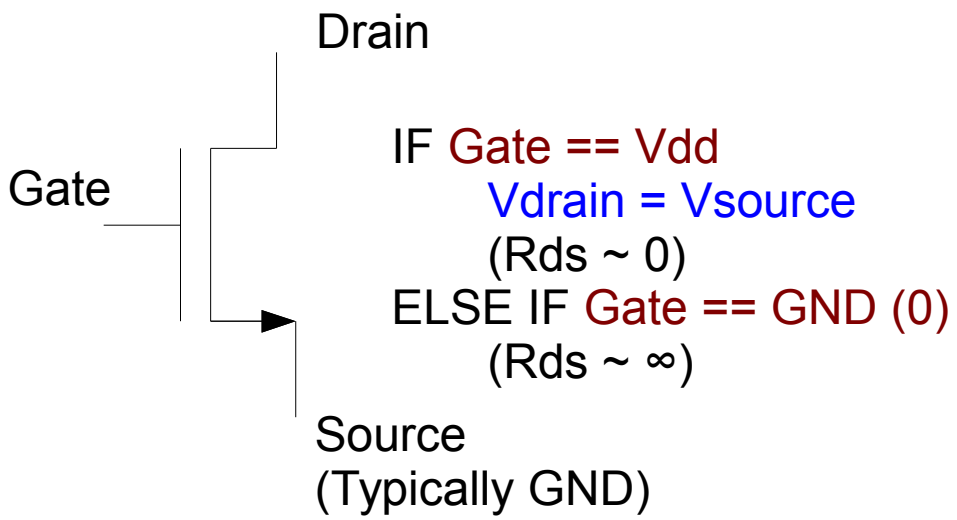
- Just like waiting for a package, don't get anything else done!
- Also, if needing to check multiple ports, may miss the change on another port while running the routine for the current port (Preview for next lecture: Interrupts are really the proper way to do this!)

How To Interact With The Digital World

- Nothing is truly digital, everything is analog!
- We only interpret analog signals as digital due to logic thresholds (If $V > V_{IH} = 1$, $V < V_{IL} = 0$)
- For CMOS Parts (including PSoC) this typcially involves FETs (TTL uses BJTs)

FETs as Switches (Digital Anyway)

NMOS



PMOS

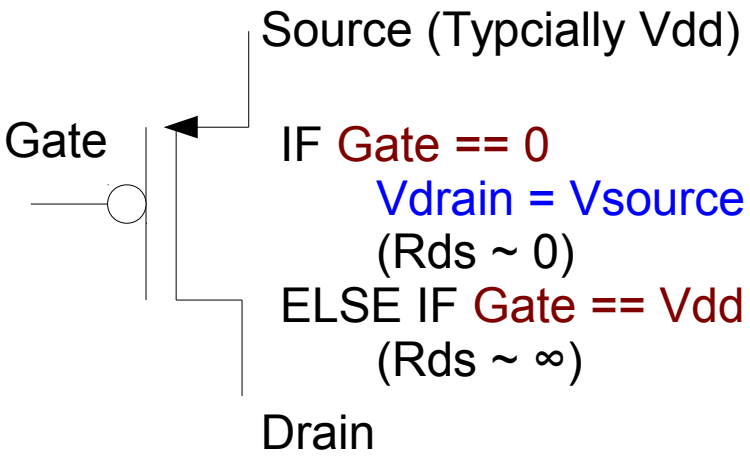
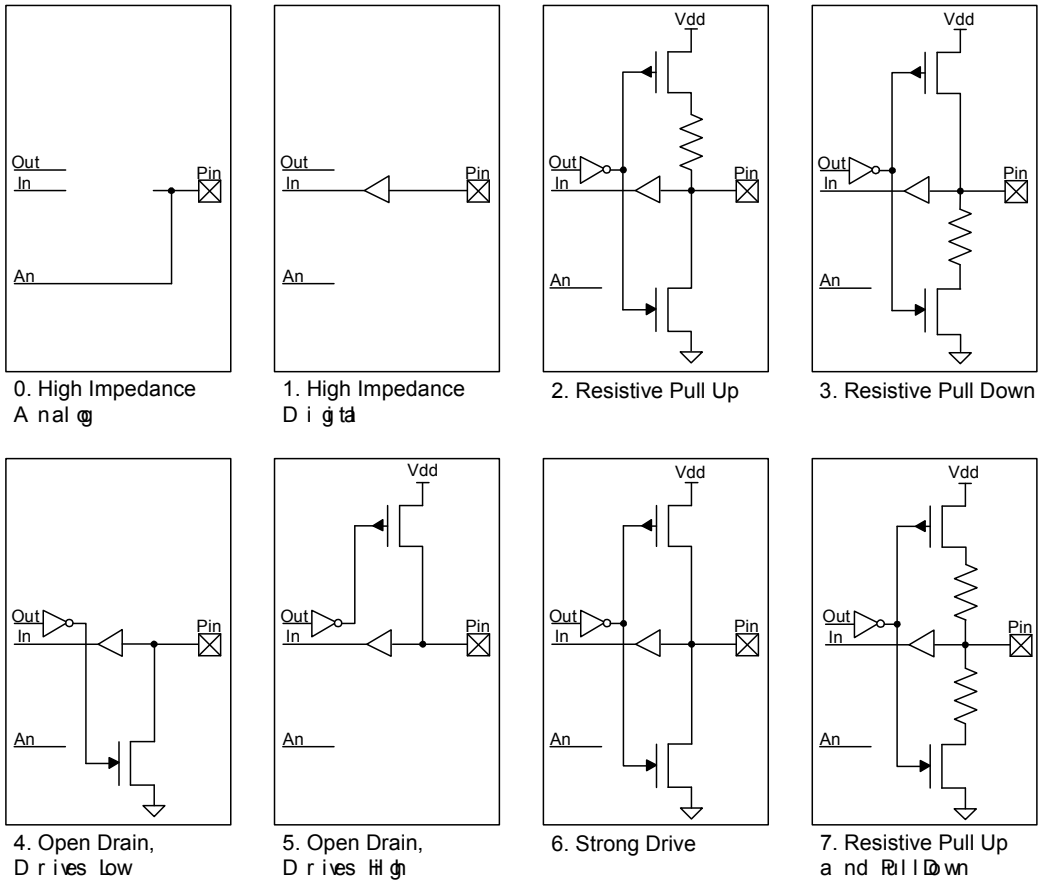


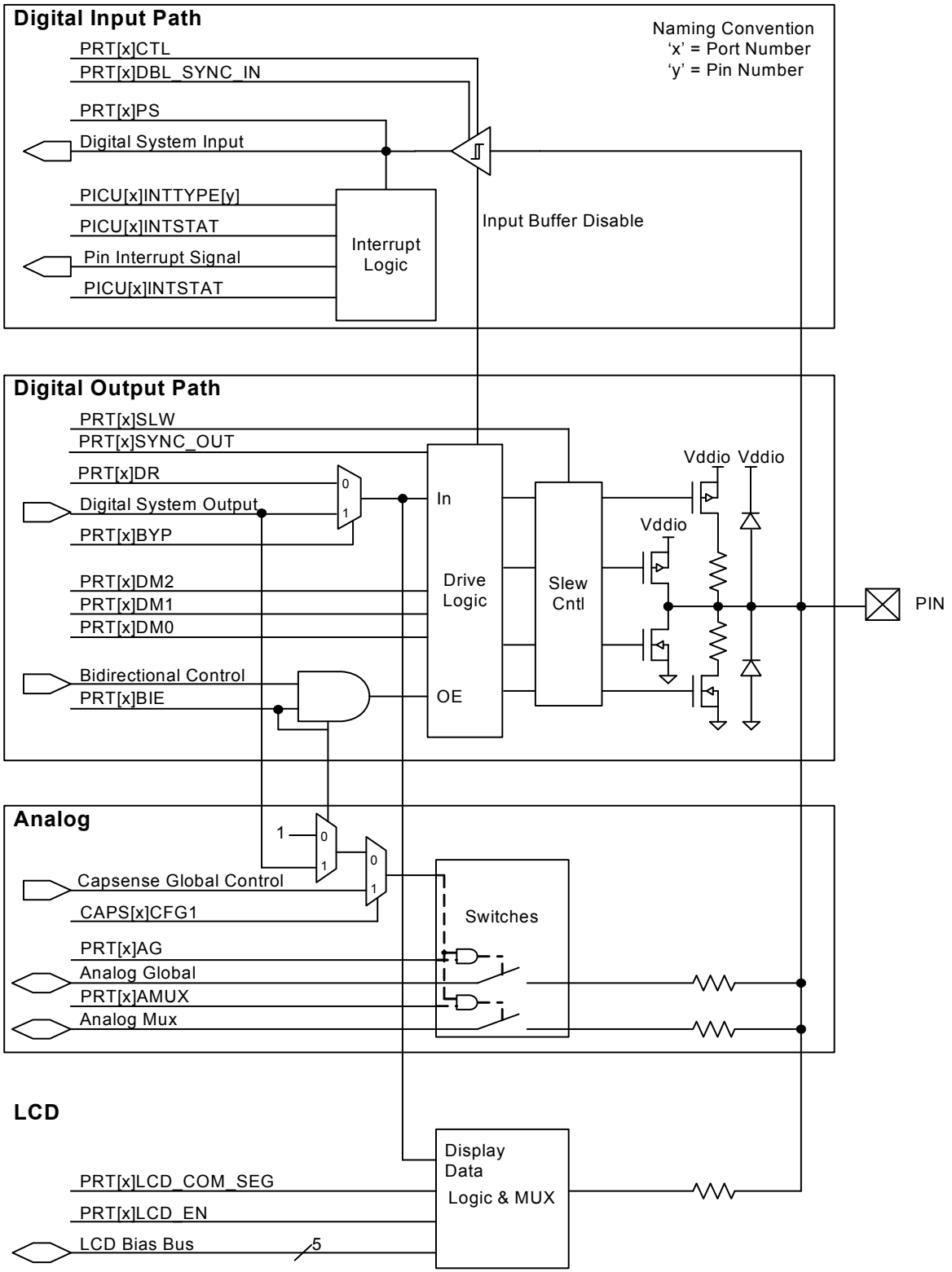
Table 19-1. I/O Drive Modes

Mode Number	Drive Mode	PRTxDM2 DM2	PRTxDM1 DM1	PRTxDM0 DM0	Data = 1	Data = 0
0	High Impedance Analog	0	0	0	High Z	High Z
1	High Impedance Digital	0	0	1	High Z	High Z
2	Resistive Pull Up	0	1	0	Res 1 (5k)	Strong 0
3	Resistive Pull Down	0	1	1	Strong 1	Res 0 (5k)
4	Open Drain, Drives Low	1	0	0	High Z	Strong 0
5	Open Drain, Drives High	1	0	1	Strong 1	High Z
6	Strong Drive	1	1	0	Strong 1	Strong 0
7	Resistive Pull Up and Down	1	1	1	Res 1 (5k)	Res 0 (5k)

Figure 19-4. I/O Drive Mode Diagram



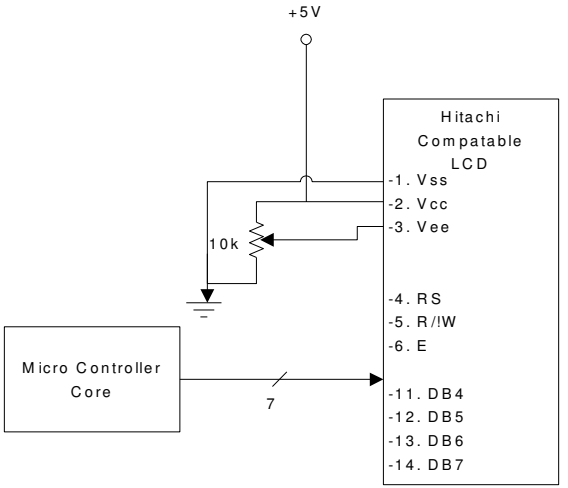
The 'Out' connection is driven from either the Digital System (when the Digital Output terminal is connected) or the Data Register (when HW connection is disabled).
The 'In' connection drives the Pin State register, and the Digital System if the Digital Input terminal is enabled and connected.
The 'An' connection connects to the Analog System.


Digital Input Path
Naming Convention
'x' = Port Number
'y' = Pin Number
PRT[x]CTL
PRT[x]DBL_SYNC_IN
PRT[x]PS
Digital System Input
PICU[x]INTTYPE[y]
PICU[x]INTSTAT
Pin Interrupt Signal
PICU[x]INTSTAT
Interrupt Logic
Input Buffer Disable
Digital Output Path
PRT[x]SLW
PRT[x]SYNC_OUT
PRT[x]DR
Digital System Output
PRT[x]BYP
PRT[x]DM2
PRT[x]DM1
PRT[x]DM0
Bidirectional Control
PRT[x]BIE
In
Drive Logic
OE
Slew Cntl
Vddio
Vddio
Vddio
PIN
Analog
1
Capsense Global Control
CAPS[x]CFG1
PRT[x]AG
Analog Global
PRT[x]AMUX
Analog Mux
Switches
LCD
PRT[x]LCD_COM_SEG
PRT[x]LCD_EN
LCD Bias Bus
5
Display Data
Logic & MUX

Hitachi LCDs

- Industry-standard Hitachi HD44780
  - 7 I/O Pins
- Use PSoC5 Display → Character LCD Module
  - Right-click Open Datasheet
  - Go to Application Programming Interface for C Functions to control it

Logical Port Pin	LCD Module Pin	Description
LCDPort_0	DB4	Data Bit 0
LCDPort_1	DB5	Data Bit 1
LCDPort_2	DB6	Data Bit 2
LCDPort_3	DB7	Data Bit 3
LCDPort_4	E	LCD Enable (strobe to confirm new data available)
LCDPort_5	RS	Register Select (select data or control input data)
LCDPort_6	R/!W	Read/not Write (toggle for polling the ready bit of the LCD)



Assignments:

- **Reading Assignments:**
  - Chapter 19 in the PSoC5 Technical Reference Manual (http://www.siue.edu/~tyork/classes/ece381/labs/files/PSoC%20Technical%20Documents/PSoC5LP_Architecture_TRM.pdf)
- **Lab Assignments:**

  Lab 2 – Polling and the LCD Module