ECE585 Mixed-Signal Design Modeling
Course Syllabus
Fall 2021

Instructor:	Dr. George L. Engel
Time:	T, R (12:30 pm - 1:45 pm)
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Office Hours:	M, W (1:30 pm - 3:00 pm) and T, R (3:00 pm - 4:30 pm)

Course Description

Fundamental circuit techniques and design issues for mixed-signal integrated circuits. Topics include: switched-capacitor techniques and circuits, analog-to-digital and digital-to-analog conversion, along with both system-level and circuit-level modeling using VerilogA.

Course Objectives

- Learn how to design and analyze mixed-signal integrated circuits.
- Learn how to analyze and design switched-capacitor circuits.
- Learn how to model analog and mixed-signal components using Verilog and VerilogA.
- Learn how to design digital-to-analog and analog-to-digital converter circuits.

Prerequisites

ECE326 or equivalent; ECE483 or significance experience with Verilog HDL; ECE484 or equivalent (co-requisite); or permission of instructor.

Required Texts

Tony Carusone, David Johns, and Kenneth Martin "Analog Integrated Circuit Design (Second Edition), John Wiley and Sons, Inc., 2012.

References

- Behzad Razavi, "Principles of Data Conversion System Design," John Wiley and Sons, 1995.
- B. Razavi, Design of Analog Integrated Circuits, McGraw-Hill, 2001.
- Roubik Gregorian and Gabor C. Temes, Analog MOS Integrated Circuit for Signal Processing, John Wiley and Sons, 1986.
- David R. Smith and Paul D. Franzon, Verilog Styles For Synthesis of Digital Systems, Prentice Hall, 2000.
- P. Allen and D. Holberg, CMOS Analog Circuit design: Third Edition, Oxford Press, 2012.

Grading Policy

Midterm Exam	25 %
Final Exam	25 %
Class Project	25 %
Homework	25 %

The following grading scale will be used:

A = 86 - 100

B = 70 - 85

C = 50 - 69

D = 40 - 49

F = $<$ 40

Administrative Issues

Students are expected to be familiar with and follow the Student Academic Code. It is included in the SIUE Policies and Procedures under Section 3C2. Students are expected to use SIUE email addresses in communications related to the course of study and other university activities. It is expected of students to check their email at least on a weekly basis.

Based on University Class Attendance Policy 1I9: It is the responsibility of students to ascertain the policies of instructors with regard to absence from class, and to make arrangements satisfactory to instructors with regard to missed course work. Failure to attend the

first session of a course may result in the student's place in class being assigned to another student.

Students needing accommodations because of medical diagnosis or major life impairment will need to register with Accessible Campus Community and Equitable Student Support (ACCESS) and complete an intake process before accommodations will be given. Students who believe they have a diagnosis but do not have documentation should contact ACCESS for assistance and/or appropriate referral. The ACCESS office is located in the Student Success Center, Room 1270. You can also reach the office by e-mail at myaccess@siue.edu or by calling 618-650-3726. For more information on policies, procedures, or necessary forms, please visit the ACCESS website at www.siue.edu/access.

Homework will be assigned on a regular basis. Students must hand in homework by assigned due date.

Lectures

T Aug 24	Verilog Review with Examples
R Aug 26	Electrical Simulation and Intro to VerilogA
T Aug 31	Conservative System VerilogA Descriptions
R Sep 02	Conservative System VerilogA Descriptions
T Sep 07	VerilogA Signal Flow Description
R Sep 09	VerilogA Signal Flow Descriptions
T Sep 14	VerilogA Event Driven Descriptions
R Sep 16	VerilogA Event Driven Descriptions
T Sep 21	VerilogA Structural Descriptions
R Sep 23	VerilogA File I/O
T Sep 28	Discussion of Class Project
R Sep 30	Chapter 13: Discrete Time Signals
T Oct 05	Chapter 13: Discrete Time Signals
R Oct 07	Chapter 13: Discrete Time Signals
T Oct 12	Midterm Exam (VerilogA and Chapter 13)
R Oct 14	*** READING DAY (NO CLASS) ***
T Oct 19	Chapter 14: Switched-Capacitor Circuits
R Oct 21	Chapter 14: Switched-Capacitor Circuits
T Oct 26	Chapter 14: Switched-Capacitor Circuits
R Oct 28	Chapter 15: Data Converter Fundamentals
T Nov 02	Chapter 15: Data Converter Fundamentals
R Nov 04	Chapter 15: Data Converter Fundamentals
T Nov 09	Chapter 15: Data Converter Fundamentals
R Nov 11	Chapter 16: Nyquist Rate DACs
T Nov 16	Chapter 16: Nyquist Rate DACs
R Nov 18	Chapter 16: Nyquist Rate DACs

T Nov 23	*** Thanksgiving Break ***
R Nov 25	*** Thanksgiving Break ***
T Nov 30	Chapter 17: Nyquist Rate ADCs
R Dec 02	Chapter 17: Nyquist Rate ADCs
T Dec 07	Chapter 17: Nyquist Rate ADCs
R Dec 09	Chapter 17: Nyquist Rate ADCs