ECE 584
Chapter 2 Homework

Dr. George Engel

Due: One week after we finish Chapter 2

You should use the process data given to you in class to answer the following questions.

Problem 1. Sensitivity Analysis

The time constant, $\tau = R \cdot C$, is a very important parameter in the design of many circuits.

(a) Perform a sensitivity analysis to determine the relative error in τ given the relative error in R and the relative error in C.

(b) Suppose the value of C is 5 % low and the value of R is 12 % high, what is the relative error in τ?

(c) Suppose the value of C is 3 % high and the value of R is 7 % low, what is the relative error in τ?

Problem 2. Current Mirror Mismatch

In this problem we will investigate the sensitivity properties on NMOS and PMOS current mirrors. You should ensure that the current mirror devices are strongly inverted and saturated.

Size (find W and L) the devices in a simple NMOS current mirror to provide a nominal drain current of 50 μA with a small-signal output resistance of at least 800 $K\Omega$. The 3σ random variations in the threshold voltages of the two devices should result in less than a 1 % difference in the drain currents of the two devices. The effective voltage should not exceed 0.75 Volts.

Problem 3. Differential Pair Input Device Mismatch

In this problem we will investigate the sensitivity properties of NMOS and PMOS differential pairs. The devices should be moderately inverted with a inversion coefficient value of 3.

Size (find W and L)the NMOS differential pair devices to have a transconductance of 100 $\mu\mho$. The input offset voltage of the differential pair should be less than 2 mV 99.8 % of the time.

Problem 4. Implementing Capacitor Ratios

We desire to match two double-poly capacitors (CPOLY), C_1 and C_2. C_1 has a value of 3 pF and C_2 has a value of 1.293 pF. Sketch a layout for the two capacitors such that their ratio will be preserved in the presence of process variability. Make sure you indicate the size of all structures. What is the size of the unit capacitor which you decided to use? Predict the relative error (given as a percentage) associated with the unit capacitors.

Problem 5. Implementing Resistor Ratios

We desire to match two RPOLYH resistors, R_1 and R_2. R_1 has a value of 6 $K\Omega$ and R_2 has a value of 3 $K\Omega$. Sketch a layout for the two resistors such that their ratio will be preserved in the presence of process variability. Make sure you indicate the size of all structures. What is the size of the unit resistor which you decided to use? Predict the relative error (as a percentage) associated with the unit resistor.