ECE 484
Digital VLSI Design
Fall 2021

Instructor:	Dr. George L. Engel
Time:	M, W (3:00 - 4:15 pm)
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Course Description

Discussion of CMOS circuits, MOS transistor theory, CMOS processing technology, circuit characterization, CMOS circuit and logic design.

Required Texts

CMOS VLSI Design: A Circuits and Systems Perspective
Neil H.E. Weste and David Money Harris
Addison-Wesley
ISBN 10: 0-321-54774-8
ISBN 13: 978-0-321-54774-3

Grading Policy

A student's grade in the class will be computed as follows:

Exam # 1	25 %
Exam # 2	25 %
Exam # 3	25 %
Project	25 %

For both undergraduate and graduate students, the following grading scale will be used:

A = 90 - 100

B = 80 - 89

C = 70 - 79

D = 60 - 69

F = < 60

Administrative Issues

Students are expected to be familiar with and follow the Student Academic Code. It is included in the SIUE Policies and Procedures under Section 3C2. Students are expected to use SIUE email addresses in communications related to the course of study and other university activities. It is expected of students to check their email at least on a weekly basis.

Based on University Class Attendance Policy 1I9: It is the responsibility of students to ascertain the policies of instructors with regard to absence from class, and to make arrangements satisfactory to instructors with regard to missed course work. Failure to attend the first session of a course may result in the student's place in class being assigned to another student.

Students needing accommodations because of medical diagnosis or major life impairment will need to register with Accessible Campus Community and Equitable Student Support (ACCESS) and complete an intake process before accommodations will be given. Students who believe they have a diagnosis but do not have documentation should contact ACCESS for assistance and/or appropriate referral. The ACCESS office is located in the Student Success Center, Room 1270. You can also reach the office by e-mail at myaccess@siue.edu or by calling 618-650-3726. For more information on policies, procedures, or necessary forms, please visit the ACCESS website at www.siue.edu/access.

Homework will be assigned on a regular basis. Students must hand in homework by assigned due date.

Graduate Credit

Students taking ECE484 for graduate credit will be required to complete ONE additional problem on each of the three exams. The problem will be worth 10 points. All students taking the course for undergraduate credit will receive full credit for the problem without having to solve the problem. The additional problem will be made more difficult and will bear less resemblance to problems worked for homework.

Graduate students will also be **required** to complete a more difficult final project. The final project is more difficult because it will require the use of more complex algorithms than

those needed to successfully complete an undergraduate project. While these algorithms are discussed in the course textbook, they are not covered in lecture. Hence, students taking the class for graduate credit will need to do some additional reading to successfully complete their final projects.

ECE484 Lecture Schedule

M Aug 23	CHAPTER 1: INTRODUCTION 1.1.0 A Brief History Moore's Law IC Economics
W Aug 25	1.4 CMOS Logic 1.4.1 Inverter
M Aug 30	1.4.2 NAND gate 1.4.3 NOR gate
W Sep 01	CHAPTER 2: MOS TRANSISTOR THEORY 2.1.0 Introduction 2.2.0 Long-Channel I-V Characteristics
M Sep 06	*** LABOR DAY (NO CLASSES) ***
W Sep 08	2.2.0 Long-Channel I-V Characteristics
M Sep 13	2.2.0 Long-Channel I-V Characteristics
W Sep 15	2.3.0 C-V Characteristics 2.4.1 Mobility Degradation and Velocity Degradation 2.4.2 Channel Length Modulation
M Sep 20	2.4.3 Threshold Voltage Effects 2.4.4 Leakage 2.4.5 Temperature Dependence 2.5.0 DC Transfer Characteristics
W Sep 22	2.5.0 DC Transfer Characteristics
M Sep 27	CHAPTER 3: CMOS PROCESSING TECHNOLOGY Texas Instruments Tour on DVD
W Sep 29	CHAPTER 4: DELAY 4.1.0 Introduction 4.2.0 Transient Response 4.3.0 RC Delay Model
M Oct 04	**EXAM #1 on Chapters 1, 2, and 3**
W Oct 06	4.3.1 Effective Resistance 4.3.2 Gate and Diffusion Capacitance 4.3.4 Transient Response
M Oct 11	4.3.5 Elmore Delay

W Oct 13	4.4.0 Linear Delay Model 4.4.1 Logical Effort
M Oct 18	4.4.2 Parasitic Delay 4.4.3 Delay in a Logic Gate
W Oct 20	4.5.0 Logical Effort of Paths 4.5.1 Delay in Multi-Stage Logic Networks 4.5.2 Choosing the Best Number of Stages
T Oct 25	CHAPTER 5: POWER 5.1.0 Introduction 5.1.3 Sources of Power Dissipation 5.2.0 Dynamic Power
R Oct 27	5.3.0 Static Power
M Nov 01	CHAPTER 6: INTERCONNECT 6.1.1 Wire Geometry 6.2 Interconnect Modeling
W Nov 03	**EXAM #2 on Chapters 4 and 5**
M Nov 08	6.2.1 Resistance
W Nov 10	6.2.2 Capacitance
T Nov 15	CHAPTER 9: Combinational Circuit Design 9.2.1 Static CMOS
R Nov 17	9.2.2 Ratioed Circuits
M Nov 22	**** THANKSGIVING BREAK ****
W Nov 24	**** THANKSGIVING BREAK ****
W Nov 29	9.2.5 Pass-Transistor Circuits
W Dec 01	CHAPTER 10: Sequential Circuit Design 10.1 Introduction 10.2 Sequencing Static Circuits
M Dec 06	10.3 Circuit Design of Latches and Flip Flops
W Dec 08	10.3 Circuit Design of Latches and Flip Flops

ECE484 Laboratory Schedule

M Aug 23	*** NO LABS ***
M Aug 30	Introduction to LINUX Schematic Capture, Symbol Creation, and Simulation
M Sep 06	Schematic Capture, Symbol Creation, and Simulation
M Sep 13	Layout, DRC, and LVS
M Sep 20	Layout, DRC, and LVS
M Sep 27	Layout, DRC, and LVS
M Oct 04	Layout, DRC, and LVS
M Oct 11	Creating a 4-bit Counter Using Standard Cells
M Oct 18	Creating a 4-bit Counter Using Standard Cells
T Oct 25	Work on final project
M Nov 01	Work on final project
M Nov 08	Work on final project
M Nov 15	Work on final project
M Nov 22	**** THANKSGIVING BREAK ****
M Nov 29	Demo final project
M Dec 06	*** NO LABS ***