EXPERIMENT 12

INTRODUCTION TO PSPICE AND AC VOLTAGE DIVIDERS

OBJECTIVE

To gain familiarity with PSPICE, and to review in greater detail the ac voltage dividers studied in Experiment 14.

PROCEDURE

1) Connect the circuit in Fig. 1, choosing values of the resistor and the capacitor so that the reactance of the capacitor, $1/2\pi fC$, is equal to the resistance at a frequency of 4 to 5 kHz. The reactance will of course be different at different frequencies.

Apply approximately a 10 volt p-p sine wave from the function generator at frequencies of 2 kHz, 4 kHz, 6 kHz, 8 kHz, and 10 kHz to the input. Measure the input voltages with the digital meter and with the scope. You will observe that the digital meter does not read "ten volts." *Why?*

Measure and plot the output voltage as a function of the frequency. *What is the output voltage at the frequency where the resistor and the capacitor have the same impedance?* (This is the "break point" frequency.) *What is the output voltage with a dc input? What is the output voltage at 100 kHz?*

2) Connect the circuit in Fig. 2, which is complementary to the circuit in Fig. 1. Using both the digital meter and the scope, measure the output voltage as a function of frequency at the same frequencies as in Part 1. *What is the output with a dc input? What is the output at 100 kHz? What is the relationship between this plot and the plot obtained in part 1?*

3) Repeat Parts 1 and 2, but using a square wave from the function generator. *What does the digital meter read now for a 10 volt p-p input signal? How does it differ from the previous value in Part 1?*

The results with a square wave input are more complicated, and quite different from before. To see what is going on reduce the input frequency to 100 Hz. *Sketch the waveforms for the two different circuits.*

With a square wave input, what are the measured rise times and fall times at the output of the circuit in Fig. 1? How do they compare with the product R times C? How do they compare with the break point frequency obtained in Part 1?

With a square wave input, what are the measured decay times at the output of the circuit in Fig. 2? How do they compare with the product R times C? How do they compare with the break point frequency obtained in Part 2?

PSPICE ASSIGNMENT

Use PSPICE to repeat Parts 1 and 2, generating continuous curves of the output voltage from 1 kHz to 100 kHz. Plot the output voltage in dB, and use a logarithmic frequency scale. *How do your experimental results compare with these theoretical curves?*

QUESTIONS

1) *What are the relative advantages of the scope and the digital voltmeter?*

2) *Which would you use to make an accurate measurement?*

3) *Which would you use if you didn't know what the waveform was?*

Figures

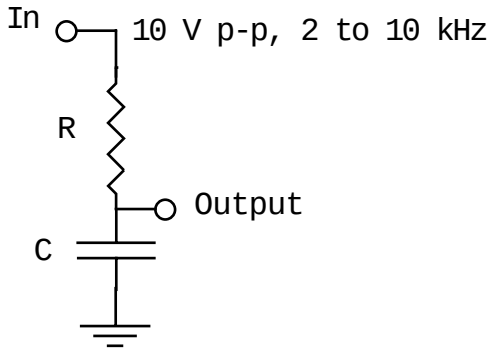


Fig 1

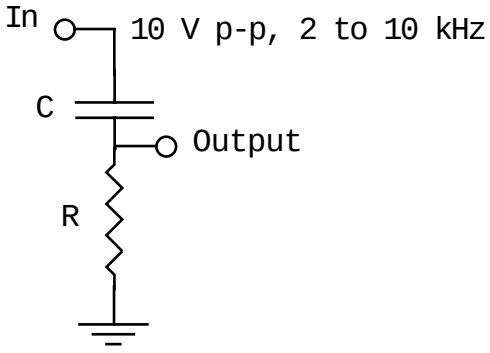


Fig 2

EXPERIMENT 4

RESISTOR CAPACITOR CIRCUITS

OBJECTIVE

To measure the time constants of typical RC circuits, and study the correlation between time constants and frequency response, using the oscilloscope as a measuring device.

THEORY

Consider a resistor and a capacitor in series, as shown in Fig. 1. Suppose points A and C have constant voltages, V_A and V_C, respectively. Then the voltage at point B, V_B, is either the same as the voltage at point A, or it is approaching it exponentially:

$$V_B - V_A = Const.e^{\frac{-t}{RC}} \qquad (4-1)$$

where t is the time in seconds, and R and C are the values of the resistor and capacitor in ohms and farads. The time RC, which is also measured in seconds, is called the "time constant" of the circuit. It is the time taken for the voltage at point B to approach closer to that on point A by a factor of e (2.718...). This analysis is correct so long as point B is not connected to anything that can supply (or drain) current. For example, point B may be connected to a component that does not draw significant current, such as a reverse biased diode, or the input to an op-amp.

If the voltage at point B approaches that at point A exponentially in time, how did it ever get to be different from A? There are two possibilities:

1) Although the voltages on points A and C are constant now, they may have changed in the recent past.

2) Although nothing is connected to point B now, something may have been connected in the recent past.

Both of these possibilities occur frequently in circuit design. "Recent" should be understood to mean within a few time constants, or otherwise the voltage at point B would already have become equal to that on point A.

PROCEDURE

1) Connect the circuit in Fig. 2, using as an input a 0 to 3 volts square wave from the function generator at a frequency of 100 Hz. Set the oscilloscope to trigger externally from the function generator, at a sweep speed of 1 msec/division. Set both channels at 1 volt/division dc, and place both scope probes on the input to the circuit. Use the scope to fine tune the frequency to 100 Hz.

What you should see is one cycle of the square wave, with an amplitude of 3 divisions, in each of the channels. Set the "vertical" controls on the scope so that ground on both channels is in the middle of the screen. Adjust the trigger level control if necessary so that the display is stationary, and starts with the positive going half of the cycle.

Now, take one of the scope probes and place it on the output of the circuit. It should **resemble** the input, which you can still see on the other channel, but it will be distorted, taking some time to rise to the 3 volt input voltage level, and then to fall to the 0 volt input voltage level. The time it takes to rise or fall to within 1/e (in this case, to within approximately 1 division on the scope) of the final constant voltage level is the RC time constant of the circuit. For the 1 kΩ resistor and 1 μF capacitor used in Fig. 2, this time constant is 1 msec, corresponding to 1 division on the scope. Increase the sweep speed of the scope to 0.2

msec/division so you can see the rise time in more detail. Change the slope on the external trigger and readjust the level, so you can see the fall time.

Return the sweep speed of the oscilloscope to 1 msec/division, and change the frequency of the function generator to 500 Hz. Each positive half cycle of the square wave is now one time constant long (and so is each negative half cycle). Examine the output at different sweep speeds. *Sketch the waveform you observe.*

Change the frequency of the function generator to 5 kHz, and adjust the sweep speed of the oscilloscope accordingly. This frequency is so high, and the time within a half cycle so short, that the output hardly has time to change at all. *Sketch the waveform you observe. What is its dc level?*

2) Connect the circuit in Fig. 3, and repeat the measurements above. *Sketch the waveforms at the different frequencies.* Note that Figs. 2 and 3 can both be considered as voltage dividers, similar to the circuits in Figs. 2 and 3 in Experiment 2. At very short times the capacitor looks like a short circuit, or a closed switch. At long times the capacitor looks like an open circuit, or an open switch. Using this model of a capacitor is a good way to understand the circuit response at short and long times.

3) Go back to the circuit in Fig. 2, but replace the square wave input with a 3 volt p-p sine wave input. Looking at both the input and output, with the two scope probes, slowly increase the input frequency from 50 Hz to 500 Hz. This circuit is called a "low pass filter". This means that as you move to higher frequencies the output voltage decreases. **Higher frequencies correspond to shorter times.**

At the higher frequencies the impedance of the capacitor decreases, so the output becomes a smaller fraction of the input. We say the "attenuation" of the circuit in Fig. 2 gets greater at higher frequencies. In addition, a phase shift develops between the output and the input waveforms. Measure the output of the circuit for a 1 volt p-p input for about 10 frequencies

between 50 Hz and 500 Hz. *At what frequency is the signal reduced to 1/√2, or about 0.7, of its original amplitude?* This frequency is called the "break point" frequency, and is related to the time constant, RC, by the formula

$$f = \frac{1}{2\pi RC} \qquad (4-2)$$

What is the phase shift at the break point frequency? What is it at much higher frequencies?

4) Repeat the frequency measurements with the circuit in Fig. 3. This is a "high pass filter," so that the response is lower at lower frequencies. **Lower frequencies correspond to longer times.** At the lower frequencies the impedance of the capacitor increases, so the attenuation of the circuit in Fig. 3 gets greater. In addition, a phase shift develops between the output and the input waveforms. As in Part 3, measure the output of the circuit for a 1 volt p-p input for about 10 frequencies between 50 Hz and 500 Hz. *At what frequency is the signal reduced to 0.7 of its original amplitude? What is the phase shift at this frequency? What is it at much lower frequencies?*

ASSIGNMENT

Use your measurements in Parts 3 and 4 to plot the **attenuation**, or ratio of the output voltage to the input voltage (Y axis), as a function of the **frequency** (X axis) from 50 Hz to 500 Hz for the low pass and high pass filters.

Figures

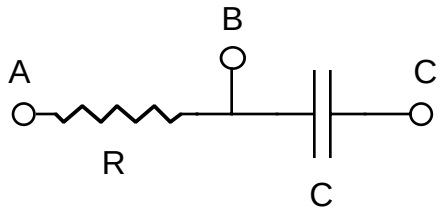


Fig 1

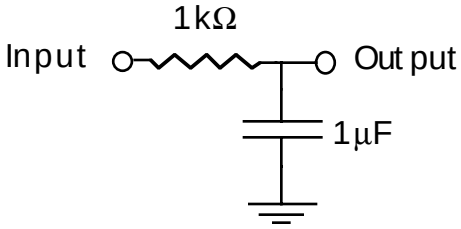


Fig 2

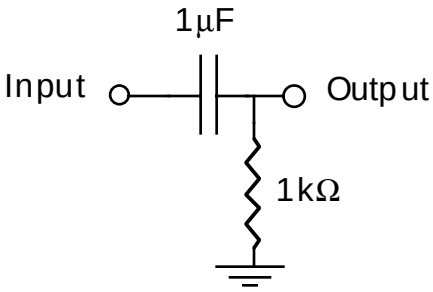


Fig 3

EXPERIMENT 10

CHARACTERIZATION OF OP-AMP CIRCUITS

OBJECTIVE

To study the performance of some typical op-amp circuits.

PROCEDURE

Connect the following circuits:

1) Comparator (Fig. 1). Apply a 1 kHz sine wave signal of about 1 volt p-p to the noninverting (+) input, with the inverting (-) input grounded. Observe this signal on the oscilloscope, triggering on external. Sketch the output. *Does it change if you reduce the input voltage to 0.1 volt? What is the effect of grounding the + input and connecting the signal to the - input?*

2) Follower (Fig. 2). Apply the same signal to the input as in part (1). Note that with negative feedback (to the inverting input) the op-amp adjusts its output so that the inverting input is at the same voltage as the noninverting input. *What is the signal at the output? What is the input impedance of the circuit? What happens with a square wave input?*

3) Non inverting amplifier (Fig. 3). The two 1 kΩ resistors divide the signal at the output of the amplifier by a factor of two. In order for the voltages at the two inputs to the amplifier to be equal the circuit must have a gain of two. Apply the same signal as in part (1) to the input. *What is the signal at the output? What is the signal at the inverting input? What is the gain of the amplifier? What happens when the input voltage is too large? What happens with a square wave input? How would you change the circuit to make the gain equal to 10?*

4) Inverting amplifier (Fig. 4). In this circuit the noninverting input is at ground. In order to keep the inverting input near ground the amplifier must "balance" a positive input with a negative output, and *vice versa*. Measure the voltage at the inverting input. The inverting input is said to be at a "virtual ground." Observe the performance of the amplifier on the oscilloscope. *What is the gain of the amplifier? What happens if you connect the inverting input to a "real" ground?*

The input impedance of a circuit is the ratio of the input voltage to the input current. With a 1 volt input, calculate the current flowing through the 1 kΩ input resistor. *What is the input impedance of the circuit? How would you change the circuit to make the gain equal to -10?*

5) Differentiator (Fig. 5). This circuit differentiates the input voltage. Since the inverting input is at a virtual ground, the current flowing through the 1 kΩ resistor, and hence the output voltage, is proportional to the derivative of the voltage across the 0.2 μF capacitor.

$$I(1k\Omega) = C\frac{dV}{dt} \qquad (10-1)$$

Apply the same signal as in part (1) to the input. *What is the signal at the output?* (**Careful** - be sure to trigger the scope on external or you may miss the 90° phase shift!) *What is the output with a triangular wave input?*

6) Integrator (Fig. 6). In this circuit the capacitor and the resistor are interchanged and the signal is integrated instead of differentiated. In addition, a 100 kΩ resistor has been added to prevent any input offset voltage that might be present from driving the output of the op-amp to one of its extreme limits. Apply the same signal as in part (1) to the input. *What is the signal at*

the output? (Better trigger the scope on external again!) *What is the output with a square wave input?*

7) D/A converter (Fig. 7). The op-amp in this circuit is effectively an inverting amplifier with four separate inputs. Because the inverting input is held at a virtual ground, currents from the four inputs are added and flow together into the output resistor. The values of the four input resistors have been chosen so that each one causes approximately twice as much current to flow as the previous one. Measure the output voltage as a function of the digital input, using the following series:

0	0000	all inputs grounded
1	0001	1st input at 5 Volts
2	0010	2nd input at 5 Volts
3	0011	1st and 2nd inputs at 5 Volts
	etc.	
10	1010	?

ASSIGNMENT

Using your measurements of the D/A converter, plot the **output voltage** (Y axis) as a function of the **digital input** (X axis). Draw a straight line fit to the data.

Figures

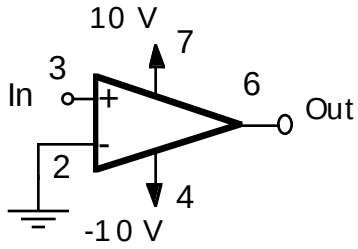


Figure 1

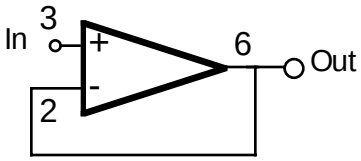


Figure 2

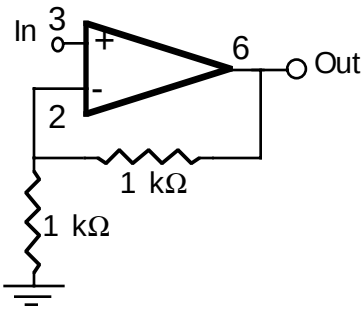


Figure 3

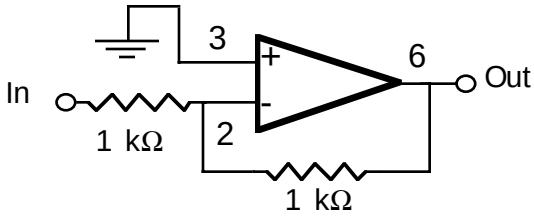


Figure 4

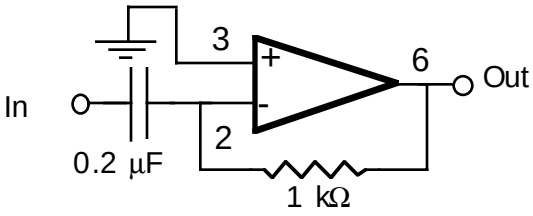


Figure 5

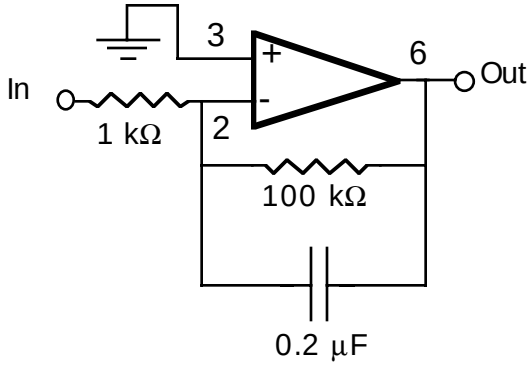


Figure 6

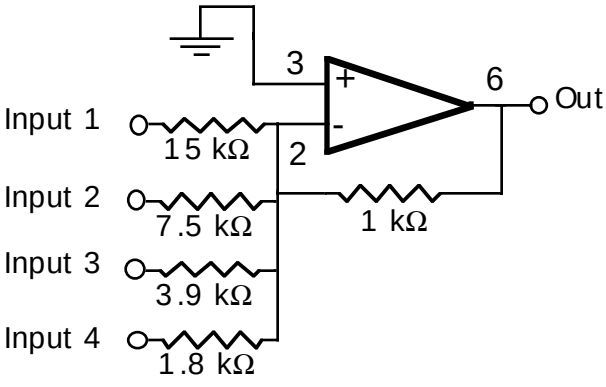
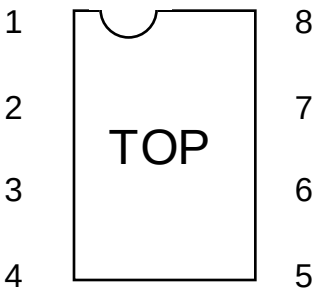


Figure 7



EXPERIMENT 3

SILICON DIODES

OBJECTIVE

To study the characteristics and applications of silicon diodes.

THEORY

Diodes are **nonsymmetrical** electrical devices. They conduct better when one end, called the **anode**, is positive with respect to the other end, called the **cathode**. Physical diodes are often marked with a line, like a minus sign, at the cathode, signifying that the diode will conduct better when this end is more negative than the other end. The symbol for a diode contains an arrowhead pointing from the anode to the cathode, which is the direction in which the current preferentially flows.

There are several useful approximations to describe the operation of diodes in circuits:

1) Crude. The diode is a short circuit, like a closed switch, when voltage is applied in the forward direction, and an open circuit, like an open switch, when the voltage is applied in the reverse direction. This is also called the "ideal diode" approximation, and is usually a good starting point in understanding a new circuit.

2) Standard. The diode is a 0.7 volt source, with no series resistance, when voltage is applied in the forward direction, and an open circuit when the voltage is applied in the reverse direction. This somewhat better approximation tries to account for the voltage drop across the diode when current is flowing through it in the forward direction by saying that the voltage across the diode is always exactly 0.7 volts.

3) Theoretical. Theoretically, the current through many silicon diodes at room temperature is related to the voltage across them by the equation

$$I = I_0\left(e^{\frac{V}{kT}} - 1\right) \approx I_0 \; e^{\frac{V}{26mV}} \qquad (3-1)$$

where k is Boltzman's constant, T is the absolute temperature, and I_o is the "leakage" current when the diode is reverse biased. This approximation implies a theoretical value for the differential resistance of the forward conducting diode. The differential resistance of the diode, *r*, which is also called the "ac" resistance, relates the change in voltage to a change in current:

$$r_d = \frac{\delta V}{\delta I} \qquad (3-2)$$

where δV and δI are small changes in the voltage and current in the diode from its operating point. For many silicon diodes at room temperature *r* is given approximately by

$$r = \frac{26mV}{I} \; ohms \qquad (3-3)$$

where I is the current in amps flowing through the diode. This resistance is often only a few ohms. It is in series with the 0.7 volts already present in the standard approximation.

The current - voltage characteristics of the three models are shown with the figures.

PROCEDURE

1) Connect the circuit in Fig. 1, and apply voltages varying from -10 to 10 volts to the input, in one volt increments. With the digital voltmeter, measure and record the output voltages. *How do your results compare with the crude approximation? How do they compare with the standard approximation?*

2) Connect the circuit in Fig. 2, and apply voltages from -10 to 10 volts to the input, in one volt increments. With the digital voltmeter, measure and record the output voltages. Since the output does not change much, be sure to measure to three significant figures. *How do your results compare with the crude approximation? How do they compare with the standard approximation?*

3) Connect the circuit in Fig. 3 and apply voltages from -2 to 2 volts to the input, in 0.2 volt increments. With the digital voltmeter, measure and record the output voltages, again to 3 significant figures. This circuit is called a "limiter." It permits small input voltages to pass without attenuating them at all, but it **limits** the output to at most about ± 0.7 volt with large input voltages. Note that in the crude approximation this circuit would not work at all; the two ideal diodes "back to back" would simply constitute a short to ground and the output would always be zero.

ASSIGNMENT

Using your measurements for Figs. 1, 2, and 3, plot the **output voltages**, (Y axes), as a function of the **input voltages**, (X axes). On the same plots, show the outputs that would be expected in the crude and standard approximations.

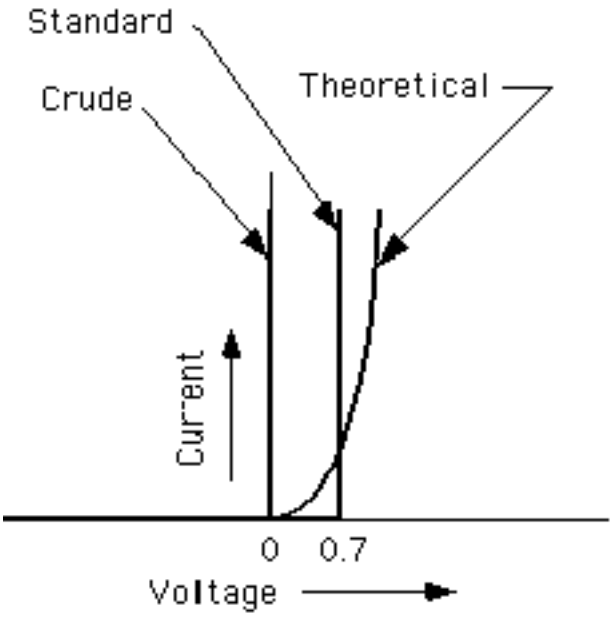
Use the data from the part 2 to compute the current flowing through the diode. This is the same as the current flowing through the 1 kΩ resistor, since there is no place else for that current to flow. The current through the 1 kΩ resistor may be computed, using Ohm's law, from

$$I = \frac{(V_{in} - V_{out})}{1\ k\Omega} \qquad (3-4)$$

Plot the **current** flowing through the diode (Y axis) as a function of the output voltage, which is the **voltage across the diode** (X axis). On the same plot show the current - voltage relationship expected in the standard approximation. *What is the maximum voltage difference between your experimental data and the standard approximation?*

Using the same data, compute the differential resistance of the diode from equation (3-2) by taking differences between successive data points for ΔV and ΔI. Plot the differential **resistance** (Y axis) as a function of the **current** (X axis) through the diode. The current used in this plot should be the average of the two successive values that form ΔI. For comparison, also plot equation (3-3) on the same graph. *How does your plot of differential resistance compare with the theoretical approximation in equation (3-3)?*

Figures



Diode Models

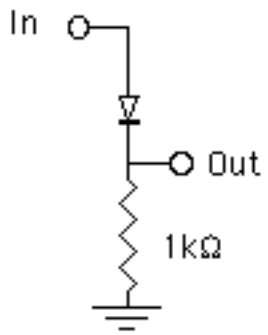


Figure 1

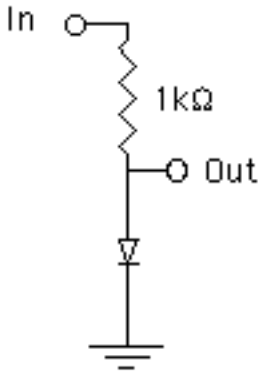


Figure 2

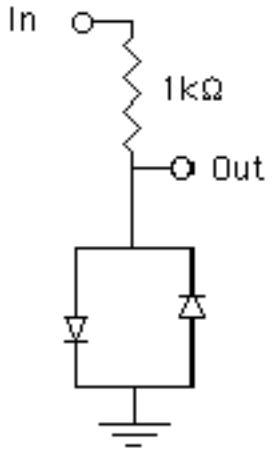


Figure 3

EXPERIMENT 5

HALF WAVE RECTIFIERS

OBJECTIVE

To study the characteristics and operation of half wave rectifiers and filter circuits.

PROCEDURE

1) Connect the circuit in Fig. 1, using a 20 volt p-p square wave at 60 Hz as the input. The square wave should have a minimum value of -10 volts, and a maximum value of +10 volts. Trigger the scope on external, at a sweep speed of 2 msec/division, so as to observe slightly more than one cycle. Set both channels at 5 volts/division, **dc**, and place both probes on the input. Then, leave one probe on the input, and observe the output with the other probe.

The circuit in Fig. 1 is the same as the circuit in Fig. 1 of Experiment 3, and your results should be very similar. When the input is at +10 volts, the output will also be at +10 volts, or, more exactly at +9.3 volts, allowing for the 0.7 volt drop across the diode. When the input is at -10 volts, the output will be at 0 volt, since the diode is reverse biased and does not conduct. The circuit is called a "half wave rectifier" since only one half, in this case the positive half, of the input appears at the output.

2) Connect the circuit in Fig. 2, using, first, the 1 μF capacitor. The positive half cycle at the output should look the same as before. However, during the negative half cycle, when the diode is reverse biased, the output doesn't drop immediately to 0 volts. Instead, the capacitor discharges through the resistor causing the output voltage to decay exponentially to 0 volts, with a time constant of 1 msec. *Sketch the waveform at the output.*

3) Replace the 1 μF capacitor in the circuit in Fig. 2 with a 100 μF capacitor. Exactly the same things happen as before, but now the time constant, 100 msec, is so long that the output doesn't have a chance to decay to 0 volts before the next positive half cycle comes and brings the output back to 9.3 volts. *How much does the voltage decrease during the negative half cycle? Sketch the waveform at the output.*

The amount by which the voltage decreases is called the "ripple." Many times it is desirable for the ripple to be as small as possible, for example in a power supply. Obviously, increasing the time constant will decrease the ripple. *Based on your observations with this capacitor, how big a capacitor would be required to reduce the ripple to 0.1 volt?*

4) Repeat parts 1 through 3 with a 20 volt p-p sine wave instead of a square wave. The ripple in part 3 should be larger than before, since there is more time available for the exponential decay, but otherwise the results should be very similar. *Sketch the waveform at the output. Identify the region in which the output in Fig. 2 undergoes exponential decay. How large is the ripple with the 100 μF capacitor?*

5) Connect the circuit in Fig. 3. This uses an additional filter stage to reduce the ripple. The 100 Ω resistor is a trade-off; the larger this resistor is, the greater the time constant, and therefore the greater the reduction in the ripple. However, the dc voltage drop across the resistor also becomes greater because of the current drawn by the 1 kΩ load. *What is the ripple observed with this filter stage in place?* Switch the scope to ac for this measurement only. This allows the gain to be increased enough to measure the ripple easily. *How much does the 100 Ω resistor reduce the dc output voltage across the 1 kΩ load (*short it out to see*)? How much does the ripple increase when the 100 Ω resistor is shorted out?*

Figures

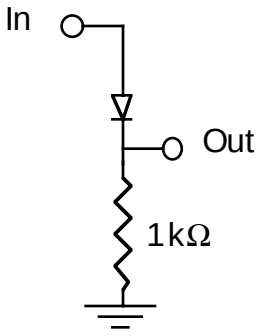
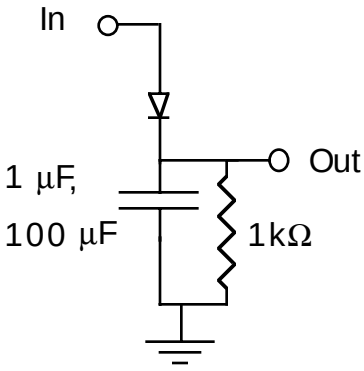


Fig 1



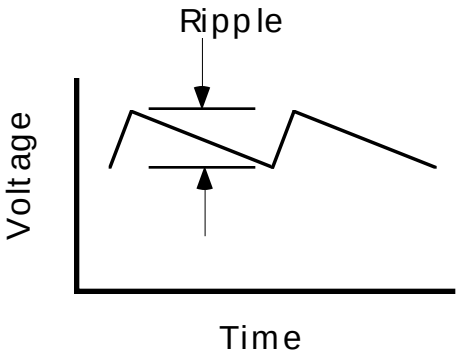


Fig 2

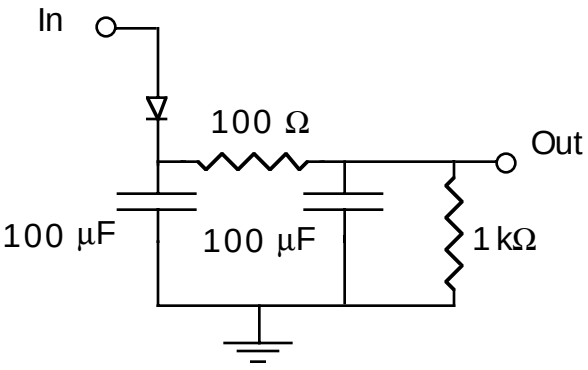


Fig 3

EXPERIMENT 7

DIODE APPLICATIONS

OBJECTIVE

To study the applications of diodes in logic circuits and as light emitters and detectors.

PROCEDURE

1) Connect the circuit in Fig. 1. This is an OR gate, as might be used in a digital circuit. It's name is derived from the fact that the output is high if either input 1 or input 2 is high. This is true because whichever input is high, the diode connected to that input will conduct, and cause the output to be high. *What would happen if both inputs were high ?*

Connect input 1 to a TTL signal from the function generator (0 to +3 volt square wave) at a frequency of about 1 kHz, and observe both the input and the output of the circuit on the scope, triggered on external. *Sketch the output waveform.* Repeat, with input (2) connected to the plus 5 volt supply. *Sketch the output waveform. Is there any loss in signal height?*

2) Connect the circuit in Fig. 2. This is an AND gate, because the output is high only if both input 1 and input 2 are high. Repeat the measurements you made in part (1) for this circuit. *Sketch the output waveforms for both cases. Is there any output with 0 volts on both inputs?*

Although these experiments should work well, diode gates are not often used in logic circuits. *Why should this be true?* (Hint: Suppose you used the output of the AND gate to drive one of the inputs of the OR gate.)

3) Connect the circuit in Fig. 3, using a light emitting diode (LED). This diode has the property that when it is forward biased it emits light which is proportional to the current flowing through it. Because it is made of a gallium aluminum arsenide compound instead of silicon the turn on voltage is much larger than the usual 0.7 volts. Apply voltages of between 1 and 10 volts

to the input of the circuit, and observe the light coming out of the diode and the voltage at point A. *What is the approximate turn on voltage of the diode?* Apply sine wave and square wave forms to the input at frequencies between 1 and 10 Hz. *Can you see the difference between a sine wave drive and a square wave drive?* Use the dc offset control to bias the drive voltage so that the diode is never turned off. Adjust this control and the amplitude control to get as bright an output from the diode as possible.

4) The circuit in Fig. 4 uses a silicon photodiode to detect the light from the LED. This diode has the property that it generates a current which is proportional to the incident light falling on it. The simplest, and sometimes the most sensitive way of using a photodiode is to measure the voltage developed across it by the incident light. Connect the photodiode directly to the scope probe, and point it at the LED. Be sure to keep the photodiode far enough away from the LED so that the signal does not exceed a few tenths of a volt - otherwise the forward turn-on characteristics of the photodiode may distort the signal. *Sketch the output across the photodiode. How does the signal you observe with the photodiode compare with the original signal driving the LED?* Increase the frequency of the signal generator to about 1 kHz. Does the signal you observe still have the same characteristics as observed at the lower frequency? *At what frequency does the LED seem to stop blinking, even though the wave form on the scope shows that it still is?*

The background light from the room is also detected by the photodiode. This may change its operating point, and therefore the gain of the circuit in Fig. 4. In addition, since the room lights may be modulated, the background light can cause an unwanted ac signal. *What happens to the signal as you shield the photodiode from the room lights?*

Figures

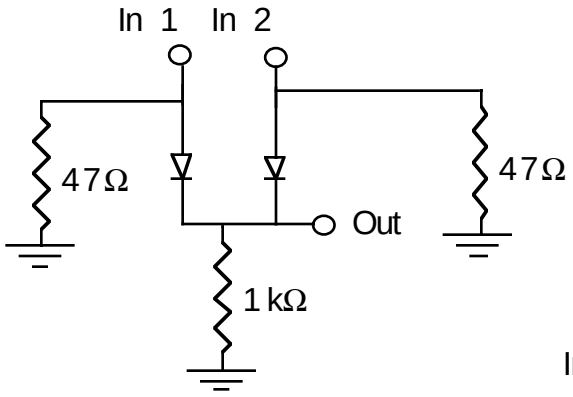


Figure 1

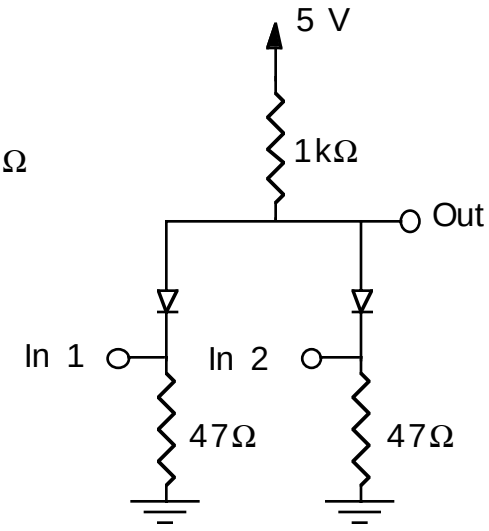


Figure 2

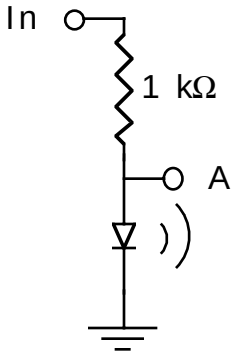


Figure 3

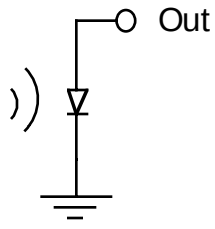


Figure 4

EXPERIMENT 9

FIELD EFFECT TRANSISTORS

OBJECTIVE

To characterize enhancement and depletion mode field effect transistors, and to implement a CMOS inverter.

THEORY

As the name implies, the current which flows through field effect transistors is controlled by an electric field. This field arises from a potential applied to the control electrode, or gate, which is separated from the rest of the transistor by a very good insulator or a reverse biased pn junction. Consequently, there is almost no input current, and the input resistance is virtually infinite. This is very different from the case of bipolar transistors, which are controlled by the input (base) current.

PROCEDURE

1) Connect the circuit in Fig. 1. **Be sure to connect pins 7 and 14 as shown.** Measure the voltages at points G (the gate electrode) and D (the drain electrode) as the input voltage is varied from 0 to 5 volts in 0.5 volt steps. Compute the drain current from the voltage drop across the 10 kΩ drain resistor, using the formula

$$I_d = \frac{5 - V_D}{10 \ k\Omega} \qquad (9-1)$$

Is there any difference between the input voltage and the voltage on the gate? Even though there is a large, 100 kΩ resistor between these two points they should be at the same potential, because the gate current is zero. However, digital meters typically have an input resistance of 10 Megohms, which would reduce the voltage on the gate by about 1%.

Compared to bipolar transistors, field effect transistors require a much larger voltage swing to turn on. The voltage at which they start to turn on is called the threshold voltage. *What is the threshold voltage, V_t, for this transistor?* It is an "n-channel" FET, roughly corresponding to npn bipolar transistors. There are also some p-channel FET's on the same chip, and they are used in part (3) below. Because a positive gate to source voltage is required for drain current in this n-channel device, this is called an "enhancement" mode FET.

2) Connect the circuit in Fig. 2. This is exactly the same as the circuit in Fig. 1, except that the transistor is a "depletion" mode field effect transistor, for which there is a drain current with zero volts on the gate with respect to the source. Measure the voltages at the gate electrode and the drain electrode as the input voltage is varied from -5 volts to 0 in 0.5 volt steps. Compute the drain current as before, using equation (1). *What is the threshold voltage for this transistor?*

3) Connect the circuit in Fig. 3. This is a very common arrangement found in CMOS (complimentary metal oxide semiconductor) integrated circuits, and uses a p-channel FET in place of the 10 kΩ resistor in Fig. 1. Measure the output voltage as the input is varied from 0 to 5 volts in 0.5 volt steps. *At what input voltage does the output "switch" from high to low? Over what voltage range does the transition occur?*

The performance of the circuit in Fig. 3 is analogous to that of the two switches in Fig. 3a. When the bottom switch is closed, and the top switch is open, the output voltage is 0 volts. When the bottom switch is open, and the top switch is closed, the output voltage is 5 volts. But the two switches should never be both open at the same time or (even worse!) both closed at the same time. *What input voltage in Fig. 3 corresponds to the switch positions shown in Fig. 3a?*

Because of their thresholds, either the bottom transistor (the n-channel one) or the top transistor (the p-channel one) conducts, depending on the input voltage. However, both cannot be on (or off) at the same time. This has some very useful consequences:

1) A good low output is obtained when the n-channel transistor is conducting and the p-channel transistor is turned off (high input voltage).

2) A good high output is obtained when the p-channel transistor is conducting and the n-channel transistor is turned off (low input voltage).

3) In both cases above no current flows through the two transistors (since one or the other is off, in both cases). This strategy minimizes the total current, and therefore the power dissipated, in the integrated circuit. For modern VLSI chips, with many millions of transistors on a chip, this is a crucial consideration.

ASSIGNMENT

Using the data from Part 1, plot the **drain voltage** (Y axis) and the **drain current** (Y axis) as a function of the **voltage on the gate** (X axis).

Repeat the two plots above, using the data from Part 2 for the depletion mode transistor.

Using the data from Part 3, plot the **output voltage** (Y axis) of the CMOS pair as a function of the **input voltage** (X axis). This is called the “transfer” characteristic of the gate circuit.

Figures

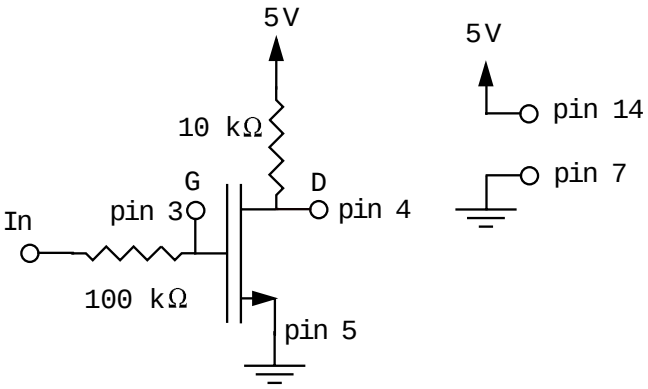


Figure 1

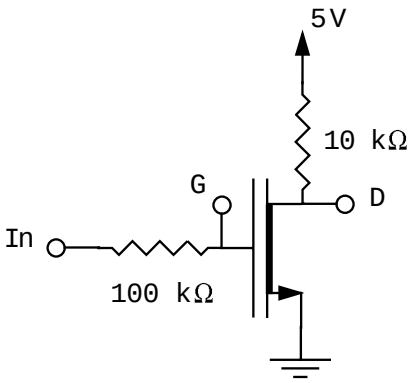


Figure 2

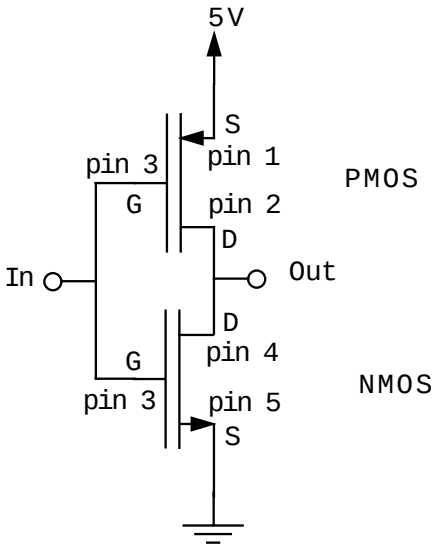


Figure 3

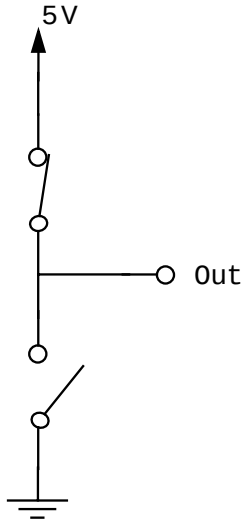
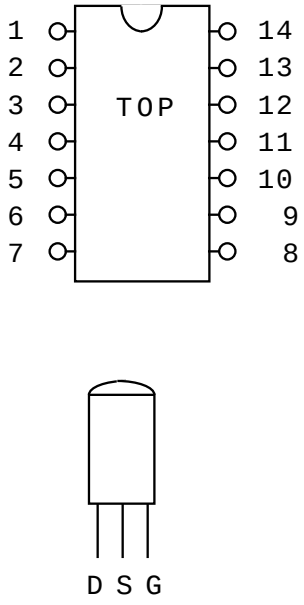


Figure 3a



FET pin connections

EXPERIMENT 8

BIPOLAR TRANSISTORS

OBJECTIVE

To characterize an npn bipolar transistor, and measure the dc operating point and the ac performance of a single transistor amplifier.

THEORY

Bipolar transistors are semiconductor devices that contain two pn junctions, similar to the junctions in diodes. For the npn transistor the p type material is common to both junctions, so that there is first an np junction and then a pn junction. However, a transistor is a lot more than two diodes in series, because it has a current gain, as discussed below.

PROCEDURE

1) Connect the circuit in Fig. 1, and use the potentiometer to vary the voltage at the input in 1 volt steps from 0 to 10 volts. Note that this is very similar to Fig. 2 in Experiment 3, because there is a diode junction from the "base" of the transistor, point B, to the "emitter" of the transistor, which is connected to ground. As you did in Experiment 3, record the voltage V_B at point B. In addition, record the voltage at point C, which is the "collector" of the transistor.

The current I_b which flows into the base of the transistor also flows through the 100 kΩ resistor, so it can be computed from

$$I_b = \frac{V_{in} - V_B}{100\ \ k\Omega} \qquad (8-1)$$

One can then compute the differential resistance of the emitter to base junction of the transistor, also called the "base impedance" of the transistor, the same as was done in Experiment 3. However, it is more interesting to look at the voltage at point C, which is the collector of the transistor. With the input at zero volts, no current flows either to the base or to the collector of the transistor. The transistor is said to be "cut off." The voltage at point C is 10 volts, the same as the supply voltage. This is because no current flows through the 1 kΩ collector resistor. However, as the base current increases, the collector current also increases, causing a voltage drop across the 1 kΩ resistor. The collector current is roughly proportional to the base current:

$$I_c = \beta I_b \qquad (8-1)$$

where β is the current gain of the transistor. Increase the input voltage in 1 volt steps and measure the collector voltage V_c and the base voltage V_b.

2) Connect the circuit in Fig. 2, without connecting the potentiometer. Note that the base is held near ground (by the 100 Ω resistor), and the emitter is attached to a 1 kΩ resistor to -5.7 volts. Therefore, the emitter-base junction is forward biased, and the emitter is at a potential of -0.7 volts, approximately 0.7 volts more negative than the base. (If the 1 kΩ emitter resistor were returned to some positive potential, +V, the emitter-base junction would be reverse biased and the emitter would go to +V. However, the emitter can't go more than about 0.7 volts negative with respect to the base because the emitter-base junction conducts. If you ever see a larger voltage (in a silicon device) throw the transistor away - it's burned out. The emitter current is the same as the current through the 1 kΩ emitter resistor; since there are 5 volts across this resistor (5.7V-0.7V), from Ohm's law the emitter current is 5 mA.

Almost all the 5 mA flows into the collector (only a little, 1/β, which is on the order of 1 %, flows into the base). Therefore there is approximately a 5 volt drop across the 1 kΩ collector resistor, and since the supply end of the resistor is at +10 volts, the collector end is at 5 volts. The circuit is said to bias the transistor in the middle of its operating range, since the collector can both increase and decrease in voltage by 5 volts without becoming either more positive than the supply voltage or more negative than the base. This is often a desirable way to bias a transistor in an analog circuit. Note that small changes in component values or voltages will only result in small changes in the operating point - it will always be pretty close to 5 volts.

Connect the potentiometer and use it to apply 0 to 1 volts to the base of the transistor (point B) in Fig. 2, in 0.1 volt steps, and measure the voltages at the collector, point C, and the emitter, point E.

Gain is defined as the change in output voltage (ΔV_{out}) divided by the change in input voltage (ΔV_{in}). Use your dc measurements to calculate the gain of the circuit from the input to the output at point E, and from the input to the output at point C.

Disconnect the potentiometer, and apply a 0.2 volt p-p signal at about 1 kHz to the base (point B), and observe the collector (point C) and the emitter (point E) with the scope. Because the series 1 kΩ resistor attenuates the signal, about 2 volts p-p is required at the input. *Based on these waveforms, what is the gain of the circuit from the input to point E? What is the gain of the circuit from the input to point C?*

This circuit biases the transistor right in the middle of its range, which is desirable, but its gain is quite low. **TRICK**: Connect a 10 μF capacitor from point E to ground. This has two consequences:

1) For dc the capacitor is an open circuit (infinite impedance) so nothing happens. The transistor remains biased as before.

2) For a high enough ac frequency the capacitor is a short circuit (almost zero impedance) so the emitter is grounded. The gain therefore becomes as large as in part 1.

Apply a small signal (much less than 0.1 volt p-p) to the input, and observe the signal at the collector, point C. *How large is the gain from the input to point C?* **Careful:** you will probably have to reduce the input signal still further to prevent the output from "clipping," or being limited at its high and low voltage limits. Note that because the transistor is biased in the middle of its active range the clipping is symmetrical.

How high in frequency does the ac signal have to be in order for the capacitor to look like a short circuit? Vary the input frequency to find a lower frequency where the gain drops to 0.71 of its high frequency value. This frequency is called the break point frequency (the full analysis of this is called a Bode plot).

Another way of studying the frequency response is to apply a (small) square wave to the input at about 100 Hz. For **short** times, corresponding to **high** frequencies, the capacitor acts as a short circuit and the gain is very high. For **long** times, corresponding to **low** frequencies, the gain is low. *Sketch the output waveform with the square wave input.*

ASSIGNMENT

Use your voltage measurements in Part 1 to compute the base current and the collector current. Plot the **collector current** (Y axis) as a function of the **base current** (X axis). This plot should be nearly linear; the ratio of collector current to base current is called the dc β. What this plot shows is that the transistor is a good current amplifier, since a relatively small base current (the input current) controls a much larger collector current (the output current).

Using the same data, plot the **collector voltage** (Y axis) as a function of the **base current** (X axis). Note that as the collector current *increases* the voltage at the collector *decreases* because there is a larger voltage drop across the 1 kΩ collector resistor.

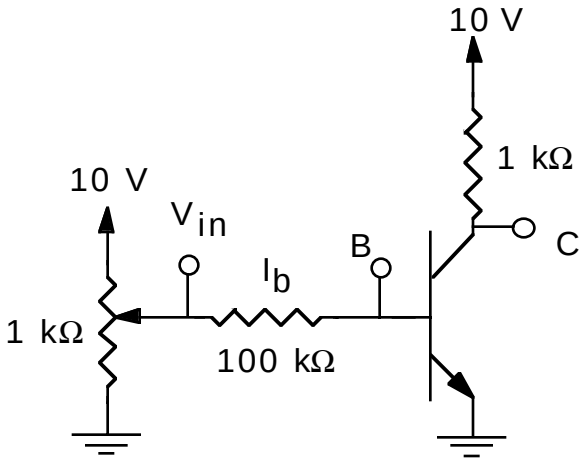
Now plot the **voltage at the collector**, point C, (Y axis) as a function of the **voltage at the input** (X axis). This shows that the circuit is a voltage amplifier, since the voltage at the collector (the output voltage) is controlled by the voltage at the input (the input voltage). Unfortunately it's not a very good amplifier: the gain, or the change in output voltage divided by the corresponding change in input voltage, is not very high. However, suppose the circuit is redefined, so that the input is considered to be at the base, point B? In that case your measurements would show that the circuit has a very high voltage gain, since the input, point B, hardly changes in voltage at all while the collector changes from 10 volts to almost zero. However, it's still not a very good amplifier, for two reasons:

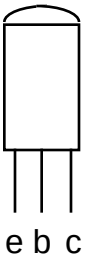
1) It has a very low input impedance, because the base-emitter junction is a forward biased diode. Usually an amplifier should have a high input impedance.

2) The gain occurs for an input voltage of about 0.7 volts. Usually an amplifier should work best when its input is near zero. Worse yet, the 0.7 varies, from transistor to transistor, even for the same transistor at different temperatures.

Using your measurements in Part 2, plot the **collector voltage** (Y axis) and the **emitter voltage** (Y axis) as a function of the **input voltage** (X axis). *What is the ac voltage gain of the circuit from the input to the collector (point C)? What is the ac voltage gain of the circuit from the input to the emitter (point E)?*

Figures





Transistor pin connections

Fig 1

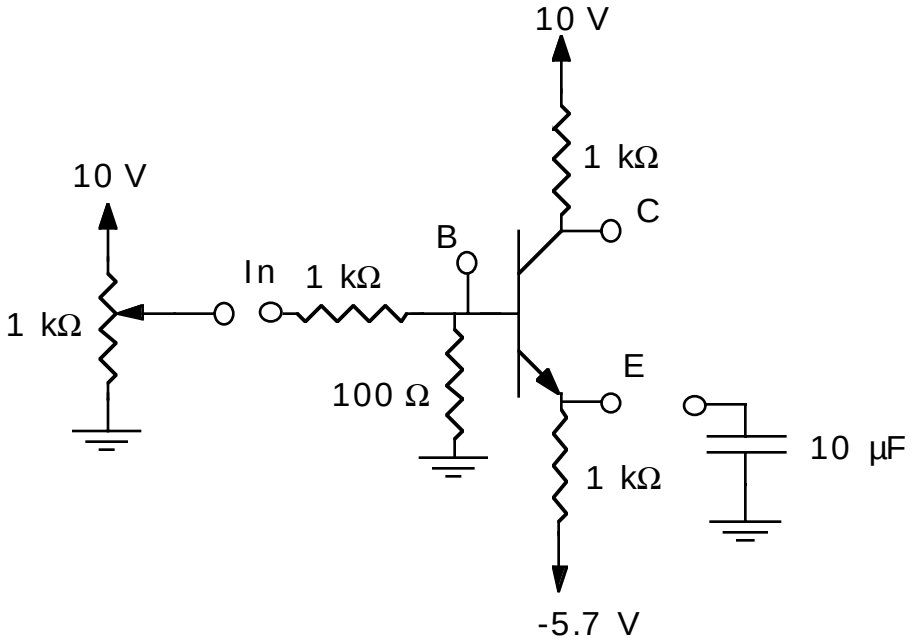


Fig 2

EXPERIMENT 11

TRANSISTOR CURVE TRACER

OBJECTIVE

To apply the principles developed in the experiments performed so far to construct a transistor curve tracer, and to use the transistor curve tracer to measure the characteristics of npn transistors.

THEORY

Transistor curve tracers are commonly used to observe the characteristics of bipolar and field effect transistors as well as other devices. In this experiment you will construct such an instrument. The various sections of the curve tracer are treated separately.

For an npn transistor the voltage applied to the collector must sweep from zero to a few volts positive. A convenient voltage is obtained from the 60 Hz line, by full wave rectifying (without filtering) a center tapped transformer (Fig. 1). It is convenient to think of this waveform as consisting of four different sections: there are two half cycles, corresponding to conduction by the two different diodes, and each half cycle is divided into an increasing and a decreasing voltage region.

The current applied to the base is obtained from large resistors which are connected to the outputs of two op-amps (Fig. 1). The first op-amp is driven as a comparator by one section of the transformer. Thus its output is positive during one half cycle, and negative during the other half cycle.

The second op-amp also acts as a comparator, but after the ac voltage has passed through an RC network. The time constant of this network has been chosen to be quite short, so the sine

wave is shifted in phase by almost 90°. Therefore, the output of the op-amp is positive during the rising portion of one half cycle, and during the falling portion of the other.

The resistors from the outputs of the op-amps supply current to the base of the transistor under test. These currents are ± 0.005 mA for the 2 Megohm resistor and ± 0.01 mA for the 1 Megohm resistor. An additional 620 kΩ resistor to the positive supply assures that the sum of the currents to the base of the transistor is always positive (or zero). There are altogether four combinations of current, corresponding to whether the outputs of each op-amp are positive or negative. The values of the resistors have been chosen to produce base currents of 0, 0.01, 0.02, and 0.03 mA. If the β of the transistor under test is 100, for example, this should result in collector currents of 0, 1, 2, and 3 mA.

The current through the transistor flows through a 100 Ω resistor from the emitter to ground. This value resistor is small enough so only a few tenths of a volt is generated at the emitter. Consequently, the emitter voltage has negligible effect on the current flowing to the base. Note that what is measured is actually the emitter current, which is only approximately equal to the collector current.

PROCEDURE

Set the oscilloscope on "X-Y" operation, with the X axis at 1 volt/division, and the Y axis at 0.1 volt/division. The X-axis scale directly indicates the voltage on the collector of the transistor under test. Because of the 100 Ω resistor, the Y axis scale is equivalent to 1 mA/division. Since the Y axis signal level is relatively low, use a cable (or a 1X probe) to make the connection, to minimize the effects of noise. You may also want to reduce the noise further with a capacitor to ground or a resistor in series with the Y axis output (not shown in Fig. 1).

Measure the characteristics of several npn transistors. *What values of β do you observe?* Try heating the transistor by squeezing it between your fingers. Can you get the β to change?

The curve tracer can also be used to measure the forward conduction characteristics of a diode, with the cathode connected to the emitter terminal and the anode connected to the collector terminal. However, the forward current will be very high, since it is limited only the 100 Ω resistor. Before attempting this **put a current limiting resistor**, such as a 1 kΩ resistor, between the anode end of the diode and the collector terminal, and expand the X-axis scale to 0.1 volt/division to clearly see the curve.

ASSIGNMENT

Design a curve tracer to work with pnp transistors.

Design a curve tracer that can test both npn and pnp transistors. Hint: The transistors may either plug into the same socket, in which case some voltages will have to be switched, or they may plug into different sockets. Which do you prefer?

Figures

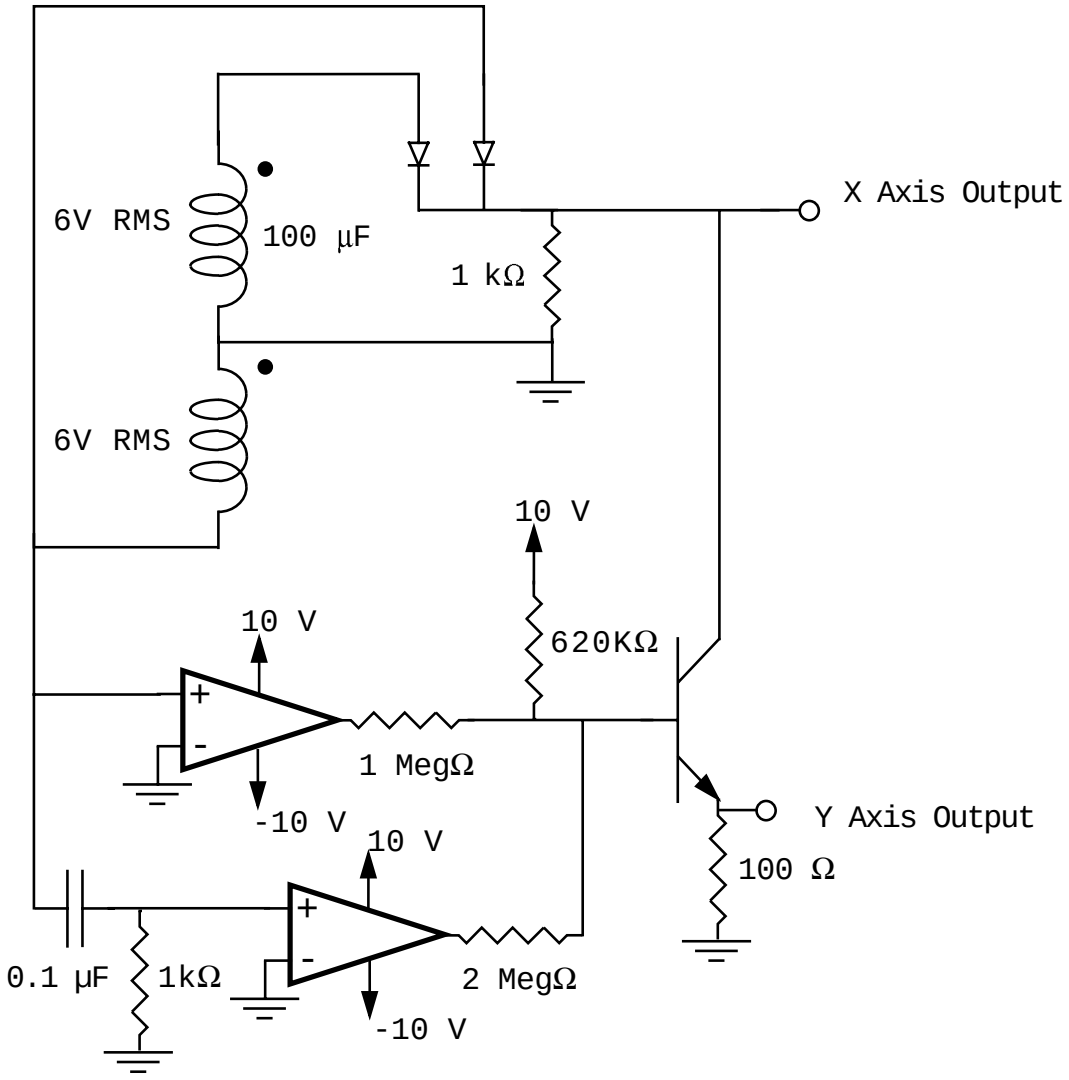


Fig 1

EXPERIMENT 15

DESIGN OF TEST CIRCUITS FOR BJT'S AND FETS AND DESIGN OF FET RING OSCILLATORS

OBJECTIVE

To design circuits which compare the response of enhancement mode FETs with that of bipolar transistors, to study the performance of CMOS circuits, and to apply ring oscillators to evaluate the high frequency response of CMOS inverters.

THEORY

In contrast to bipolar transistors, field effect transistors require a voltage to turn them on, but almost no current. For enhancement mode FETs the voltage between the gate and the source must exceed a threshold value, V_t, before appreciable current flows. CMOS digital circuits use a P-channel FET in series with an N-channel FET to produce an output voltage which is either high or low. The magnitude of the threshold voltage is carefully selected and controlled so that the P-channel FET and the N-channel FET are not both turned on at the same time in the steady state. This is very important, because it minimizes the steady state current, and hence the power, drawn by the circuit.

PROCEDURE

1) Using the dc offset control on the function generator (for many function generators the appropriate knob must be pulled out) prepare a triangular wave signal that goes from 0 volts to 5 volts at a frequency of 1 to 1.2 kHz. Trigger the 'scope on 'External', so that the positive going ramp from the triangular wave can be viewed. This input signal will be used for most of the experiment; it will generate a variety of different output responses in different circuits.

2) Consider the circuits shown in Figs. 1 through 4, which will be used to test the performance of common collector and drain (Figs. 1 and 2) and grounded emitter and source (Figs. 3 and 4) transistors, respectively. Complete the design, by choosing values for R_1, R_2, R_3, and R_4 to produce reasonable currents and voltages. The function of R_1 is to provide a path to ground in the absence of an input signal. R_2 generates a voltage drop from the base or gate current; since these currents are small, R_2 should be chosen large to make the voltage easier to measure. R_3 and R_4 are load resistors, and should be chosen to match the characteristics of the device under test. **Make sure the chip's pin 14 is at 5 volts and pin 7 is at ground in all the figures.** Observe the waveforms at points A, B, and C. As discussed above the voltage difference between points A and B is a measure of the current drawn from the input signal. *Can you detect any current drawn by the FET?* (**Careful**: The 'scope draws some current!)

Compare the emitter follower in Fig. 1 to the source follower in Fig. 2. The voltage difference between points B and C is a measure of the ability of the output to "follow" the input. For the emitter follower this voltage difference is about 0.7 volt, while for the source follower it is approximated by $V_t + 2I/g_m$ where g_m is the transconductance. *What V_t do you measure on the scope?*

Compare the grounded emitter inverter in Fig. 3 to the grounded source inverter in Fig. 4. The voltage at point C is the output response to the triangular input. *At what input voltage does C start to decrease in voltage?* For the grounded emitter this should be about 0.7 volt, while for the grounded source this should be at V_t.

3) Connect the CMOS circuit in Fig. 5, in which a P-channel FET replaces the load resistor in Fig. 4. Compare the output voltage at point C with the corresponding waveform in Fig. 4. *At what input voltage does the transition occur? For what value of R_4 does the output of Fig. 4 most closely resemble the output of Fig. 5?* Add a resistor to the source (Fig. 6) to measure the current drawn by the circuit. Choose a resistor small enough not to disturb the operation of

the circuit, but large enough to generate a voltage (a few tenths of a volt, maximum) which is easy to measure. *Is there any current? Attach a capacitive load; now is there any current? How does it depend on the value of the capacitor?*

4) Connect the "ring oscillator" circuit in Fig. 7. This is a commonly used circuit to measure the switching time of CMOS gates. It is unstable because it has an odd number of inverters. *At what frequency does it oscillate? What is the switching time of a single gate?* Notice there are no resistors. *Were they needed in the CMOS circuits used before?*

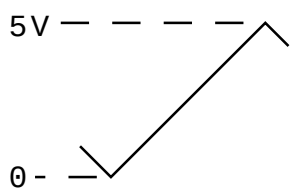
DESIGN OF AUDIO RING OSCILLATOR

The circuit in Fig. 7 oscillates at a few MHz because the rise times at each individual inverting gate are relatively fast. By introducing RC filters these rise times can be made much longer. Using this principle, design a ring oscillator that works at about 1 kHz. You can start by putting large resistors from the output of each gate to the input of the next gate. Then add capacitors from the inputs to ground. In order to oscillate, all three stages must have about the same rise times. Draw the circuit. *What time constant did you start with? What time constant led to 1 kHz oscillation?* Sketch the waveforms you observe at the different terminals.

PSPICE ASSIGNMENT

Set up the arrangements in Figs. 3, 4, and 5 in PSPICE, and apply the 0 to 5 V ramp that you used in the experiment. Compare the output given by PSPICE with the output you obtained experimentally. *Do you expect any differences?*

Figures



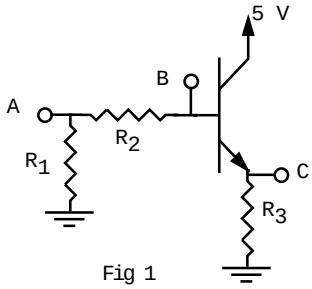


Fig 1

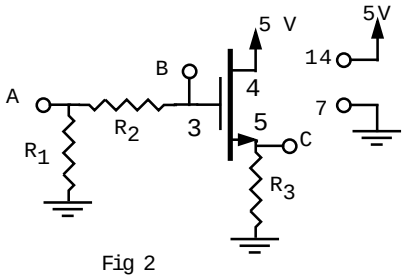


Fig 2

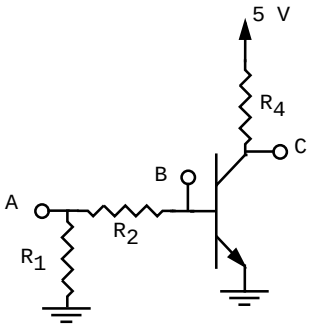


Fig 3

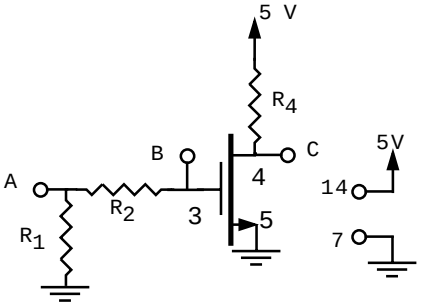


Fig 4

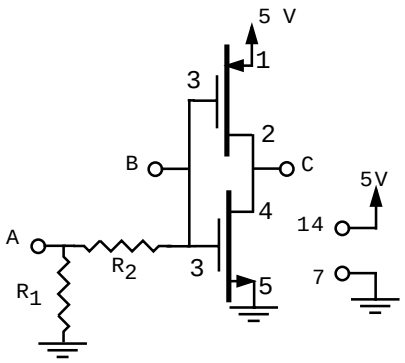


Fig 5

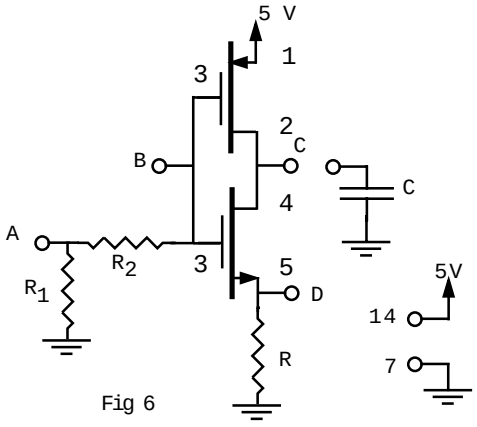


Fig 6

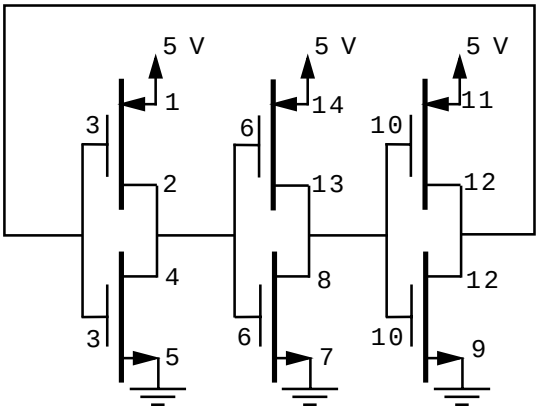


Fig 7