

# Multi-Channel Integrated Circuits for Use in Research with Radioactive Ion Beams

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# Inter-University Collaboration

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# Design Team

## **Southern Illinois University Edwardsville:**

- Dr. George Engel
- Michael Hall (graduate student)
- Justin Proctor (graduate student)
- Vikram Vangapally (graduate student)
- Naveen Duggireddi (graduate student)
- Dinesh Dasari (graduate student)
- Nagendra Sai Valluru (graduate student)
- James Brown (undergraduate student)
- Mytheri Nethi (graduate student)
- Muthu Sadisivam (graduate student)
- Mahadevan Ganesan (graduate student)
- Mohamedsha Malikasari (graduate student)

## **Washington University in St. Louis:**

- Dr. Lee Sobotka
- Jon Elson (electronics specialist)
- Dr. Robert Charity
- Rebecca Shane (graduate student)

# Research Goals

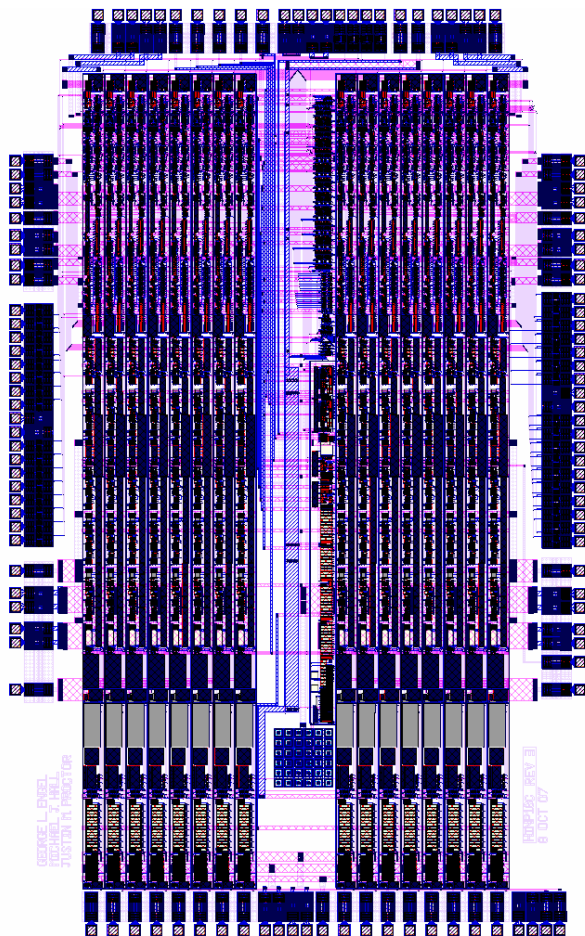
- Our goal is to develop a *family* of multi-channel custom integrated circuits (ICs) suitable for use in a wide variety of low- and intermediate-energy nuclear physics experiments.
- The ICs should be useful in experiments where energy, relative timing, and position information is desired.
- Particle identification using pulse shape discrimination should also be supported.

# Why design custom chips?

- The need for high-density signal processing in the low- and intermediate-energy nuclear physics community is widespread.
- No commercial chips were identified which were capable of doing precisely what the researchers wanted.
- The scientists deemed it necessary for the “experimenter” to be in the “designer’s seat.”
- We envision a “toolbox” of IC circuits, useful for researchers working with radioactive ion beams, which could be composed in different ways to meet the researchers’ evolving needs and desires.

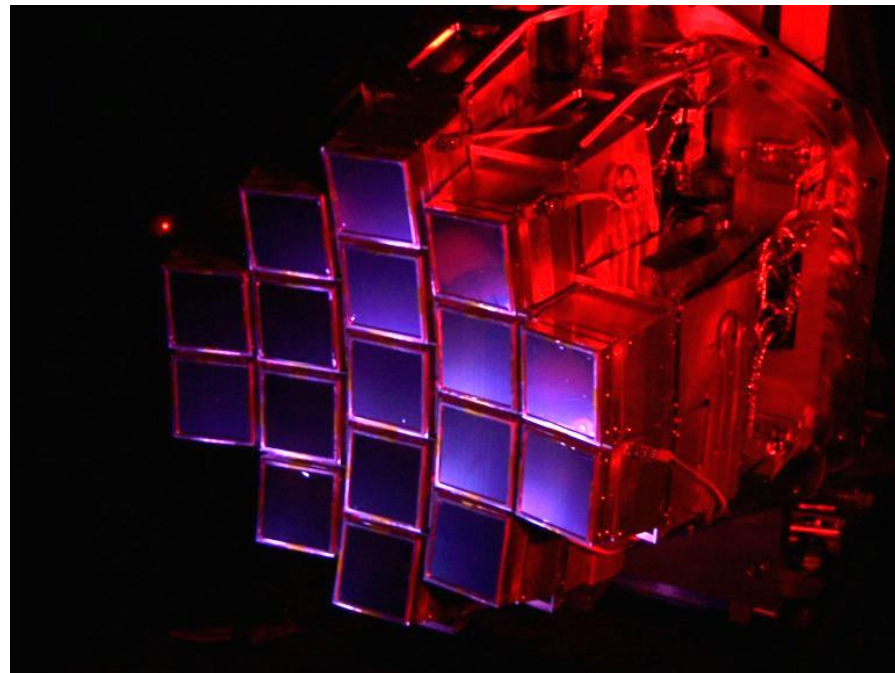
# What have we accomplished thus far?

- First chip was an analog-shaped and peak-sensing chip known as *HINP16C* (Heavy-Ion Nuclear Physics – 16 Channel) and is intended for use with solid-state detectors.
- The second chip, christened *PSD8C* (Pulse Shape Discrimination – 8 Channel), was designed to logically complement (in terms of detector types) the HINP16C chip and is a multi-sampling, PSD-enabling IC.

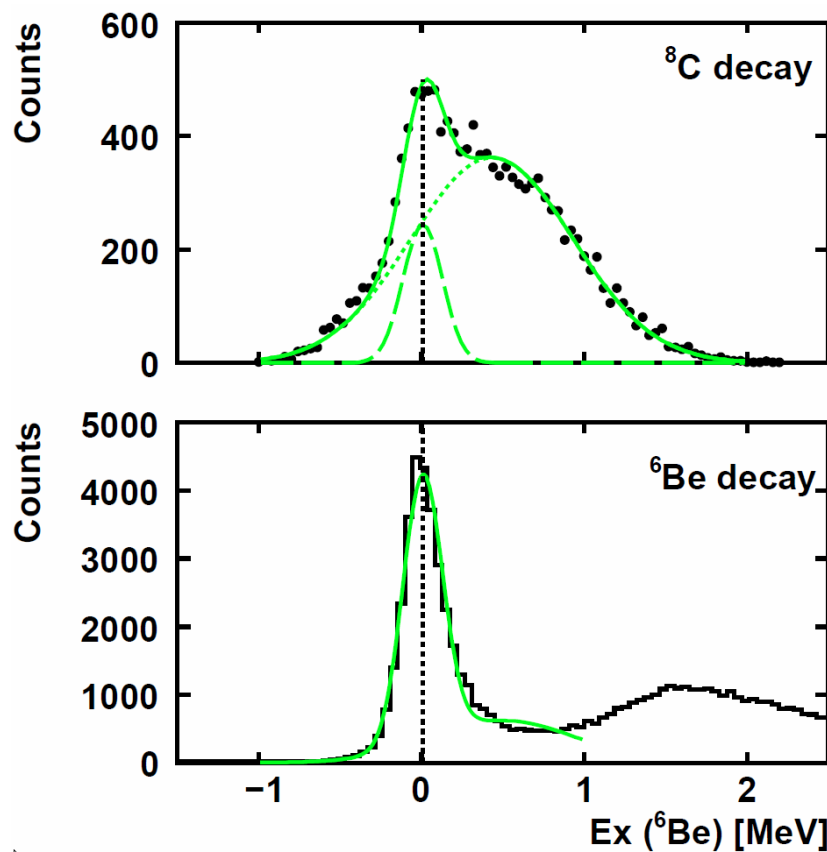
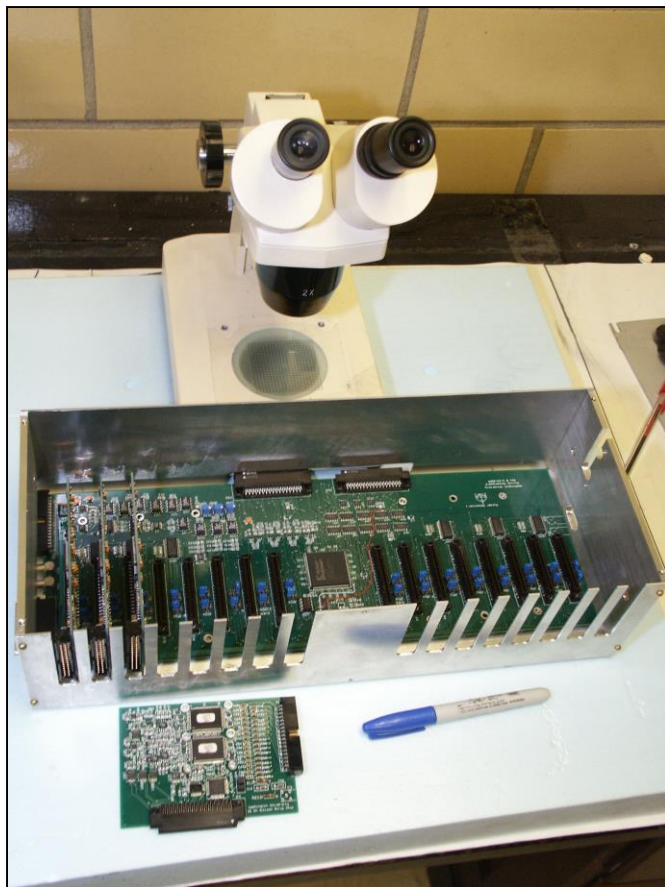


HINP16C-Rev 3 layout. The biasing and circuits used for configuring the IC as well as for readout are located in the center (“common” channel) of the chip. Eight channels lie to the left of this “common” area, and eight channels lie to the right.

The IC is 4 mm x 6.4 mm. HINP16C is packaged in a 14 x 14 mm, 128 lead thin quad flat pack. The chip’s power consumption is about 800 mW



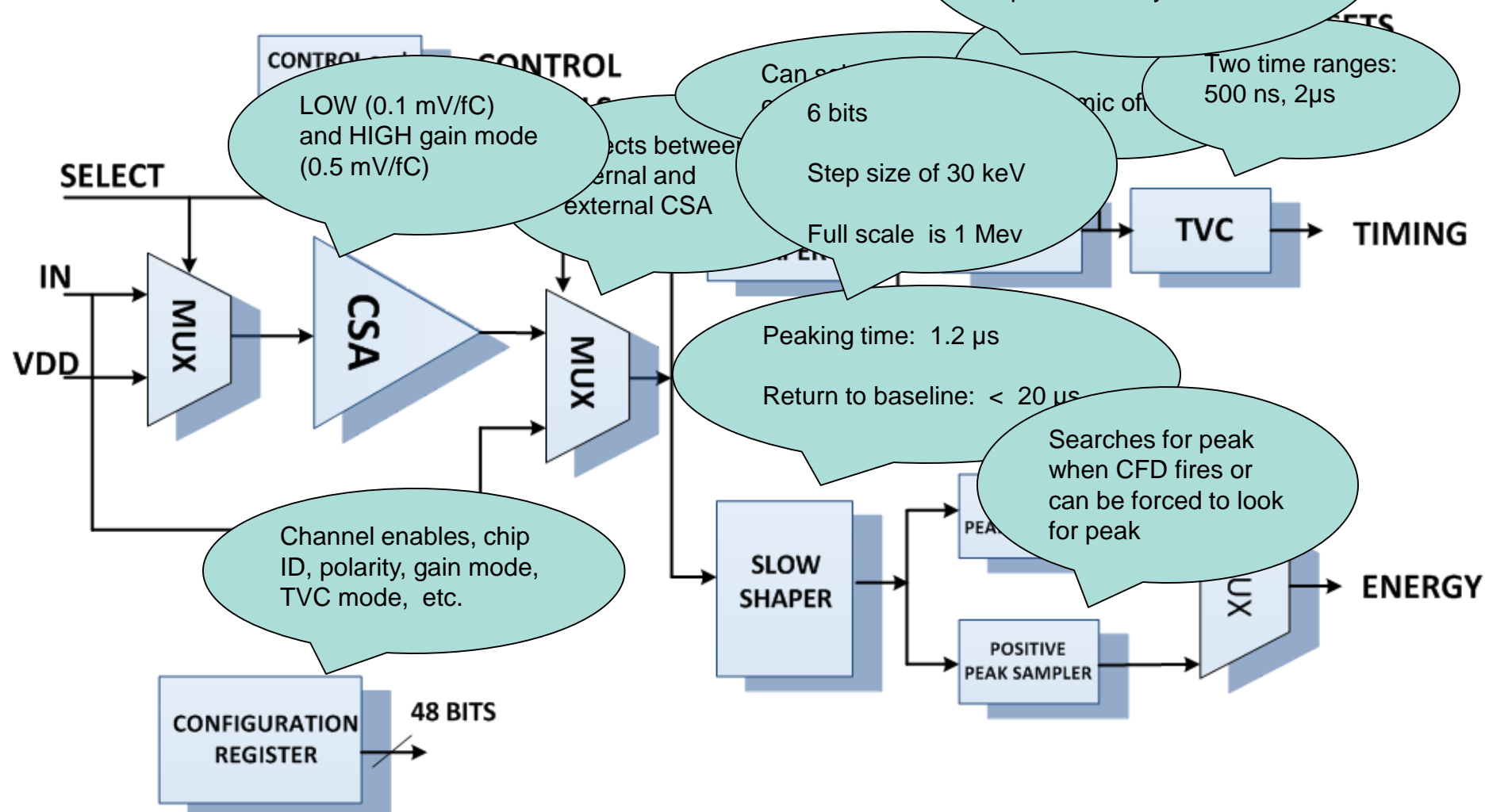
HiRA (High-Resolution Array) Detector Array at MSU  
A series of HINP16C ICs currently services the array.



Results for the study of <sup>6</sup>Be and <sup>8</sup>C. The current version of the HINP16C chip was used for a 5-particle correlation study of the decay of <sup>8</sup>C (into an alpha and 4 protons) .



# Tour of HINP16C



LOW (0.1 mV/fC) and HIGH gain mode (0.5 mV/fC)

Channel enables, chip ID, polarity, gain mode, TVC mode, etc.

CONFIGURATION REGISTER 48 BITS

Switches between internal and external CSA

Can set resolution to 6 bits  
Step size of 30 keV  
Full scale is 1 MeV

Peaking time: 1.2 μs  
Return to baseline: < 20 μs

Searches for peak when CFD fires or can be forced to look for peak

If event is not selected for read-out, the channel resets itself after user specified delay

Two time ranges: 500 ns, 2 μs

# HINP16C Performance

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Parameters

Value

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Energy Branch:

Resolution at 75 pF	28 keV
Linear range in LOW gain mode	500 MeV
Linear range in HIGH gain mode	100 MeV
CSA gain in LOW gain mode	0.1 mV / fC
CSA gain in HIGH gain mode	0.5mV / fC

Timing Branch:

Walk through CFD	< 1 ns over a range of 40 dB
Jitter	1 ns

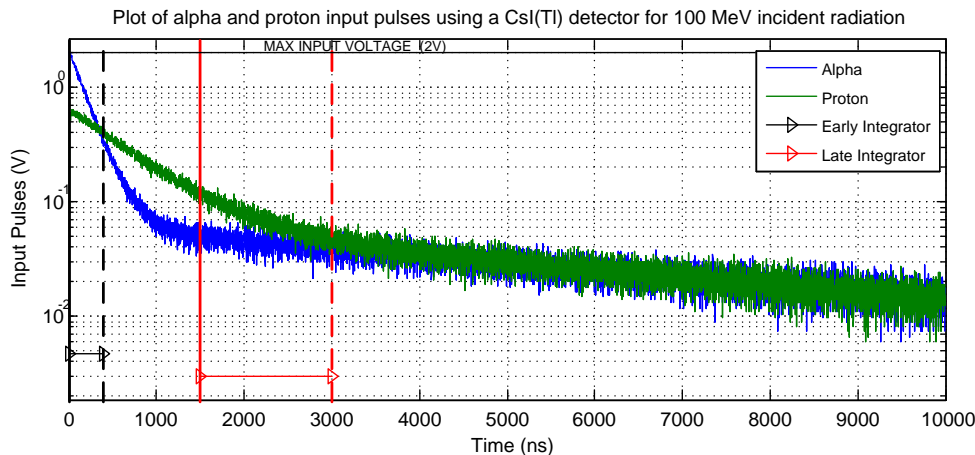
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# HINP16C Integrated Circuit

The first generation HINP16C chip is fully described in

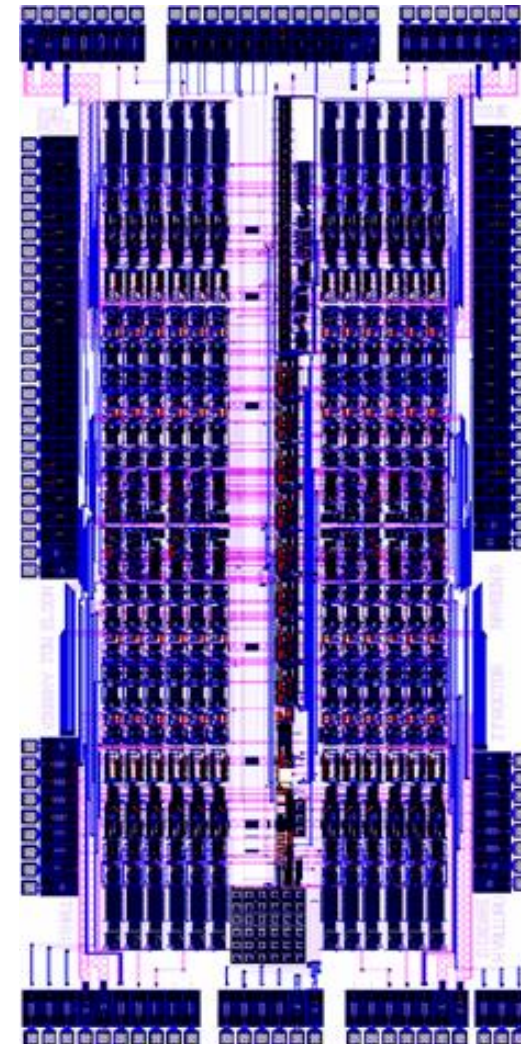
G.L. Engel, M. Sadasivam, M. Nethi, J.M. Elson, L.G. Sobotka, R.J. Charity  
(2007) A Multi-Channel Integrated Circuit for Use in Low- and Intermediate-  
Energy Nuclear Physics - HINP16C, *Nucl. Instru. Meth. A*, 573, 418-426

# PSD8C Chip

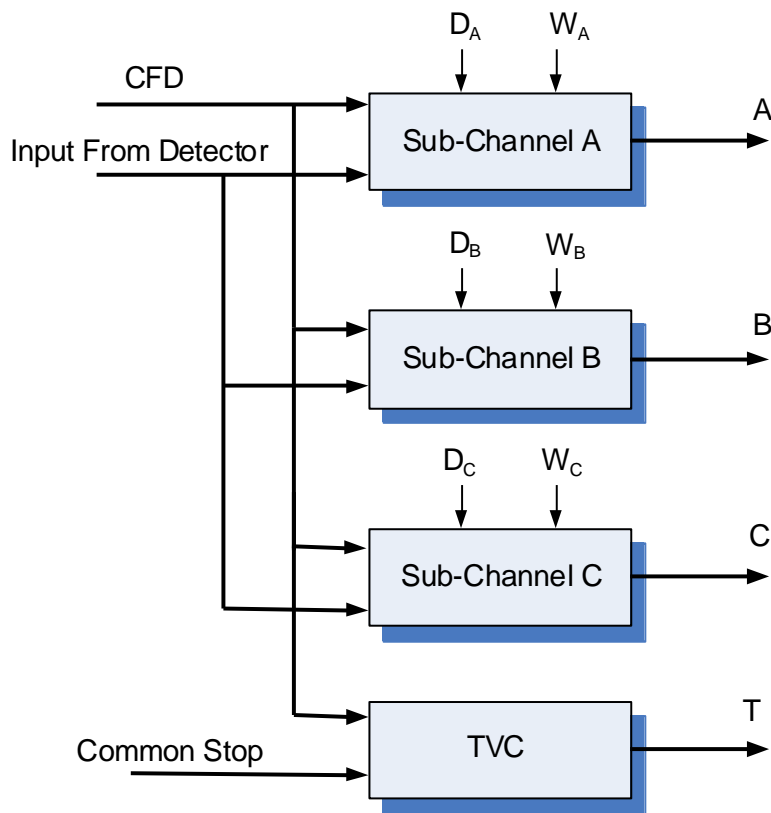


Pulse Shape Discrimination using gated integrators.

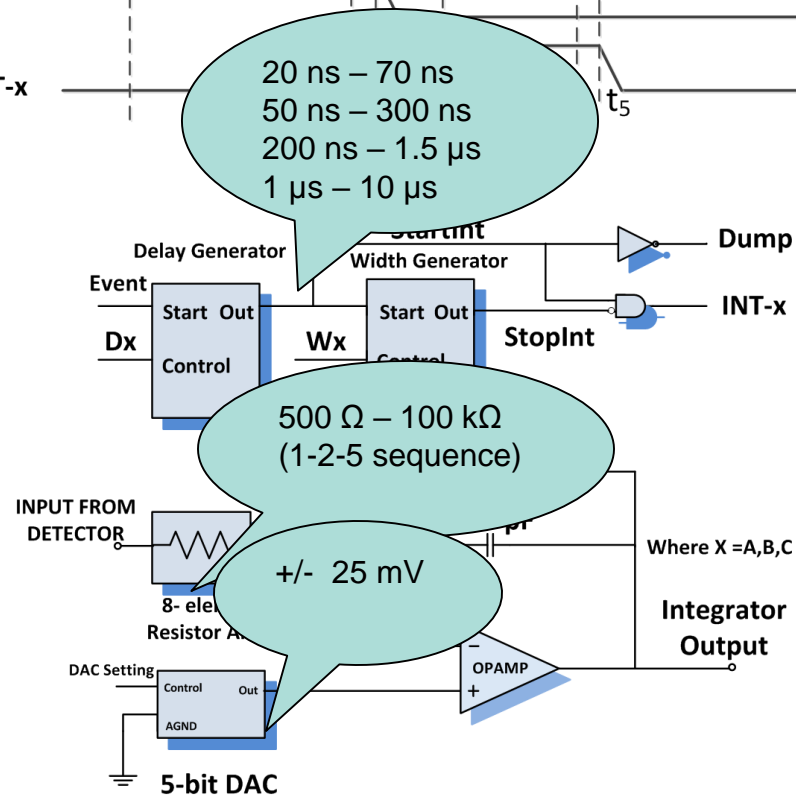
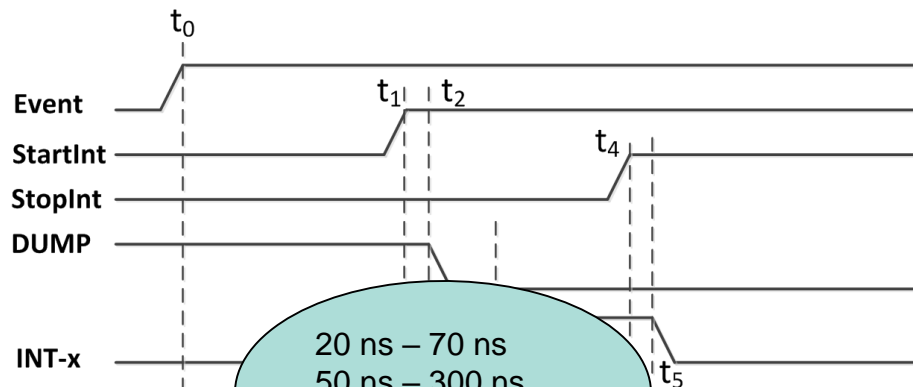
Each PSD8C channel contains 3 gated integrators.



Layout of PSD8C (Rev. 2.0). IC is 2.8 mm x 5.7 mm. PSD8C is packaged in a 14 x 14 mm, 128 lead thin quad flat pack. Power consumption is 65 mW in low-bias mode.

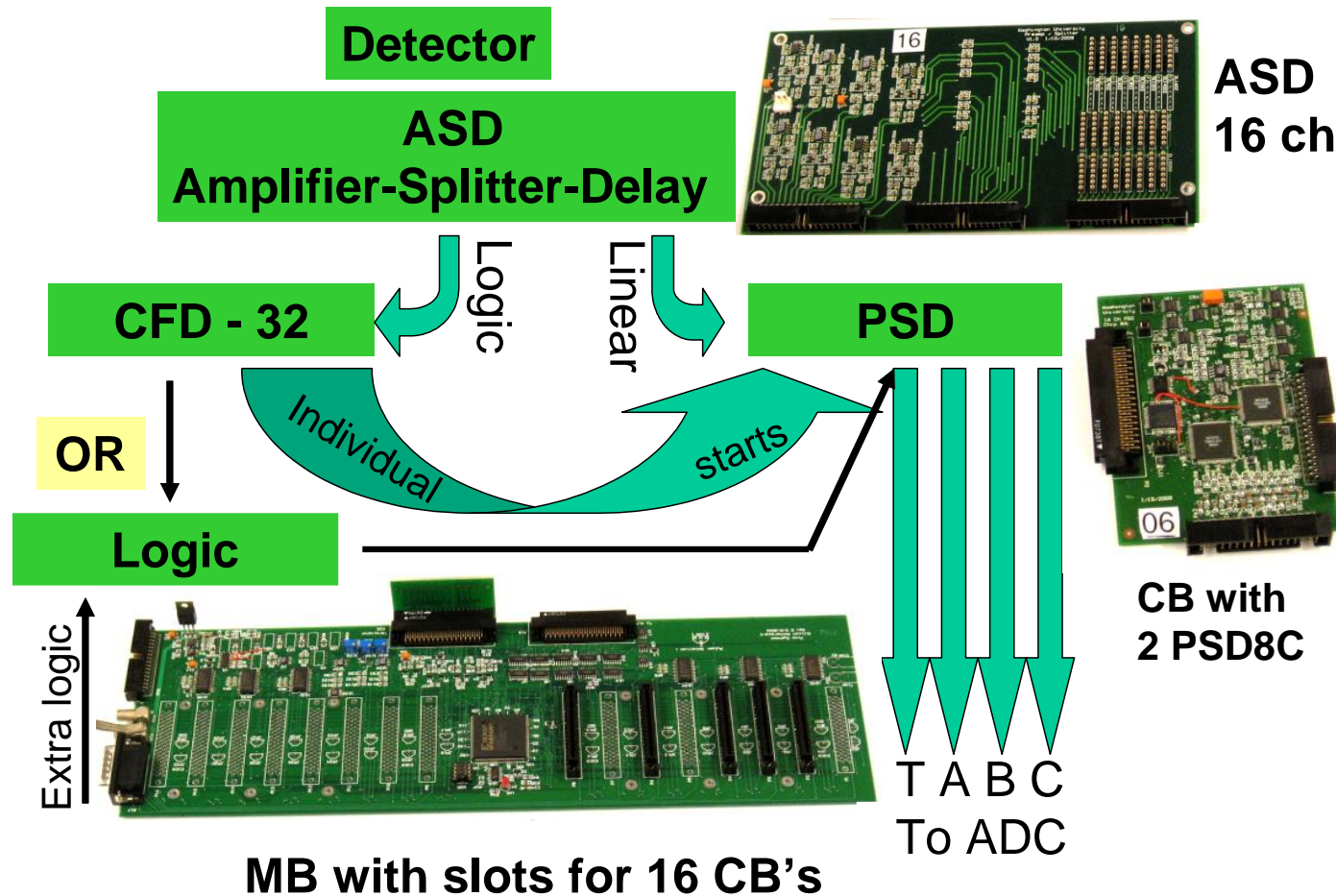


PSD8C Channel

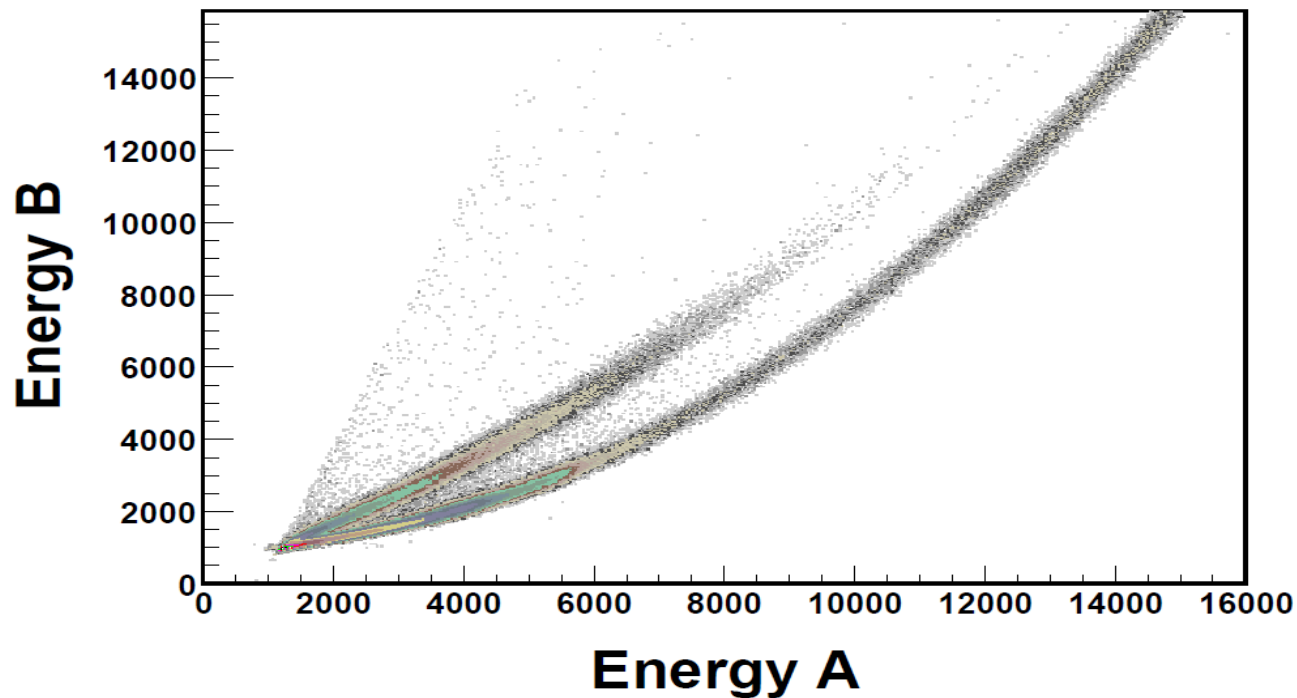


PSD8C Sub-Channel

# Pulse Shape Discrimination (PSD) System

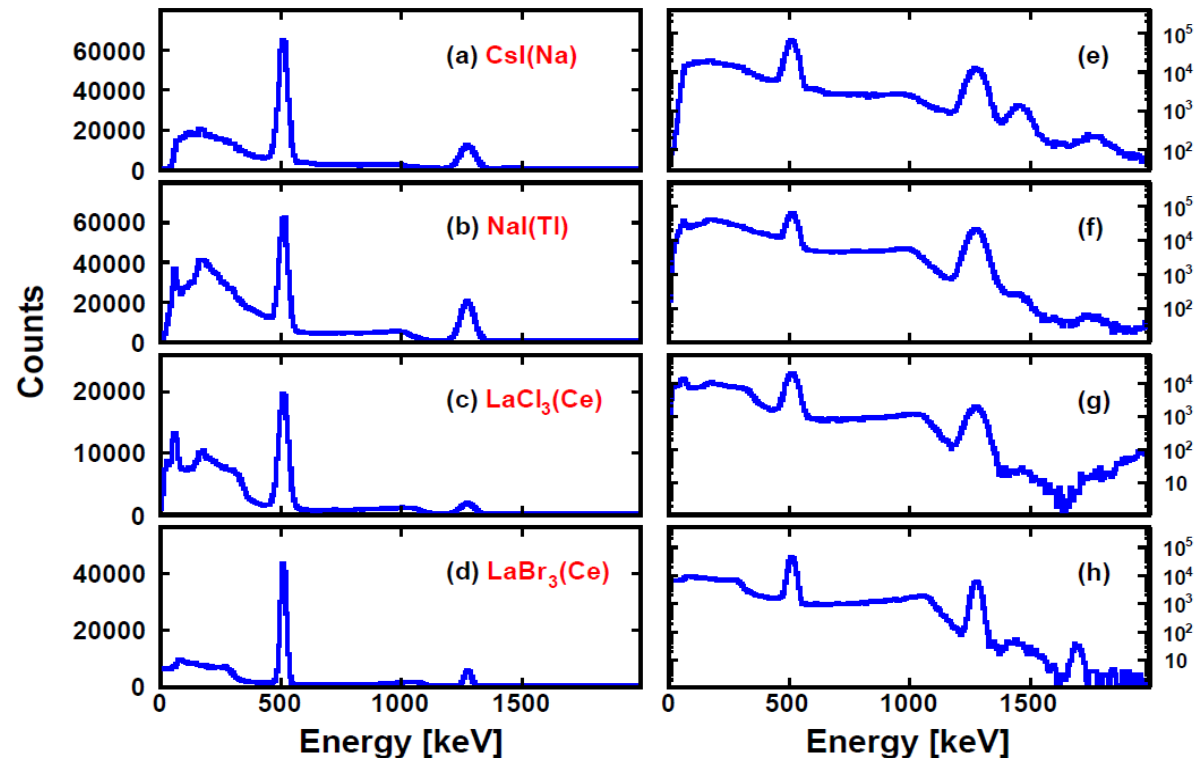


# Neutron – Gamma Ray Discrimination



PSD map taken with a BC501A liquid scintillator detector. The abscissa captures the integral with a prompt gate of 400 ns duration, while the ordinate is integral resulting from an equal length gate starting approximately 100 ns after the start of the prompt gate. The bottom locus corresponds to gamma rays while the top to neutrons. For an energy reference, the Compton edge of  $^{137}\text{Cs}$  has an abscissa channel value of 2850.

# Energy Spectra Using PSD8C



From top to bottom the spectra are from a) CsI(Na) (3"x3"x4"), b) NaI(Tl) (2" diameter x 3"), c) LaCl<sub>3</sub>(Ce) (1" dia. x 1"), and d) LaBr<sub>3</sub>(Ce) (1" dia. x 1"). Spectra are shown with both linear and logarithmic ordinates. The trigger rate for these data was approximately 1kHz and the gate widths were approximately: a) 600 ns, b) 2000 ns, c) 300 ns, and d) 125 ns. In some cases external (i.e. <sup>40</sup>K) and internal (likely  $\alpha$ -emitters) background features as well as the sum peak are observed.



# PSD8C Integrated Circuit

The PSD8C chip is fully described in

G.L. Engel, M.J. Hall, J.M. Proctor, J.M. Elson, L.G. Sobotka, R. Shane, R.J. Charity (2009) Design and Performance of a Multi-Channel, Multi-Sampling, PSD-Enabling Integrated Circuit, *Nucl. Instru. Meth. A*, 612, 161-170

# Who is using the ICs?

Nuclear Physics groups at

- Washington University (WU),
- Michigan State University (MSU),
- Indiana University (IU),
- Texas A&M University (TAMU),
- Oak Ridge National Laboratory (ORNL),
- Louisiana State University (LSU), and
- Florida State University (FSU)

are either using HINP16C or will be doing so by summer of 2010.

A group at Los Alamos National Laboratories (LANL) is helping us evaluate PSD8C performance.

# Conclusions

Since 2001, our university-based group has been working on a “toolbox” of IC circuits useful for researchers working with radioactive ion beams.

The circuits which we have designed can be composed in different ways to meet the researchers’ evolving needs and desires

To date, the group has produced two micro-chips: one analog shaped and peak sensing (HINP16C) while the other multi-sampling and PSD-enabling (PSD8C).

# Acknowledgements

- Early work on HINP16C was supported in part by an NSF MRI grant to build the High Resolution Si Array (HiRA) and the U.S. Department of Energy under Grant No. DE-FG02-87ER-40316.
- The support for the PSD8C chip development was from NSF Grant #06118996 while the implementation support came from the U. S. Department of Energy, Division of Nuclear Physics under grant # DOE-FG02-87ER-40316.
- Currently, work on PSD8C is sponsored by a grant from LANL. For the latter we are indebted to Dr. Mark Wallace.

# Questions

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