3. PROJECT DESCRIPTION

a) Research Activities

The energy density of the Nuclear Equation of state (EoS) is known to depend on both the overall nuclear density [ρ] and neutron/proton asymmetry [$\delta = (\rho_n - \rho_p)/ \rho$] and to have the general form: $E(\rho,\delta) = E(\rho,\delta=0) + S_{asy}(\rho)* \delta^2$. However, the density dependence of the asymmetry term $S(\rho)$ is poorly constrained by data. Plausible phenomenological forms for the density dependence of the asymmetry energy are shown in Fig. 1. The uncertainty is such that these plausible models predict pressures of neutron star matter (at normal nuclear densities) that vary by a factor of 6 [1]. One consequence of this uncertainly is that it is not clear if proto-neutron stars can cool by the so called direct URCA process (ν cooling via n-p equilibrium interconversion without a third body to aid in momentum conservation.)

Constraints on the density dependence of the asymmetry energy can come from: 1) measuring the root mean square radius R_n^{rms} in ^{208}Pb [see 2], 2) astrophysical measurements, like the "Shapiro delay" [3] which provides an opportunity to determine the masses of the individual neutron stars in a nearby binary [1,4], or 3) heavy-ion (HI) reaction experiments. There is a proposal to measure R_n^{rms} at Jefferson lab using parity violating e^- scattering. This difficult experiment, if successful, would provide information on the derivative of $S(\rho)$ near saturation. The second approach provides a more global constraint, but we have to be rather lucky to get the appropriate data. Our group is involved in the third approach, which suffers from the requirement that the EoS must be inferred within the framework of dynamical nuclear reaction models. Information from at least two of these approaches will be needed to fix the dependence of $S(\rho)$.

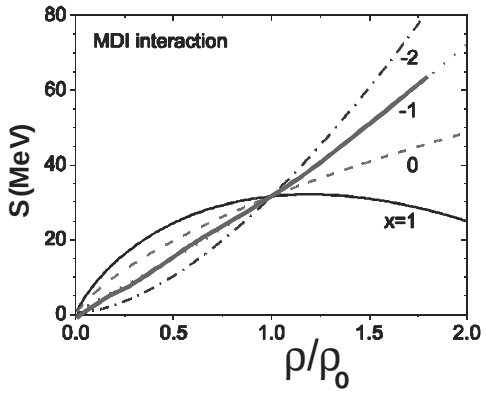

Fig. 1: Plausible phenomenological models for the density dependence of the asymmetry term in the nuclear equation of state. Presently the favored model is the near-linear dependence represented by the (bold green) curve labeled by -1. For details see Bao-An Li et al. [5].

There are several observables in heavy-ion reactions which are sensitive to the density dependence of the asymmetry term. One is the difference in the (directed) flow between neutrons and protons. This difference arises from the fact that flow is directed by the partial pressures of the separate species. For example, in n-rich matter, at high density with a stiff potential (x = -2 in Fig. 1), the neutron (protron) potential is highly replusive (attractive). Therefore the n (p) partial pressure is large (small) which enhances (suppresses) the n (p) flow. The flow difference (n-p) for the stiff asymmetric case is thus large. The observable is constructed in the above prescribed sense for forward (projectile-like) emission and inverts for $V_{cm} < 0$, see x = -2 line in Fig. 2.

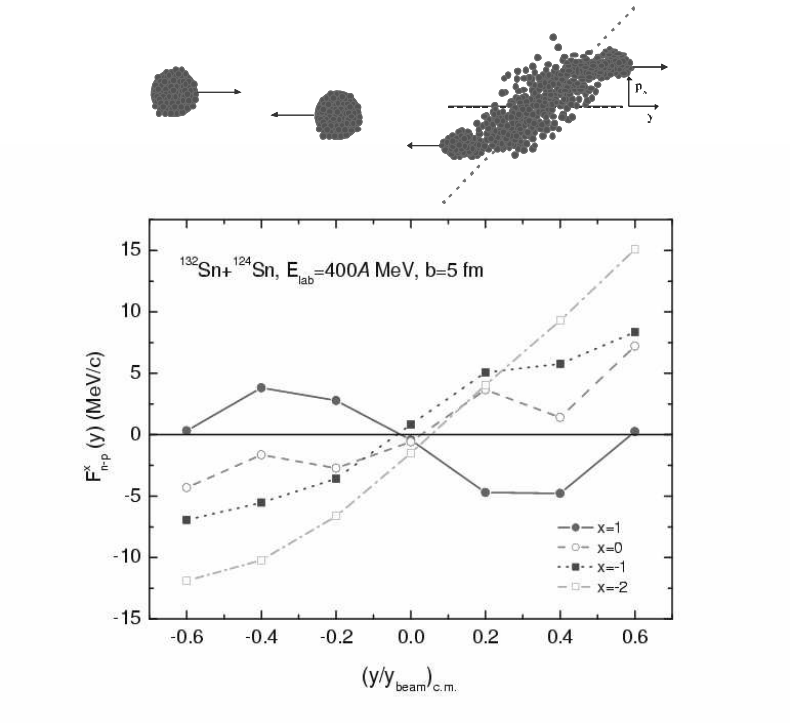

Fig. 2: This figure illustrates the logic of the whole experimental program. The different interactions (shown in Fig. 1) exhibit different flow patterns (top part of the figure) for neutrons and protons. The difference in the (directed) flow between neutrons and protons is shown in bottom portion of this figure as a function of beam rapidity (degenerate with $V_{//}$ at low energy.) This calculation is for a possible RIA experiment. (At RIA, π differential measurements will also be sought.) The whole project seeks to collect an excitation function of such data. The effort in 2007 will be at ~ 50 MeV/u where the differential effects are much smaller but still observable. This figure is adopted from the work of Bao-An Li [6].

This proposal seeks funds to allow for creation of electronics suitable for new experiments (one already approved) to attack the density dependence of the asymmetry term. We propose to fabricate a pulse-shape discrimination (PSD) CMOS chip which will allow the approved experiment (at the National Superconducting Cyclotron Laboratory NSCL -[6]) to be performed in the summer of 2007. The time between approval and execution is usually not this long at the NSCL, however this experiment (and a few other

experiments) requires the reconfiguration of a vault (S2) for neutron TOF work. This conversion will not be completed before the end of 2006.

Specifically, we propose to design, extensively simulate, and fabricate a PSD chip suitable for use with both CsI(Tl) (used for charge-particle discrimination) and liquid scintillator (used for neutron-gamma discrimination). The IC will require no active cooling. An 8-channel "prototype" chip will be submitted for fabrication within 8 months of funding being approved and a revised, 16-channel "production" version will be submitted after use of the "prototype" IC in the experiment planned for the summer of 2007. The "production" chip will address any deficiencies uncovered in the initial "prototype" and will be made available to other groups.

This rapid fabrication of the first chip can be done because 1) many of the chip features and all the chip readout functions are *similar* to our existing (HiRA [7]) chip (which has been used in 3 experiments in 2005), 2) the support system, (chip boards [CB's] mother boards [MB's], chip control system [XLM-80] and pipeline ADC [SIS-3300 or 3301] are similar or identical to those used for our existing (peak-sensing) chip and 3) the CMOS design effort is modest as the high-gain (low-noise) amplification is done off chip and some circuits from the existing IC can be re-used.

The last point is worth some amplification. While CMOS design always poses challenges, this design is rather straightforward given the extensive experience that we have gained over the past several years in the design of our existing peak-sensing IC. A PSD chip has not been made to date because the need for large scale PSD is much less common than is single pulse-height processing. The proposed technique is far more cost effective than a "gold-plated" digital signal processing (DSP) scheme, for which funds are not available, and we doubt would be superior for the intended applications.

An added benefit to the development and production of this integrated circuit is that it will compliment our existing analog chip and thus provide a ``tool-box" from which both (single) peak sensing and (single or multiple) charge integration(s) within a common platform and readout scheme can be done.

Our approved experiment (see Fig. 3) will use the ~ 200 CsI(Tl) scintillators of the MINIBALL [9], the MSU neutron walls [10] (100 channels), and another 50 (approximately) discrete neutron detectors [11], all of which require PSD analysis. An additional 100 element forward array also must be instrumented with QDC's and TDC's. All of these detector systems could be serviced by the proposed technology. Beyond this, our recently completed HiRA array, with over 1000 Si channels, will be used for high resolution charged-particle detection. Our HINP16c will service these Si channels.

The CsI(Tl) detectors at backward angles are used to determine the reaction plane. The flow for neutrons and charged particles come from the n detectors and HiRaA, respectively. The forward array, of fast scintillators provides a high quality event time (triggered by protons) needed for the n time of flight. We will not discuss the forward array in this proposal. Despite the fact that such detectors do not contain significant PSD

information, we intend (for convenience) to process the signals from this array by the proposed electronics.

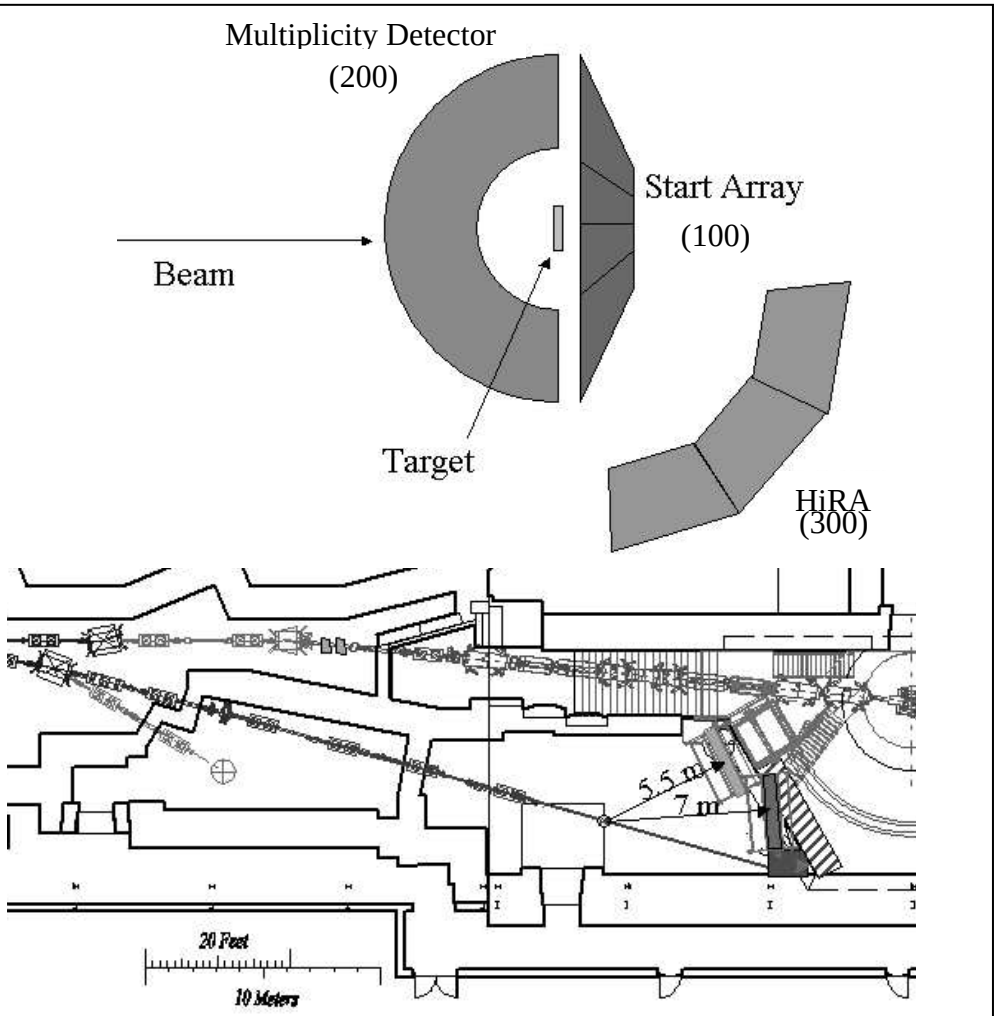

Fig. 3: (Top) Schematic of 2007 experiment and (bottom) new NSCL S2 vault layout. The neutron walls are shown in the vault layout with the 5.5 and 7.0 m flight paths.

We had originally proposed the experiment using the Washington University μ-ball [12] as we had done in our first experiment in this project [13]. However, the analysis of these data showed that this device to be both insufficiently granular and too thin. Much of the original electronics for the MINIBALL no longer functions and can not be repaired (LeCroy units). The approved experiment could be done with conventional (off-the-shelf) electronics, *i.e.*, individually gated CAEN QDC's. The "off the shelf" digitizer cost would be in excess of 100k$ (in excess of 150k$ if one counts the crates and interconnections.) This proposal offers, at a roughly similar (one-time) cost, to create a new and flexible technology, that can be used by us or by others who need many channels of PSD, with a very modest expenditure. This might allow programs to proceed

which could not, under the present budget climate, and to do so with dedicated electronics.

It is perhaps also useful to keep in mind the funds presently spent for digitizers based on a detector per digitizer logic (rather than in the pipeline scheme we employ.) For reference, the cost in just QDC's and TDC's of just one recent project at the NSCL (MoNA) was 80k$. In addition, and the annual expenditures, at this one laboratory, for the equipment pool for conventional digitizers is approximately 20k$. The present proposal would largely alleviate the needs for future purchases of this sort (as well as the crates to power these low-density ADC per detector channel systems.)

The requested funds over the course of two years will produce a "prototype" chip, a "production chip", the auxiliary support boards, equipment needed to bring up a complete ``remote" test station at Western Michigan University, and support for both graduate and undergraduate students. Funds are also requested to provide course release time and summer salary for the PI who will oversee the students that will assist him in the design of the integrated circuit.

b) Description of Research

Our design makes use of CMOS technology to provide a) integration of several regions of the analog signal, b) provide time-to-amplitude conversion and c) prepare each of the above as pulse streams for a pipeline VME ADC.

Detector outputs will be split for logic and linear branches. Timing signals would be generated by leading-edge or constant-fraction-discriminators. We plan to use VME CFD's for the upcoming experiment but specialty timing chips, such as the TA chip from Ideas ASA, could ultimately be used. The individual timing signals and delayed linear signals would be sent to the CMOS chip.

The proposed pulse-shape discrimination scheme with a 16-channel chip is illustrated in Fig. 4. The individual CFD logic signals ANDed with a global enable signal provide channel enables. For each linear signal (accompanied by its logic), three different integrations (called **A, B** and **C**) would be performed with start times referenced to the individual discriminators. In addition, an amplitude **T** will be produced proportional to the difference between the individual discriminator and an external common stop reference. (The **T** amplitude eliminates the need for conventional VME TDC's.)

The delays in the integrators starting times (D_A, D_B, D_C) and the widths (W_A, W_B, W_C) of the integration windows are controlled by the user on a chip-by-chip basis. In Fig. 4, the delays D_A, D_B, D_C are voltages that are converted to times on-chip as are the widths W_A, W_B, W_C.

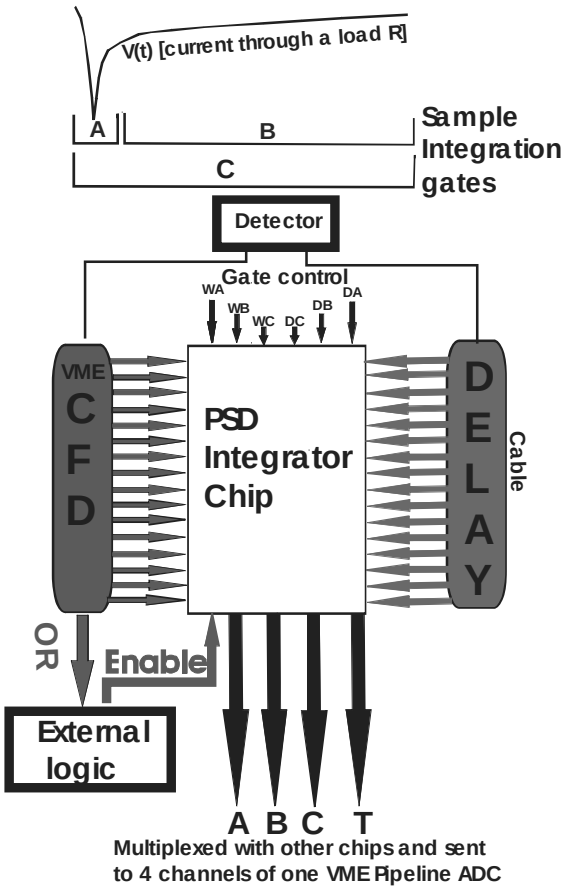

Fig. 4: Overview of analog pulse-shape discrimination scheme integration. The new chip is the center box.

Each channel, pictured in Fig. 5, in the multi-channel IC is composed of three sub-channels and a time-to-voltage converter (TVC). The sub-channels produce the three different integrations (**A, B** and **C**), and the TVC will produce the amplitude **T** that will be proportional to the difference in time between the channel's discriminator firing and an external common stop reference.

The sub-channels are not identical, in the sense that each sub-channel will support a different range of delays and integration widths. For example, the A sub-channels may support delays and integration widths of tens to hundreds of nanoseconds while the C sub-channels would support delays and integration widths of microseconds. The best range of delay values and integration widths for the three sub-channels is still under investigation.

Aside from the user controlled delay and widow widths, the feature that allows this chip to be used with detectors as diverse as liquid scintillators (fast) and CsI (slow) is a bank of resistors (for each sub-channel) which determine the charging rates of the integrating capacitors. The architecture of a typical sub-channel is depicted in Fig. 6. The figure is included as an aid to the reader in understanding the proposed design, and details of the implementation have been omitted to retain clarity.

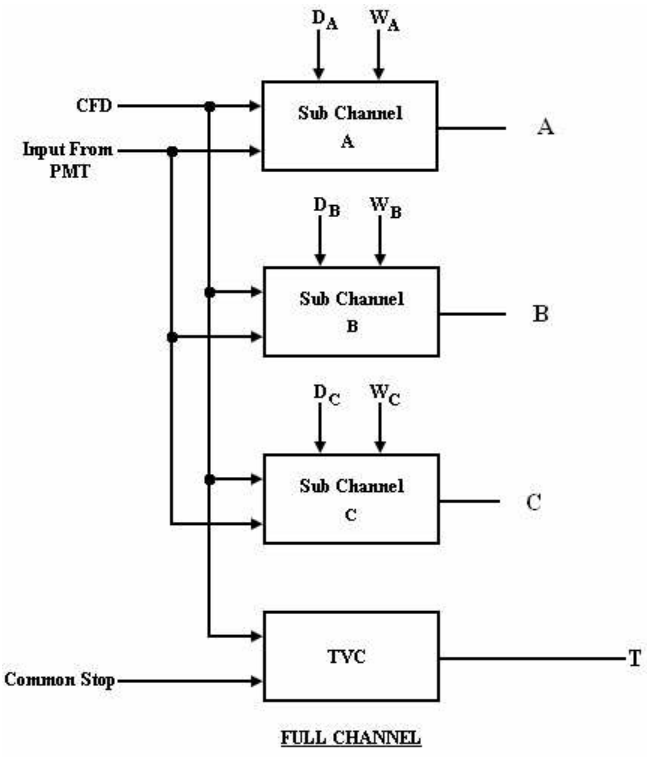

Fig. 5: Architecture of a single channel composed of three sub-channels and time-to-voltage converter

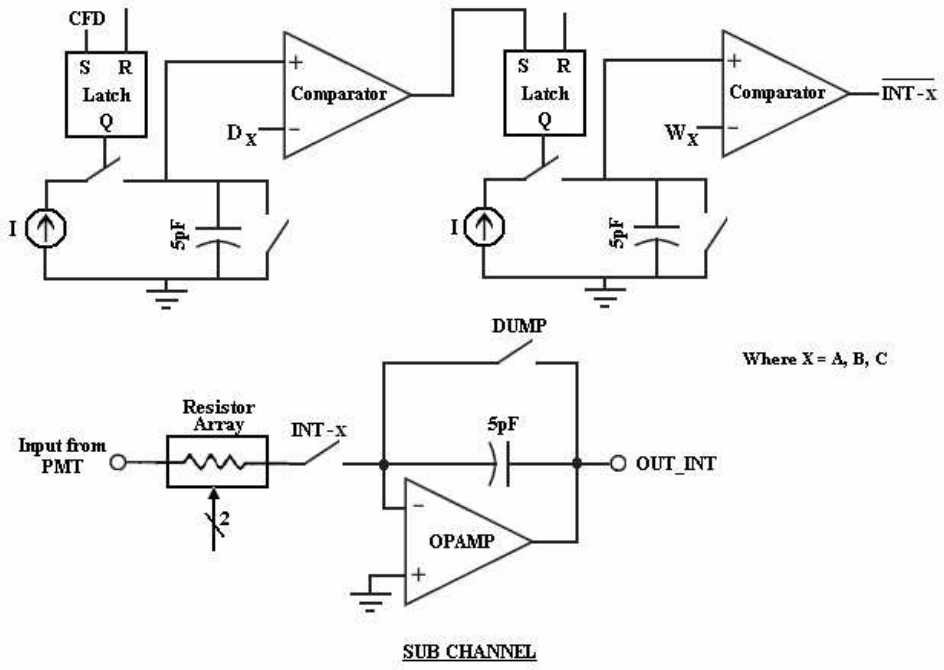

Fig 6: A sub-channel contains an integrator with programmable charging rate and circuitry to control start of and duration of integration period.

The programmable resistor array will support four different charging rates. One of the major goals of the design effort is to ensure that the integrator output is not corrupted due to charge injection (the dumping of charge onto capacitors when CMOS switches are opened.) Well-established techniques (half-size dummy switches, pseudo-differential topologies – not illustrated, *etc.*) for dealing with charge injection will be employed to ensure high performance.

The sub-channel of Figure 6 would operate as follows. Initially, the integration capacitor would be discharged (DUMP signal active). The firing of the channel's CFD starts the time-to-amplitude converter (TAC) on the left side of the figure. The constant current source charges the capacitor, producing a voltage linearly proportional to time. When the voltage equals the externally applied control voltage D_x (where x = **A**, **B**, or **C)**, the comparator will fire and start a second TAC. The value of the charging current (or the TAC capacitor value) will be different for each of the three sub-channels in keeping with our desire to have the three sub-channels possess different ranges of delay and integration width.

When this second TAC (shown on right of Fig. 6) starts, the DUMP signal would be de-asserted thereby starting the integration. The integration period will end when the output voltage of this second TAC equals the voltage, W_x, which determines the *width* of the integration period for the sub-channel. The switch controlled by the signal INT_x would in turn open, disconnecting the charging resistor and forcing the integrator to "hold" its output voltage until it could be sampled. After the output voltage is read by the off-chip ADC, both TACs would be reset and the capacitor voltage dumped.

In reality, producing a high-performance TAC, for example, is not nearly as simple as the above discussion might suggest. The interested reader should consult our website (http://www.ee.siue.edu/~gengel/HINP.htm) (which describes our existing peak-sensing chip - HINP16C) for details of implementation. Here is a good example of where we will be able to re-use modules developed over several years for our existing IC (and which are known to perform well) in the proposed PSD chip. Some tweaking of capacitor values and/or current levels might be needed, but the proven circuit techniques and topologies can and will be used. The bandgap reference, the comparator, *etc.* are other examples of where we can re-use designs from our existing IC.

In many cases, existing physical layout will also be re-used. This is possible because we will employ the same technology *i.e*. the AMIS 0.5 micron NWELL process available through MOSIS (MOS Implementation Service). The process supports double-poly capacitors and high-valued resistors (1 kΩ/square). We plan to re-use existing layouts, as well, for the digital circuits used in configuring the IC and for the readout electronics.

The simulated responses of the chip (a) liquid scintillator (gamma - red, neutron – blue) and (b) CsI (proton – red, alpha – blue) is shown in Fig. 7. These crude simulations are at the symbolic math level and make use of average (noiseless) signals deduced from devices built by the Washington University group ([11] for liquid and [14] for CsI(Tl) scintillators.) In these simulations only the **A** and **B** sub-channels were needed to clearly

distinguish the waveforms (modeled by sums of exponential functions with parameters determined from the real devices cited above.)

Different charging rates, *i.e.* resistor values, were used for the **A** and **B** integrators to match the integrator outputs to the ADC range. On the chip boards (CB's) a differential amplifier (with jumper selectable gains) would be supplied separately for the **A**, **B**, **C**, and **T** outputs to provide additional gain matching capabilities.

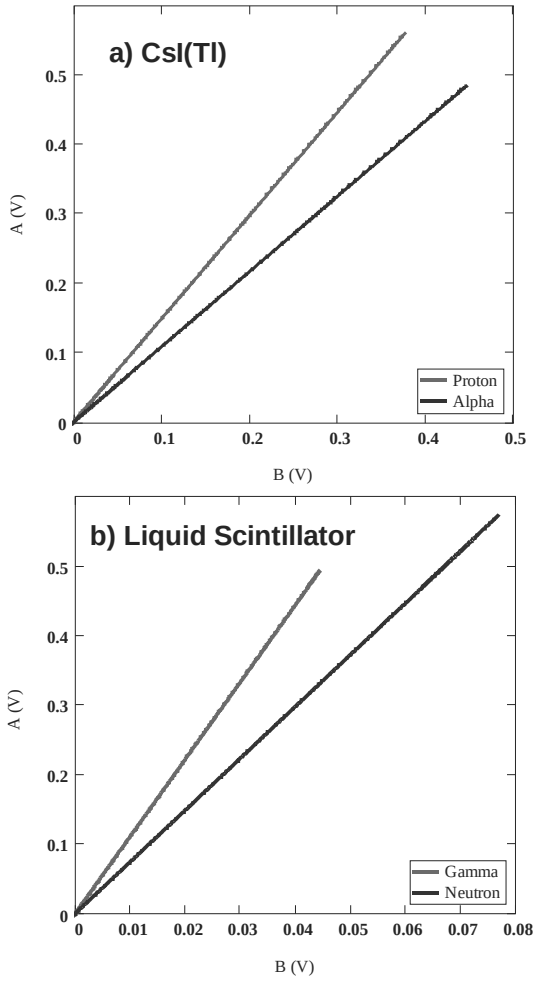

Fig. 7: Pulse-shape discrimination plots (integrations in two different regions plotted against one another) as a function of deposited energy. (The energies increase going up the curves.) These plots are for: (a) CsI(Tl) (proton – red, alpha – blue) and (b) liquid scintillator (gamma - red, neutron – blue) . The B voltage (delayed gate) for the liquid scintillator would be differentially amplified off chip before digitization. These simulations model the time dependent detector outputs as the sums of exponentials with particle dependent but energy independent parameters. The locus for α-particles would become non-linear if an energy dependence were included in one of the exponentials. (This improvement is an undergraduate project at WU.)

In summary, experiments both approved and planned require large-scale application of PSD. While in principle this could be done, on one hand with conventional electronics or, on the other, with digital signal processing, neither of these options are competitive with the proposed scheme. Each of the alternatives requires either: far more manpower, development time, or money. Only two VME slots (one for Chip control with the XLM-80 and one for an 8 channel pipeline SIS ADC) is all that is required to read in the two completely different large-scale arrays needed for charged-particle (CsI) and n detection (liquid scintillator). These two systems would each use 4 channels of a single commercial 8-channel VME ADC.

c) Impact

Funding of this proposal would allow the EoS research to move forward in a resource efficient fashion. It would not only allow us to proceed with minimal resources but to allow modest expansion costs and minimal impact on facility resources. Furthermore we would create a technology that others could use. The proposal seeks to ensure the latter by generating the "production" chip with the standing design team after experience is gained with the prototype.

Very few university based groups are engaged in analog or mixed-signal analog-intensive design for physics applications. The marriage of such an effort to the basic science efforts embraced generally by the NRC strategic plan for "Physics of the Universe" and specifically by the low energy Nuclear Physics community is highly desirable.

In the course of the two years covered by this proposal, not only will the PSD IC be designed and tested, but potential users will become familiar with this technology by: a) presentations at meetings, b) demonstrations of the technology at SIUE-WU, c) interaction via open SKYPE sessions and ultimately d) use of one of a few test stations built in the second year.

The SIUE and WU groups have met almost every week at Washington University for the past few years. (At critical design times, the SIUE site is used.) Recently Prof. Mike Famiano (WMU), who wrote much of the FPGA control for our last chip, has joined us via SKYPE. If this proposal is approved, monthly open meetings would be held at which interested users would 1) get a student prepared powerpoint talk via email and 2) could participate in the SKYPE meeting if they choose. This would allow the interested community to keep in touch at virtually no cost. These meetings could also serve to address problems from the users of our previous chip - HINP16C.

The funds requested for VME equipment for WMU are to ensure that the entire system is robust and can be brought up without the immediate presence of one of the designers.

This project will be used to train several graduate students in mixed-signal (CMOS) design. (The HINP16C project produced three high-quality Masters Theses.) We expect that the proposed PSD chip project will produce two Masters Theses as well as providing projects to undergraduates at both SIUE and WU to work on advanced technology useful for physics experiments.

While SIUE is a non-granting Ph.D. institution, we encourage students who earn Masters Degrees at SIUE to continue as doctoral students at WU. This is not only beneficial to the students involved, but it creates a mechanism that can guarantee continuity in our design efforts and thus help ensure that analog-based IC expertise, useful for physics applications, expands.

On the undergraduate level, our goal is to have two ECE and two Physics students working as a team. The ECE students (from SIUE) would help in the design effort, write the FPGA chip control programs, and would also participate in the ultimate chip testing. The physics students (from WU and WMU) would do the actual chip testing, work with the ECE students in FPGA debugging, and would also be engaged in the design effort from the beginning. Over the past few years we have become acutely aware that students from these two somewhat closely related disciplines have different perspectives and use different language to describe the same reality. Learning how to communicate effectively with one another is very valuable and only comes with practice. The undergraduates would follow the development of the proposed IC and be engaged, side-by-side, in observing (and helping out where they can) the design, simulation, and testing of the prototype chips. They will also serve to help document the development process. Co-authorship of undergraduates (both from ECE and physics) is guaranteed in both engineering and physics journals.

Two of the anticipated 4 undergraduate students have already been identified. (James Brown, a minority ECE major, and Kevin Mercurio, a physics major.) Both are highly talented, interested in pursuing this interfacial project, and intend to pursue advanced degrees in engineering physics or basic physics research. We anticipate two more undergraduate students joining the effort. They will be selected from Professor Engel's spring (present term) digital design class and Sobotka's spring nuclear science course.

SIUE is a member of ILSAMP (Illinois Louis Stokes Alliance for Minority Participation). ILSAMP is a consortium of 17 area community colleges, universities and research organizations participating in a collaborative effort to provide programs to improve the quality of science, mathematics, engineering, technology and science education (SMET) for underrepresented minority students. The goal of the program is to significantly increase the number of undergraduate and graduate degrees awarded to underrepresented minority students in SMET disciplines.

As part of SIUE's involvement in ILSAMP, each year undergraduates from SIUE participate in the *Argonne Symposium of Undergraduates in Science, Engineering, and Mathematics*. If involved in this project, SIUE would provide support for the PI and Mr. Brown to attend the symposium to report progress on the project.

d) Management Plan

We need to keep the community informed about our progress and solicit input from potential users. This will be accomplished through meetings in St. Louis and elsewhere as well as SKYPE sessions. It is important that Prof. Engel interact with experimentalists in addition to those at WU. The more experimentalists who understand what can, and cannot, be done with this technology the better. Funds to allow Prof. Engel and selected students to attend the RIA workshops are requested.

The face-to-face meetings (as well as the SKYPE interactions) are ways to ensure the broadest possible involvement and to help prevent "Group-Think" by the designers or for that matter users. Three rigorous design reviews are planned. All interested parties will be invited to participate in these reviews.

During the first few months of the project the EE graduate students will fully specify the various circuits, perform high-level simulation to verify the specification, and create VerilogA models of the complete IC and all of its sub-systems. These include the bias circuits, operational amplifiers, the integrators, the time-to-amplitude converter, and the readout electronics. In general, several VerilogA models will be created for each of the modules with differing amounts of detail (for example, a "noiseless" and "noisy" model of the integrator). We know that extensive VerilogA modeling was critical to the success of our HINP16C IC. Simulations at an even higher level of abstraction will be performed using MATLAB. Undergraduates involved in the project will help the graduate students complete these tasks. The PI will oversee this effort. After the complete IC is modeled at the behavioral level, a design review will be conducted before proceeding on to implementation at the electrical level.

The design of a large analog-intensive system with a significant mixed-mode component is not simple. We will use Cadence IC design software as we did for the HINP16C design. Students affiliated with the VLSI Design Research Laboratory at SIUE are familiar with all aspects of the software. We have extensive experience with Virtuoso (schematic and layout editor), SpectreVerilog (simulator), and with the OCEAN/SKILL scripting language. The PI, with student assistance, will perform the detailed circuit design. Students will help by running simulations across process corners and a wide temperature range. Special attention will be paid to the temperature sensitivity of the various subsystems. All necessary time domain, frequency domain, noise, and Monte Carlo simulations will be performed and *carefully* documented. Another design review will be conducted at this time before proceeding on to physical layout.

After correct operation is verified through simulation at the electrical level, physical layout will take place. Post-layout simulations on the extracted layout will be performed. A third and final, comprehensive design review will take place before submitting the IC for fabrication. We anticipate that our 8-channel "prototype" system will be submitted for fabrication in early March 2007 so that it will arrive back from the fabricators in May 2007 and can be integrated into a system for use in experiments later in the summer of 2007.

Students working on the project during the first part of the second year of the grant would be more deeply involved in the testing of the ICs and in the design, construction, and testing of the prototype systems. They will also develop the FPGA control required by the data acquisition system. Undergraduate and graduate students will work together on the FPGA design.

While we anticipate the 8-channel "prototype" chip will provide acceptable performance when used in the experiments during summer 2007, we will apply what we learn from this initial use of the IC to improve its performance and expand to 16 channels. This 16-channel so-called "production" version of the PSD chip will be submitted in January 2008 and should be back from fabrication by April 2008. It is our intention to allow the "prototype" and "production" chips to be used interchangeably on system mother boards.

The final months of the project will be devoted to assembling a small number of systems, distributing the systems, training users of the system, completing documentation of the IC, and evaluating the overall success of the project.

The specific time-line for the development of the proposed IC is provided in Table 1.

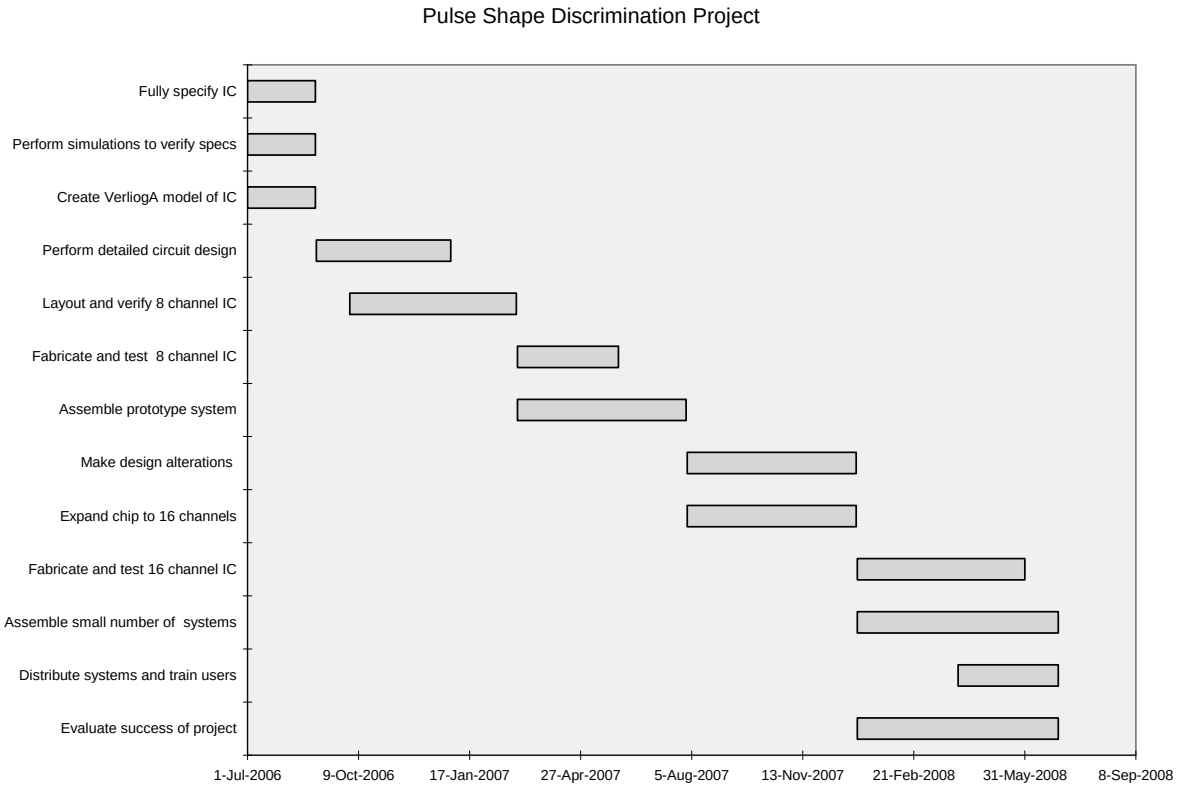

Table1: Schedule for major components of PSD IC project.