Annual Report for Period: 09/2007 - 08/2008
Submitted on: 08/21/2008
Principal Investigator: Engel, George L.
Award ID: 0618996
Organization: Southern Ill U Edwardsvill
Submitted By:
Engel, George - Principal Investigator
Title:
Development of a Pulse Shape Discrimination CMOS ASIC

Project Participants

Senior Personnel

Name: Engel, George
Worked for more than 160 Hours: Yes
Contribution to Project:
Dr. Engel supervises the development of the ASIC under development for this NSF project.

Name: Sobotka, Lee
Worked for more than 160 Hours: Yes
Contribution to Project:
Dr. Sobotka leads the Washington University nuclear physics group that is helping specify how the ASIC under development should operate.

Name: Famiano, Michael
Worked for more than 160 Hours: Yes
Contribution to Project:
Dr. Famiano will use the ASIC, currently under development, in an upcoming experiment.

Post-doc

Graduate Student

Name: Hall, Michael
Worked for more than 160 Hours: Yes
Contribution to Project:
Michael Hall has worked as a graduate research assistant since the start of the project (Sept. 2006). Mike has been one the principal designers of the integrated circuit under development. Mike will defend his thesis on the topic (December 2007). Mike's support for the past year has come directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $920. Mike completed his thesis and graduated in December. Mike is now a doctoral student in the Computer Science and Engineering Department at Washington University in Saint Louis. We have a proposal into NSF and hope Mike will continue to be involved in the project working under the new NSF grant.

Name: Proctor, Justin
Worked for more than 160 Hours: Yes
Contribution to Project:
Justin Proctor has worked as a graduate research assistant since the start of the project (Sept. 2006). Justin has been one the principal designers of the integrated circuit under development. Justin will defend his thesis on the topic (December 2007). Justin's support for the past year has come directly from the NSF grant.The support consists of tuition remission and a monthly stipend of $920.

Justin graduated in December and is now working for a company here in the St. Louis area.

Name: Valluri, Nagendra
Worked for more than 160 Hours: Yes
Contribution to Project:

Nagendra (Hari)Valluri has worked on the project as a graduate research assistant since June 1, 2007. Hari is responsible for the physical layout of the digital circuits used in the integrated circuit currently under development for the this NSF project. Hari's support lastsummer came directly from the NSF grant. Hari will continue to work on the project until August 2008 when he will complete his thesis work. The support consists of tuition remission and a monthly stipend of $920.

Name: Dasari, Dinesh

Worked for more than 160 Hours: Yes

Contribution to Project:

Dinesh Dasari has worked on the project as a graduate research assistant since May 15, 2007. Dinesh is responsible for the physical layout of the analog circuits used in the integrated circuit under development for the this NSF project. Dinesh's support last summer came from state of IL matching funds ($10,000) that the university awarded me to be used on the project. Dinesh will continue to work on the project until Summer 2008. The support consists of tuition remission and a monthly stipend of $920.

Name: Ngyuen, Nam

Worked for more than 160 Hours: Yes

Contribution to Project:

Nam Ngyuen has worked as a graduate research assistant on this project since January 2008. Nam was a quarter-time graduate assistant (10 hours/week) from January 2008 until May 2008. Beginning this summer he has been made a half-time assistant (20 hours/week). Nam is designing a I2C interface for the custom integrated circuit under development. Nam plans to write a thesis on his work and graduate in December 2008. Nam is replacing another graduate student who will graduate this summer. Nam's support comes directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $460 while he was quarter-time and $920 now that he is half-time.

Name: Yelchuri, Naga

Worked for more than 160 Hours: Yes

Contribution to Project:

Naga Yelchuri has worked as a graduate research assistant on this project since June 9, 2008. He is a half-time assistant (20 hours/week). Naga is replacing another student currently working on the project who will graduate this summer. Naga plans to write a thesis on his work and graduate in May 2009. Naga's support comes directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $920.

Name: Reddy, Sruthi

Worked for more than 160 Hours: Yes

Contribution to Project:

Sruthi Laxma Reddy has worked as a graduate research assistant on this project since May 15, 2008. She is a half-time assistant (20 hours/week). She is only working on the project this summer (2008). She assists the PI in maintaining the CAD tools and the UNIX boxes that we use in the project. She is also helping train students use the IC design tools. Sruthi's support comes directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $920.

Name: Paul Antony, Arokia

Worked for more than 160 Hours: Yes

Contribution to Project:

Arokia has worked as a graduate research assistant on this project since May 15, 2008. He is a half-time assistant (20 hours/week). He is only working on the project this summer. He assists the PI in accomplishing many miscellaneous tasks; for example, drawing figures for papers/reports, setting up a second IC design lab (we outgrew our original research room), and preparing/maintaining documents associated with the project. Arokia's support comes directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $750.

Undergraduate Student

Technician, Programmer

Other Participant

Research Experience for Undergraduates

Name: Brown, James

Worked for more than 160 Hours: Yes

Contribution to Project:

James Brown is an undergraduate who worked on the project last summer (2007). James learned how to use AutoCAD and then prepared a bonding diagram for the integrated circuit under development. James also helped develop the project's web site last summer. James continued to work on the project as an undergraduate in the Fall 2007 and Spring 2008 semesters. James continued work on materials displayed on the project's website and made a presentation about the project at the Argonne Undergraduate Symposium in November 2007. James' support came directly from the NSF grant. James worked 10-20 hours per week at a rate of approximately $13.00/hour.

Years of schooling completed: Junior

Home Institution: Same as Research Site

Home Institution if Other:

Home Institution Highest Degree Granted(in fields supported by NSF): Master's Degree

Fiscal year(s) REU Participant supported: 2007

REU Funding: REU supplement

Organizational Partners

Washington University

Western Michigan University

Other Collaborators or Contacts

Activities and Findings

Research and Education Activities:

Findings:

Training and Development:

The project has provided several graduate students (Mike Hall, Justin Proctor, Nagendra Hari Valluru, Dinesh Kumar Dasari, Sruthi Laxma Reddy, Nam T. Ngyuen, Naga C. Yelchuri, and Antony Paulan) with an opportunity to work on the development of a mixed-signal integrated circuit. Skills provided to students working on this project include: report preparation, maintaining IC design CAD tools, physical layout of both analog and digital integrated circuits, design of digital and analog circuits (operational amplifiers, voltage and current references, digital-to-analog converters), and modeling of systems using both VerilogA and Matlab. Many (Dasari, Valluru, Ngyuen, and Yelchuri)of these students are working on (or have completed - Proctor and Hall) Master Theses. Justin Proctor and Michael Hall made presentations at a graduate symposium held on the SIUE campus in April 2007. Mike Hall also made a presentation at the CSUI symposium held at Argonne National Laboratory in November 2007.

The project also has allowed an undergraduate and a minority student (James Brown) to become involved in a research project and interact with graduate students. James learned how to use AutoCAD to produce bonding diagrams for integrated circuits and on how to create web pages. James made a presentation at a conference this November at Argonne National Laboratory and also presented a poster at the ILSAMP conference near Chicago in October 2007.

Outreach Activities:

In February 2007 and February 2008, the SIUE School of Engineering held an Open House. Many (several hundred) prospective students and parents toured the engineering building. As part of the open house we (myself and graduate students) showcased the IC Design Research

Laboratory. We explained to the visitors the goals and objectives of the NSF project and demonstrated how the integrated circuit under development as part of this NSF grant is designed. We also explained that in addition to the IC being used in nuclear physics experiments how it might someday be used in systems for detecting radiation released as part of a terrorist threat.

Journal Publications

Books or Other One-time Publications

Michael Hall, "Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation
", (2007). Thesis, Published
Bibliography: Masters Thesis, December 2007, can be found in Southern Illinois University Edwardsville Lovejoy Library

Justin M. Proctor, "Design of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Required
", (2007). Thesis, Published
Bibliography: Master Thesis, December 2007, available in Southern Illinois University Edwardsville Lovejoy Library

Dinesh Dasari, "Design of On-chip ADC for Custom ASICs Used in the Detection of Ionizing Radiation", (2008). Thesis, Accepted
Bibliography: Masters Thesis. Available at SIUE Lovejoy Library.

Nagendra Sai Hara Krishna Valluru, "Design of a RAM Buffer for Multi-channel Integrated Circuits
Used in the Detection of Ionizing Radiation
", (2008). Thesis, Accepted
Bibliography: Masters Thesis. Available at SIUE Lovejoy Library.

Web/Internet Site

URL(s):
www.ee.siue.edu:~gengel/PSD.htm
Description:
This site serves as a repository for reports related to the progress of the project. It also provides items of interest to other researchers in the field. For example, the site contains a large collection of Cadence OCEAN scripts which were developed to evaluate the performance of circuits used in the project. The site also contains MathCAD worksheets that were developed to design key components on the IC. The site also contains schematics and other design related data that is available to those interested in the details of the project and/or as examples that may be of use to engineers working on related activities.

Other Specific Products

Contributions

Contributions within Discipline:
A group at Los Alamos (LANL) has become very interested in our PSD chip. They would like to use the chip in the work they do at LANL. We have been talking with Mark Wallace and Edward McKigney among others.

Contributions to Other Disciplines:

Contributions to Human Resource Development:

Contributions to Resources for Research and Education:

Contributions Beyond Science and Engineering:

Special Requirements

Special reporting requirements: None
Change in Objectives or Scope: None
Animal, Human Subjects, Biohazards: None

Categories for which nothing is reported:

Activities and Findings: Any Research and Education Activities
Activities and Findings: Any Findings
Any Journal
Any Product
Contributions: To Any Other Disciplines
Contributions: To Any Human Resource Development
Contributions: To Any Resources for Research and Education
Contributions: To Any Beyond Science and Engineering

2008 NSF Annual Report (August 2008) for Grant #06118996

This report is divided into three sections. We begin by providing a brief overview of the project along with a list of activities that we had proposed to accomplish during over the course of the grant period. In Section II, we describe the activities that have taken place over the past year in broad terms and discuss the status of the project, indicating which of the proposed activities have been accomplished and which must still be completed before the grant ends in February 2009. In the third and final section, we summarize our findings.

I. Project Overview

The IC Design Research Laboratory at Southern Illinois University Edwardsville is part of an interuniversity collaboration which has as its long-term aim the determination of the density dependence of the nuclear asymmetry energy. This greater collaboration has a new experiment in this long-term project which was initially planned to run in early 2008 but was postponed. The experiment is now expected to take place in late 2008 or early 2009. This upcoming experiment (as well as future ones) requires the use of large detector systems for both charged particles and neutrons. Some of these detector systems require particle identification as well as total pulse-height information.

The current objective of this NSF grant was to produce a micro-chip that will complement our existing (shaped and peak-sensing) analog chip (called **HINP16C**) with one capable of particle identification using pulse-shape discrimination (PSD). The PSD integrated circuit (IC) which we have named **PSD8C** is suitable for use with both CsI(Tl) (used for charge-particle discrimination) and liquid scintillator (used for neutron-gamma discrimination) detectors.

Over the initial two-year grant period (Sept. 1, 2006 – Aug. 31, 2008) we had proposed to perform the following activities:

1) design, simulate, layout, and fabricate an IC capable of PSD,
2) train several graduate and undergraduate students,
3) build a prototype system,
4) use it in an upcoming experiment,
5) make a "production chip",
6) and distribute test stations to other interested groups.

In short, successful completion of this project adds a powerful new capability to the CMOS ASIC "tool box" for radiation detection

instrumentation, make large detectors arrays with important information in the pulse shape more cost effective, and trains several graduate and undergraduate students in mixed-signal (CMOS) design.

In the following section of this report we will describe the activities that we were engaged in over the past year (in general terms) and discuss the status of the project. We will indicate which of the proposed activities have been accomplished and which must still be completed before the grant ends in February 2009

II. Activities

Since submitting our first interim report last year at this time, much progress towards completing the project has been made. The PSD8C simulations and layout were completed, and in February 2008 the IC was submitted for fabrication through MOSIS (MOS Implementation Services). The completed chip, PSD8C, is pictured in Figure 1.

We had hoped to fabricate the chip in October or November of 2007, but it took longer than anticipated to physically lay out the PSD8C IC. This was in large part due to the fact that we were not able to re-use as many designs and layouts from our earlier HINP16C IC as we had initially anticipated. Also, verifying correct operation of the IC turned out to be a very time consuming activity. It took three or four days in some cases to perform a single electrical-level simulation. Since the experiment in which the PSD8C is to be used was delayed, it was deemed prudent to use this additional time to verify that the IC would indeed perform well once fabricated.

The eight-channel chip fabrication cost was a little more than $10,000 (die area of 15 mm^2) which was slightly less than what we had budgeted. The PSD8C chip came back from fabrication in mid-May and is currently undergoing testing and performance characterization at Washington University. The chip has been successfully integrated into a prototype system. A prototype system consists of a mother-board which can house several chip-boards. A pair of PSD8C ICs resides on a chip-board. The chip-board was successfully designed, fabricated, and has been tested. An unforeseen problem with the motherboard has delayed testing and performance characterization of the IC but we hope to finish in the near future.

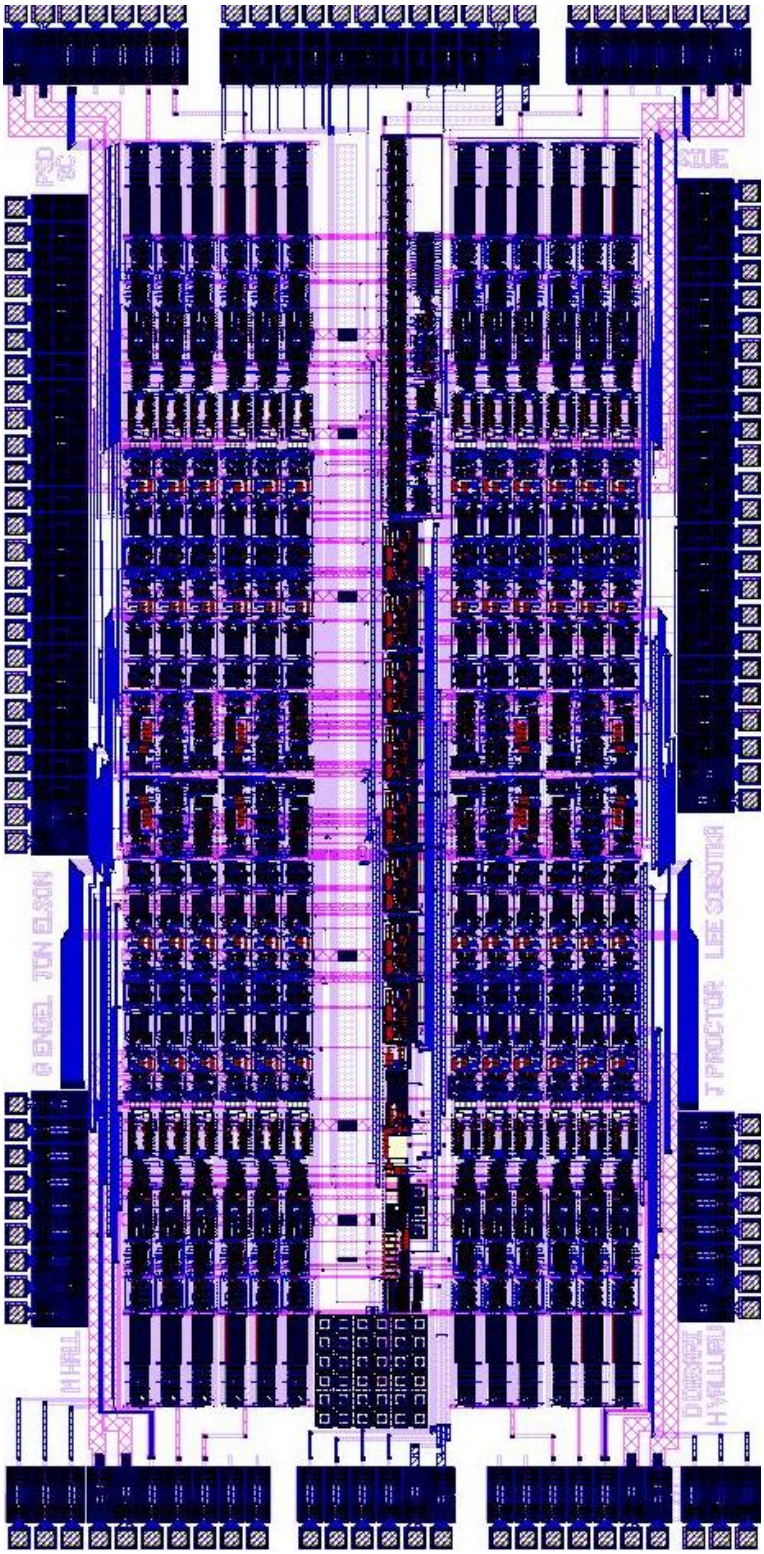

Figure 1: Final layout for PSD8C chip

For the reasons just enumerated we requested and were granted a 6 month no-cost extension to the grant so that we may complete testing of the IC, finish the prototype system, and then use the IC in an experiment either later this year or in early 2009. At that time the chips could also be distributed to other interested groups.

In the list of activities in Section I, item (5) was to produce a "production" chip which meant that we would produce an IC with any known bugs from the first IC fixed and expanded from 8 channels to 16 channels. After many discussions with the nuclear physics community, this item was dropped from our list. This was in large part because we feel very confident that the IC that was submitted and that is currently being tested will perform well enough for it to be used in the first experiment for which it was designed. While the current PSD8C performs the tasks for which it was intended, there are ways to make it easier for a broader community to use. A decision was made to "listen" (as we promised in our NSF proposal we would) to the community of potential users and work on enhancing the existing design.

What the nuclear physics community was really clamoring for, we found out, is a version of PSD8C IC which would have digital output data streams in addition to the analog output pulse trains currently provided by the PSD8C chip pictured in Figure 1. Sensitive analog signals are easily corrupted while digital data streams display great noise immunity. Digital outputs could greatly improve overall system performance.

In order to provide this feature, 3 additional sub-systems must be added to the existing PSD8C design. They are (1) a 12-bit, 2Msample/sec analog-to-digital converter (ADC); (2) a buffer RAM which can store the digital data from ADC prior to its being transmitted back to the host computer via a (3) serial "I2C-like" interface. Finally, the existing readout electronics would need to be modified and enhanced to coordinate the various transfers that need to take place.

Therefore, starting in February 2008 we started on the design of the three sub-systems listed above. Significant progress has been made on (1) and (2) culminating in a pair of Master Theses in August 2008. We hope to make significant headway on item (3) before the grant period ends in February 2009.

Success in training students is exemplified by the four excellent Master Theses that have been produced to date. A description of the work described in the four theses is provided in the following section of this report. A fifth thesis is expected to be completed by December 2008. Graduate student Nam Ngyuen (at SIUE) is working on the "I2C-like" interface mentioned above.

III. Findings

The results of all work carried out to date under NSF Grant #06118996 have been thoroughly documented through a series of four Masters Theses written under the supervision of Dr. George L. Engel (PI). The theses were in partial fulfillment of the requirements for a Masters Degree in Electrical Engineering at Southern Illinois University Edwardsville (SIUE). The theses are available at the SIUE Lovejoy Library. They are also available online at http://www.ee.siue.edu/~gengel/PSD.htm.

The reader is encouraged to read the full text for all of our research findings. In order to keep this report from becoming excessively long, we include only bibliographic information and the abstracts associated with each of the four theses. We feel that the abstracts due an adequate job of summarizing our key findings.

Title: Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation

Author: Michael J. Hall

Date: December 2007

Abstract:

Often in nuclear physics experiments the type of incident radiation must be classified, the energy of the particle must be determined, and the position of interaction within the detector must be estimated. This thesis presents design considerations for several systems that use gated integrators to extract the above information from the pulse. Since the performance of such systems depends upon the signal-to-noise ratio (SNR) of the integrators, an analysis of the SNR characteristics of a gated integrator is presented.

A particle identification (PID) system employing pulse-shape discrimination (PSD) is highlighted. The proposed system makes use of a newly developed multi-channel integrated circuit (PSD8C). We demonstrate that the PID system will work well with both fast and slow detectors, such as organic liquids (e.g. BC 501) and CsI(Tl) scintillation detectors, respectively. For liquid scintillation detectors with a full scale energy range of 10 MeVee, simulation shows a discrimination threshold (1% error of misclassification) of 1.44 MeVee (dynamic range of 17 dB). For CsI(Tl) scintillation detectors with a full scale energy range of 100 MeV, simulation shows a discrimination threshold of 1.55 MeV (dynamic range of 36 dB).

Pulse data from an experiment using a prototype CsI(Na) detector was also analyzed and used to generate an energy spectrum. The energy spectrums for a “noise-free” and a “noisy” (additive noise consistent with the PSD8C chip) system were compared. As these pulse data were collected with ^{137}Cs (662 keV) and ^{60}Co (1173 and 1332 keV) gamma-ray sources, the generated spectrum contained three Gaussian peaks corresponding to the photopeaks. The effect of the chip’s noise is not significant. The width of the first Gaussian increased from 5.68% to 6.34%. The second increased in width from 4.37% to 4.58% while the third increased in width from 4.20% to 4.24%.

This work was initiated by the heavy-ion nuclear chemistry and physics group at Washington University in Saint Louis and is funded by NSF grant #06118996.

Title: Design of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Required

Author: Justin M. Proctor

Date: December 2007

Abstract:

The thesis presents the design, simulation, and layout of an eight channel integrated circuit (IC) for use in nuclear physics experiments where particle identification, total pulse height, and relative timing information is needed. The design employs a technique known as pulse shape discrimination (PSD) to classify the incident radiation. Each of the eight channels is composed of a time-to-voltage converter (TVC) with two time ranges (0.5 μsec, 2 μsec) and three sub-channels. Each of the sub-channels consists of a gated integrator with 8 programmable charging rates and an externally programmable gate generator that defines the start (with 4 time ranges) and width (with 4 time ranges) of the gate relative to an external discriminator signal. The chip supports 3 triggering modes.

The IC produces four sparsified analog pulse trains (3 integrator outputs and 1 TVC output) with synchronized addresses for off-chip digitization with a pipelined ADC. The micro-chip, christened PSD8C, with two bias modes occupies an area of approximately 2.8 mm x 5.7 mm and has an estimated power dissipation of 135 mW in the high-bias mode. The chip is to be fabricated in the AMIS 0.5-micron NWELL process (C5N) in early 2008. This work was initiated by the heavy-ion nuclear chemistry and physics group at Washington University in Saint Louis and is funded by NSF Grant #06118996.

Title: Design of On-Chip ADC for Custom ASICs Used in the Detection of Ionizing Radiaiton

Author: Dinesh K. Dasari

Date: August 2008

Abstract:

This thesis presents the design and simulation of a 12-bit, 2 MSample/sec Analog-to-Digital Converter (ADC). The ADC is intended for integration into a family of integrated circuits (ICs) used in the detection of ionizing radiation. The ICs are being developed by the Integrated Circuit Design Research Laboratory at Southern Illinois University Edwardsville (SIUE). The current chip designs provide analog outputs. Storing data in a digital format on-chip before transmittal to a host computer over an "I2C-like" interface will result in improved system performance.

The ADC will be implemented in the future in a 5-Volt AMIS 0.5 μm, double-poly, tri-metal CMOS process (C5N). The converter described in this thesis employs a two-step flash technique with digital error correction. It is configured as a fully-differential circuit. The converter performs a 7-bit "coarse" flash conversion followed by 6-bit "fine" flash conversion, the results of which are then combined through a digital correction algorithm to produce the desired 12-bit output.

Electrical simulations demonstrate that the noise characteristics of the converter are consistent with those of a 12-bit quantizer. Simulations indicate that, in the presence of typical offset and mismatch errors, the effective number of bits (ENOB) will be 11.8. This work was initiated by the heavy-ion nuclear chemistry and physics group at Washington University in Saint Louis and is funded by NSF Grant #06118996.

Title: Design of a RAM Buffer for Multi-channel Integrated Circuits Used in the Detection of Ionizing Radiation

Author: Nagendra K. Valluru

Date: August 2008

Abstract:

This thesis presents the design, simulation, and layout of a 32 location by 18-bit static Random Access Memory (SRAM). The RAM buffer is intended for use in a family of integrated circuits (ICs) that are being designed by the IC Design Research Laboratory at Southern Illinois University Edwardsville for use in science experiments where the detection of ionizing radiation is needed.

The RAM buffer described will be integrated along with a 12-bit, 2 MSample/sec analog-to-digital converter onto a custom micro-chip, previously designed by our research group, called PSD8C. PSD8C is an eight channel integrated circuit, with analog pulse train outputs, which is to be used in nuclear physics experiments where particle identification is required. Storing the data in a digital format on-chip before transmittal to a host computer over an 'I2C-like' bus will result in improved system performance.