Annual Report for Period: 09/2006 - 08/2007
Submitted on: 08/23/2007
Principal Investigator: Engel, George L.
Award ID: 0618996
Organization: Southern Ill U Edwardsvill
Title:
Development of a Pulse Shape Discrimination CMOS ASIC

Project Participants

Senior Personnel

Name: Engel, George
Worked for more than 160 Hours: Yes
Contribution to Project:
Dr. Engel supervises the development of the ASIC under development for this NSF project.

Name: Sobotka, Lee
Worked for more than 160 Hours: Yes
Contribution to Project:
Dr. Sobotka leads the Washington University nuclear physics group that is helping specify how the ASIC under development should operate.

Name: Famiano, Michael
Worked for more than 160 Hours: Yes
Contribution to Project:
Dr. Famiano will use the ASIC, currently under development, in an upcoming experiment.

Post-doc

Graduate Student

Name: Hall, Michael
Worked for more than 160 Hours: Yes
Contribution to Project:
Michael Hall has worked as a graduate research assistant since the start of the project (Sept. 2006). Mike has been one the principal designers of the integrated circuit under development. Mike will defend his thesis on the topic (December 2007). Mike's support for the past year has come directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $920.

Name: Proctor, Justin
Worked for more than 160 Hours: Yes
Contribution to Project:
Justin Proctor has worked as a graduate research assistant since the start of the project (Sept. 2006). Justin has been one the principal designers of the integrated circuit under development. Justin will defend his thesis on the topic (December 2007). Justin's support for the past year has come directly from the NSF grant.The support consists of tuition remission and a monthly stipend of $920.

Name: Valluri, Nagendra
Worked for more than 160 Hours: Yes
Contribution to Project:
Nagendra (Hari)Valluri has worked on the project as a graduate research assistant since June 1, 2007. Hari is responsible for the physical layout of the digital circuits used in the integrated circuit currently under development for the this NSF project. Hari's support this summer came directly from the NSF grant. Hari will continue to work on the project until Summer 2008. The support consists of tuition remission and a monthly stipend of $920.

Name: Dasari, Dinesh
Worked for more than 160 Hours: Yes

Contribution to Project:

Dinesh Dasari has worked on the project as a graduate research assistant since May 15, 2007. Dinesh is responsible for the physical layout of the analog circuits used in the integrated circuit under development for the this NSF project. Dinesh's support this summer came from state of IL matching funds ($10,000) that the university awarded me to be used on the project. Dinesh will continue to work on the project until Summer 2008. The support consists of tuition remission and a monthly stipend of $920.

Undergraduate Student

Technician, Programmer

Other Participant

Research Experience for Undergraduates

Name: Brown, James

Worked for more than 160 Hours: Yes

Contribution to Project:

James Brown is an undergraduate who worked on the project this summer (2007). James learned how to use AutoCAD and then prepared a bonding diagram for the integrated circuit under development. James also helped develop the project's we site this summer. James will continue to work on the project as an undergraduate this coming Fall. James' support this summer came directly from the NSF grant. James worked 20 hours per week at a rate of $13.00/hour.

Years of schooling completed: Junior

Home Institution: Same as Research Site

Home Institution if Other:

Home Institution Highest Degree Granted(in fields supported by NSF): Master's Degree

Fiscal year(s) REU Participant supported: 2007

REU Funding: REU supplement

Organizational Partners

Washington University

Western Michigan University

Other Collaborators or Contacts

Activities and Findings

Research and Education Activities: (See PDF version submitted by PI at the end of the report)

Findings: (See PDF version submitted by PI at the end of the report)

Training and Development:

The project has provided several graduate students (Mike Hall, Justin Proctor, Nagendra Hari Valluri, Dinesh Kumar Dasari) with an opportunity to work on the development of a mixed-signal integrated circuit. Skills provided to students working on this project include: physical layout of both analog and digital integrated circuits, design of digital and analog circuits (operational amplifiers, voltage and current references, digital-to-analog converters), and modeling of systems using both VerilogA and Matlab. All of these students are working on

Master Theses and Justin Procor and Mike Hall made presentations at a graduate symposium held on the SIUE campus this past April.

The project also has allowed an undergraduate and a minority student (James Brown) to become involved in a research project and interact with graduate students. James learned how to use AutoCAD to produce bonding diagrams for integrated circuits and on how to create web pages. James plans to make a presentation at a conference this November at Argonne National Laboratory and also plans to present a poster at the ILSAMP conference near Chicago this October.

Outreach Activities:

In February 2007, the SIUE School of Engineering held an Open House. Many (several hundred) prospective students and parents toured the engineering building. As part of the open house we (myself and graduate students) showcased the IC Design Research Laboratory. We explained to the visitors the goals and objectives of the NSF project and demonstrated how the integrated circuit under development as part of this NSF grant is designed. We also explained that in addition to the IC being used in nuclear physics experiments how it might someday be used in systems for detecting radiation released as part of a terrorist threat.

Journal Publications

Books or Other One-time Publications

Web/Internet Site

URL(s):

www.ee.siue.edu:~gengel/PSD.htm

Description:

This site serves as a repository for reports related to the progress of the project. It also provides items of interest to other researchers in the field. For example, the site contains a large collection of Cadence OCEAN scripts which were developed to evaluate the performance of circuits used in the project. The site also contains MathCAD worksheets that were developed to design key components on the IC. The site also contains schematics and other design related data that is available to those interested in the details of the project and/or as examples that may be of use to engineers working on related activities.

Other Specific Products

Contributions

Contributions within Discipline:

Contributions to Other Disciplines:

Contributions to Human Resource Development:

Contributions to Resources for Research and Education:

Contributions Beyond Science and Engineering:

Special Requirements

Special reporting requirements: None

Change in Objectives or Scope: None

Unobligated funds: $ 0.00

Animal, Human Subjects, Biohazards: None

Categories for which nothing is reported:

Any Journal
Any Book
Any Product
Contributions: To Any within Discipline
Contributions: To Any Other Disciplines
Contributions: To Any Human Resource Development
Contributions: To Any Resources for Research and Education
Contributions: To Any Beyond Science and Engineering

ACTIVITIES

Project Overview

The IC Design Research Laboratory at Southern Illinois University Edwardsville is part of an interuniversity collaboration which has as its long-term aim the determination of the density dependence of the nuclear asymmetry energy. This greater collaboration has a new experiment in this long-term project which is planned to run in early 2008. This upcoming experiment (as well as future ones) requires the use of large detector systems for both charged particles and neutrons. Some of these detector systems require particle identification as well as total pulse-height information.

The current objective of this NSF grant is to produce a micro-chip that will complement our existing (shaped and peak-sensing) analog chip (called **HINP16C**) with one capable of particle identification using pulse-shape discrimination (PSD). The PSD integrated circuit (IC) which we have named **PSD8C** will be suitable for use with both CsI(Tl) (used for charge-particle discrimination) and liquid scintillator (used for neutron-gamma discrimination) detectors.

Over the two-year grant period (Sept. 1, 2006 – Aug. 31, 2007) we proposed to perform the following activities:

1) design, simulate, layout, and fabricate an IC capable of PSD,
2) build a prototype system,
3) use it in an upcoming experiment,
4) make a "production chip",
5) and distribute test stations to other interested groups.

Successful completion of this project will add a powerful new capability to the CMOS ASIC "tool box" for radiation detection instrumentation, make large detectors arrays with important information in the pulse shape more cost effective, and train several graduate and undergraduate students in mixed-signal (CMOS) design.

In short, we hope to complete **PSD8C** (1) by early October, at which time the IC will go out to the fabricators. It is expected back from the fabricator before year's end. Work will begin shortly on the construction of the prototype system (2) and will be finished in early 2008 at which time this prototype will be used in an experiment (3). A "production" version (**PSD16C)** of the chip (4) will address any deficiencies uncovered in the initial "prototype" and will be fabricated in Spring 2008 in sufficient quantities so that in can be incorporated into a small number of test stations that will be distributed to a few interested groups (5) around the country. The remainder of the "Activities" section of the report will provide a description of the IC (**PSD8C**) under development and of the activities performed during the past year. While the description is based on the one included in the original proposal, it has been updated to reflect changes that have been a direct result of this past year's work.

Description of Integrated Circuit (PSD8C)

Our design makes use of CMOS technology to provide a) integration of several regions of the analog pulse generated by the detector, b) provide time-to-amplitude conversion and c) prepare each of the above as analog data streams for a pipeline VME ADC.

Detector outputs are split for logic and linear branches. Timing signals are generated by leading-edge or constant-fraction-discriminators (CFDs). We plan to use VME CFD's for the upcoming experiment. The individual timing signals and delayed linear signals are sent to the CMOS chip.

The proposed pulse-shape discrimination scheme with a 16-channel chip, **PSD16C**, (we are currently working on an 8-channel version, **PSD8C**) is illustrated in Fig. 1. The individual CFD logic signals, ANDed with a global enable signal, provide channel enables. For each linear signal (accompanied by its logic), three different integrations (called **A, B** and **C**) will be performed with start times referenced to the individual discriminators. In addition, an amplitude **T** is produced which is proportional to the difference in time between the individual discriminator firing and an external common stop reference. The **T** amplitude eliminates the need for conventional VME TDC's.

The delays in the integrators' starting times (D_A, D_B, D_C) and the widths (W_A, W_B, W_C) of the integration windows are controlled by the user on a chip-by-chip basis. In Fig. 1, the delays D_A, D_B, D_C are voltages that are converted to times on-chip as are the widths W_A, W_B, W_C.

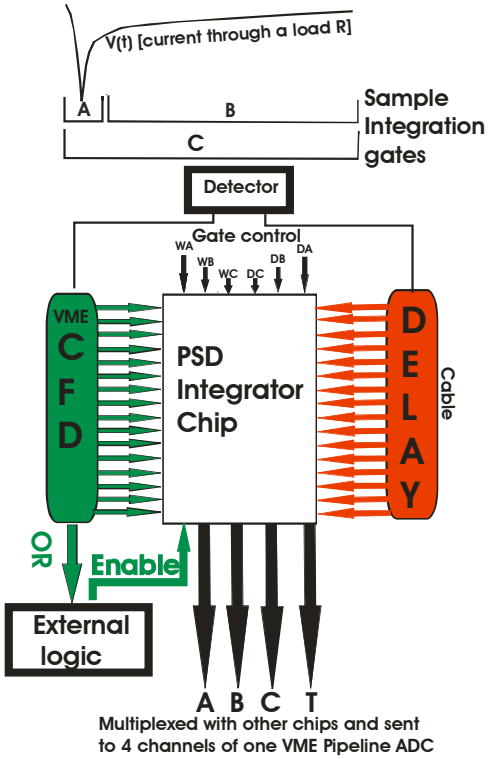

Fig. 1: Overview of analog pulse-shape discrimination scheme integration.

Each channel, illustrated in Fig. 2, in this multi-channel IC is composed of three sub-channels, a time-to-voltage converter (TVC), and read-out related electronics. The three sub-channels are identical. The sub-channels produce the three different integrations (**A, B** and **C**), and the TVC produces the amplitude **T** that is proportional to the difference in time between the channel's discriminator firing and an external common stop reference.

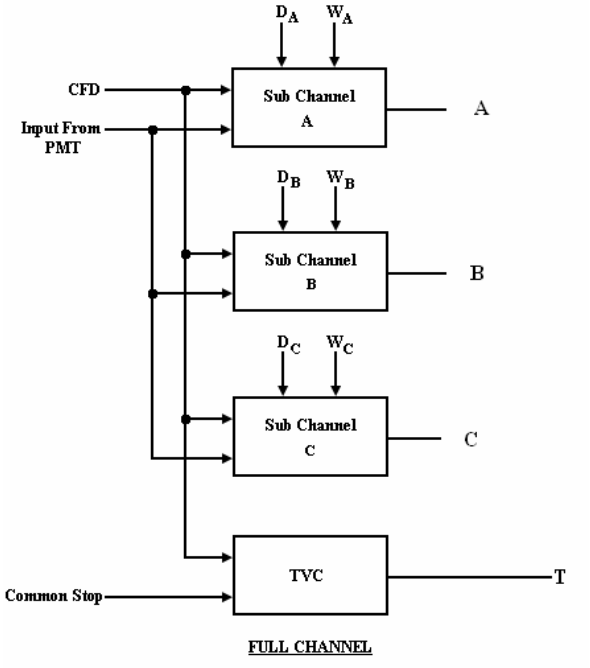

Fig. 2: Architecture of a single channel composed of three sub-channels and time-to-voltage converter (TVC)

Aside from the user controlled delay and widow widths, the feature that allows **PSD8C** to be used with detectors as diverse as liquid scintillators (fast) and CsI (slow) is a bank of resistors (in each sub-channel) which determine the charging rate of the integrating capacitor (10 pF). The values settled upon (after much discussion over the course of the last year) are shown in Table 1.

Setting	Resistance	
0	500 Ω	*default*
1	1,000 Ω	
2	2,000 Ω	
3	5,000 Ω	
4	10,000 Ω	
5	20,000 Ω	
6	50,000 Ω	
7	100,000 Ω	

Table 1: Resistor values that set charging rate

The architecture of a sub-channel is presented in Fig. 3.

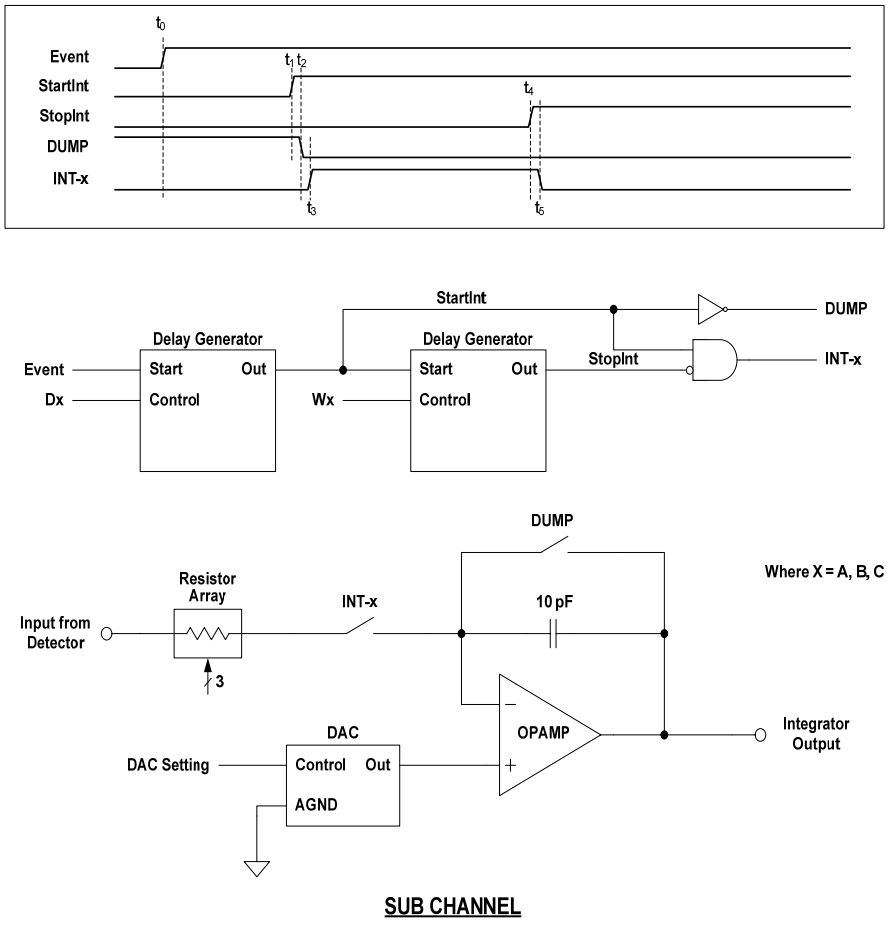

Fig 3: A sub-channel contains an integrator with programmable charging rate and circuitry to control start of and duration of the integration period.

The sub-channel of Fig. 3 operates as described herein. Initially, the integration capacitor is discharged (DUMP signal is active). The firing of the channel's CFD starts the delay generator on the left side of the figure.

The delay generator consists of a constant current source charging a capacitor which produces a voltage linearly proportional to time. When this voltage equals the externally applied control voltage D_x (where x = **A**, **B**, or **C)**, an analog comparator fires and starts the second delay generator depicted in Fig. 3. The charging rate of the capacitor in the delay generators can be different for each of the three sub-channels in keeping with our desire to have the three sub-channels possess different ranges of delay and integration width. However, all **A** sub-channels on a chip will have the same setting. The same is true of the **B** and **C** sub-channels. While the delay within the range is controlled by an

external voltage, one of four ranges can be selected by the user. The time delay depends upon both the range selected and the applied externally control voltage. The ranges chosen (once again after much study over the past year) are presented in Table 2.

Setting	Minimum	Maximum	
0	10 ns	50 ns	*default*
1	30 ns	150 ns	
2	120 ns	600 ns	
3	2,000 ns	10,000 ns	

Table 2: Delay and Integration Width Ranges

When the second delay generator (shown on right-side of Fig. 3) starts, the DUMP signal is de-asserted thereby starting the integrator. The integration period ends when the output voltage of this second ramp voltage equals the voltage, W_x, which determines the *width* of the integration period for the sub-channel. The switch controlled by the signal INT_x in turn opens, disconnecting the charging resistor from the integrator amplifier and forcing the integrator to "hold" its output voltage until it can be sampled. After the output voltage is read by the off-chip ADC, both delay generators are reset and the integrating capacitor voltage dumped. If the voltages are not read out within a user-specified window after the event occurs, the channels are *automatically* reset. The duration of time before the automatic reset occurs is determined by an externally supplied control voltage. It can be set from a few hundred nanoseconds to many microseconds.

PSD8C supports 3 triggering modes. The triggering logic is illustrated in Fig. 4 and operation is summarized in Table 3.

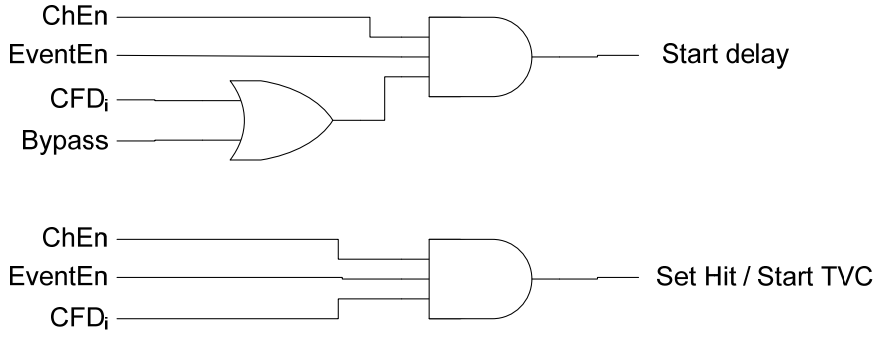

Fig. 4: Trigger Logic

	Mode 1	Mode 2	Mode 3
Acquisition All	1 (prior to readout)	0	0
Bypass	1	1	0
EventEn	Timing signal for start	Timing signal for start	1
CFD_i	Ignore	Sets the hit register	Timing signal for start & sets the hit register
TVC	Ignore	Relative to CFD_i	Relative to CFD_i

Table 3: Trigger modes

The triggering logic is designed to have considerable flexibility. This logic has three modes which are designed for the following purposes:

- Externally event enabled and gated timed without time-to-common stop.
- Externally event enabled and gated timed with individual CFD_i to common stop.
- Externally event enabled, internally gated timed with individual CFD_i to common stop.

.
The three modes are described below.

- ***MODE 1***: EventEn sets the timing for starting the delay in the sub-channels. All channels are then forced to be hit by asserting the "acquisition all" pin. The output of the TVC should be ignored, since it is relative to CFD_i, NOT EventEn in this mode.
- ***MODE 2***: EventEn sets the timing for starting the delay in the sub-channels. The CFD_i signal for each channel sets the appropriate hit register for the channel that was hit. TVC timing is relative to the CFD_i signal. For Mode 2, the EventEn needs to arrive prior to the CFD_i signal for timing to be relative to the CFD_i signal
- ***MODE 3***: CFD_i sets the timing for starting the delay in the sub-channels. It also sets the hit register for the channel that was hit. TVC timing is relative to the CFD_i hit signal.

  For all modes, the TVC is always stopped by the "common stop" signal.

In addition to the three sub-channels, each channel contains a time-to-voltage converter (TVC) as mentioned earlier. The TVC has two timing ranges, given in Table 4.

Setting	Range	
0	2 µs	*default*
1	500 ns	

Table 4: TVC timing ranges

A large number of user-selected options can be programmed via **PSD8C's** 48-bit configuration register as presented in Table 5.

Bit Position	Function	Default
0 – 7	0 = Enable Ch X (Bit 0 = Ch 0) 1 = Disable Ch X	Ch X enabled
8 – 15	Reserved (for 16 channel chip)	
16 – 18	Gain setting A (Bit 18 MSB)	500 Ω
19 – 21	Gain setting B (Bit 21 MSB)	500 Ω
22 – 24	Gain setting C (Bit 24 MSB)	500 Ω
25 – 26	VTC delay range setting A (Bit 26 MSB)	50 ns range
27 – 28	VTC width range setting A (Bit 28 MSB)	50 ns range
29 – 30	VTC delay range setting B (Bit 30 MSB)	50 ns range
31 – 32	VTC width range setting B (Bit 32 MSB)	50 ns range
33 – 34	VTC delay range setting C (Bit 34 MSB)	50 ns range
35 – 36	VTC width range setting C (Bit 36 MSB)	50 ns range
37	VTC range setting	2 μs range
38	0 = high bias mode 1 = low bias mode (1/5th current)	High bias mode
39	0 = test mode TAC OFF 1 = test mode TAC ON i.e. Start and stop signals for selected channel and subchannel brought out to pins	Test mode TAC OFF
40-47	Chip ID #	0

Table 5: Configuration Register

The simulated responses of the chip (a) liquid scintillator (gamma - red, neutron – blue) and (b) CsI (proton – red, alpha – blue) are shown in Fig. 5. These crude simulations are at the symbolic math level and make use of average (noiseless) signals deduced from devices built by the Washington University group. In these simulations only the **A** and **B** sub-channels were needed to clearly distinguish the waveforms (modeled by sums of exponential functions with parameters determined from the real devices.)

Much of the work over the past year focused on identifying sources of noise, estimating the level of the various noise sources, and predicting **PSD8C** performance. The remainder of this report attempts to detail the steps taken to determine chip expected performance and our findings to date.

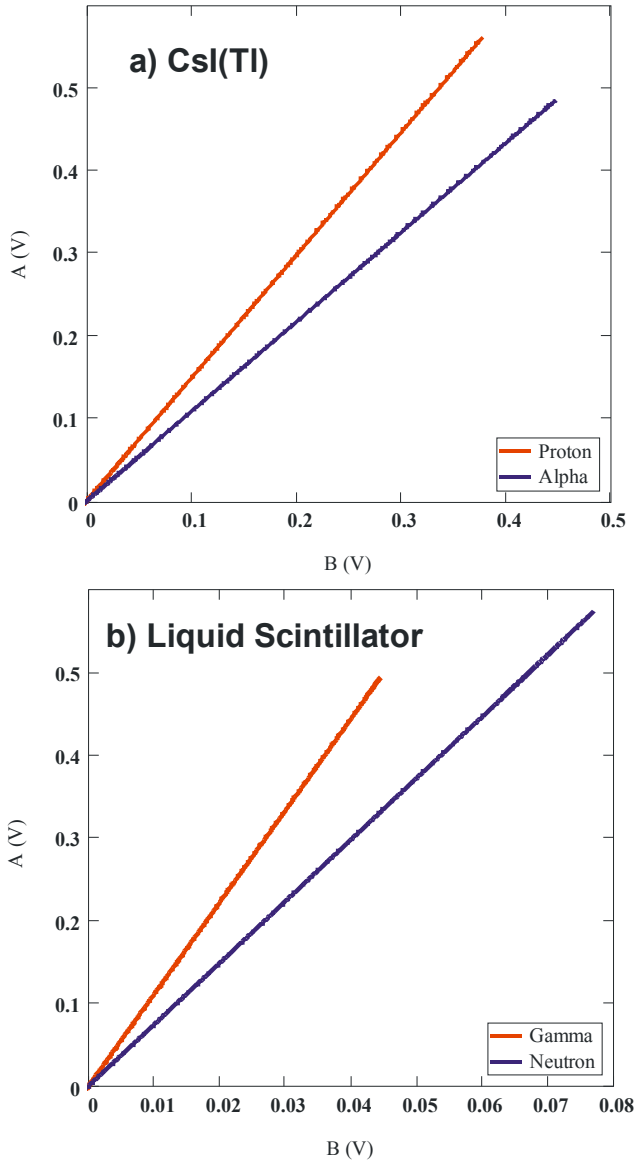

Fig. 5: Pulse-shape discrimination plots (integrations in two different regions plotted against one another) as a function of deposited energy. (The energies increase going up the curves.) These plots are for: (a) CsI(Tl) (proton – red, alpha – blue) and (b) liquid scintillator (gamma - red, neutron – blue). The B voltage (delayed gate) for the liquid scintillator would be differentially amplified off chip before digitization. These simulations model the time dependent detector outputs as the sums of exponentials with particle dependent but energy independent parameters.

Activities Performed Over Past Year

Over the past year a wide range of tasks were performed in our attempt to develop the **PSD8C** IC described in the previous section of this report. Here is a summary of the important tasks that were undertaken and successfully completed.

- Representative detectors and particles for identification were chosen. Specifically, we selected CS-I (for alpha-proton discrimination) and liquid scintillator (for neutron-gamma discrimination) to study. CS-I is representative of a class of *slow* detectors while the liquid scintillator is a good example of a *fast* detector.

- Appropriate signal and *noise* models (Poisson) for the representative signals were created. The models included the impact of the off-chip electronics that condition the signals before they are presented to the IC. Time-domain representative waveforms were generated using MATLAB.

- All sources of electronics noise that determine the signal-to-noise ratios (SNRs) at the output of the integrators were identified and studied. Time-domain noise waveforms for each of the noise sources were generated using MATLAB. Extensive time-domain simulations (*very slow*) were performed and SNRs determined. The probability of miss-classifying a particle is related to the SNRs associated with the individual integrator outputs. The higher the SNRs associated with the integrator outputs, the better the performance.

- Analytical expressions to describe the SNR characteristics of the integrators were derived and compared to the time-domain results (above). The statistical properties of the various noise sources are parameters in our analytical expressions. The agreement was very good so in future studies we were able to *very quickly* compute the SNRs associated with the integrator outputs using the analytical expressions and not have to resort to the *slow* time-domain simulations to compute SNRs.

- In Fig. 5, ideal (noiseless) pulse-shape discrimination plots were presented. *Noisy* versions of these plots were produced using the analytical expressions described above. While each channel in the IC contains three sub-channels (known as **A**, **B**, and **C**) in many of the studies undertaken thus far we have only used the **A** and **B** integrator outputs. Sub-channel **A** integrates early in the pulse (*early* gate) while sub-channel **B** (*delayed* gate) is used to integrate into the tail region of the pulse. A better way to visualize system performance (defined as one's ability to properly discriminate particles) was developed. We produced what we term "angular PSD plots". The angle in question is defined as

  $$\theta = \tan^{-1}(A/B)$$

  where **A** is the output of sub-channel's **A** integrator and **B** is the output of sub-channel' **B** integrator. If we consider the *noiseless* case where we would like to

discriminate between two particles which we shall call the "0"-particle and the "1"-particle, then one would observe an angle θ_0 whenever the "0"-particle is presented to the channel and an angle θ_1 whenever the "1"-particle is presented. The plot contains only two vertical lines. When noise is introduced, the plot becomes that of two Gaussians with the means located at the locations of the previous vertical lines in the noiseless case. A figure of merit (FOM) was defined:

$$FOM = \frac{|\theta_1 - \theta_0|}{\sqrt{\text{var}(\theta_1) + \text{var}(\theta_0)}}$$

- We developed analytical expressions for both the mean of the angle θ (depends on signal and integration interval) and for the variance of the angle θ (depends on signal level, noise properties, and the integration period). This allowed us to actually derive an *analytical* expression for the FOM.

- Code was developed to locate (very quickly) optimal regions of integration by searching for the maximum FOM using the aforementioned analytical expression which had as its parameters the start and duration of each of the three sub-channel integration periods. This was, in part, undertaken so as to make sure that we would choose ranges for the delays and integrations widths that would allow for the best performance possible.

- Since SNRs also depend upon the integrating charging rates, MATLAB simulations were performed to determine the appropriate number of and value of resistors that set the charging rate. The values were given in Table 1 earlier.

- With results from the above activities we were able to move on to the actual circuit level design of **PSD8C**. For each functional block the following tasks were performed:

    - A VerilogA model was written and simulated.
    - An electrical circuit was designed and simulated.
    - Scripts were written to characterize the circuit across many process, supply voltage, and temperature corners.
    - The circuit was physically layed out and then design rule checked and verified against the schematic for correctness.

- **PSD8C** consists of 8 identical processing channels along with a common channel. The common channel hosts the bandgap voltage reference, biasing circuits, buffer amplifiers (that permit us to drive off-chip electrical loads), readout electronics, and a 48-bit configuration register. The functional blocks that make up the common channel were assembled, simulated, and physically layed out. The same can be said for the functional blocks that comprise the signal processing channel.

A processing channel consists of 3 sub-channels, a time-to-voltage converter (TVC), channel-level readout electronics, and triggering logic. Each sub-channel, in turn, consists of a bank of 8 gain-setting resistors, an integrating capacitor, an integrating op amp, a 5-bit DAC (used for offset cancellation of the integrating op amp), and two delay generators.

- The tasks of simulating correct operation of the entire chip as well as assembling the layout of the 8 channels, the common channel, and the I/O pads into a completed layout is yet to be undertaken but will occur over the next two months so that the IC can be submitted for fabrication in mid-October.

Findings

In this section of the report we summarize our findings. To keep the report from becoming excessively long, we will only include a sampling of our results. More extensive results can be found on our website. MATLAB code and MathCAD design sheets used in the project as well as a complete set of schematics for the IC under development are available at our website: http://www.ee.siue.edu/~gengel/PSD.htm.

Fig.1 shows representative analog waveforms for an alpha particle and a proton when using a CsI detector. The waveforms were produced using the popular MATLAB simulation program. The waveforms were modeled using the sum of two exponentials. Appropriate levels of Poisson noise were added to produce the *noisy* waveforms shown below. In the figure below sub-channel **A** (in each of the 8 channels) integrates from 0 to 600 ns, **B** from 1000 to 7000 ns, and **C** from 0 to 9000 ns.

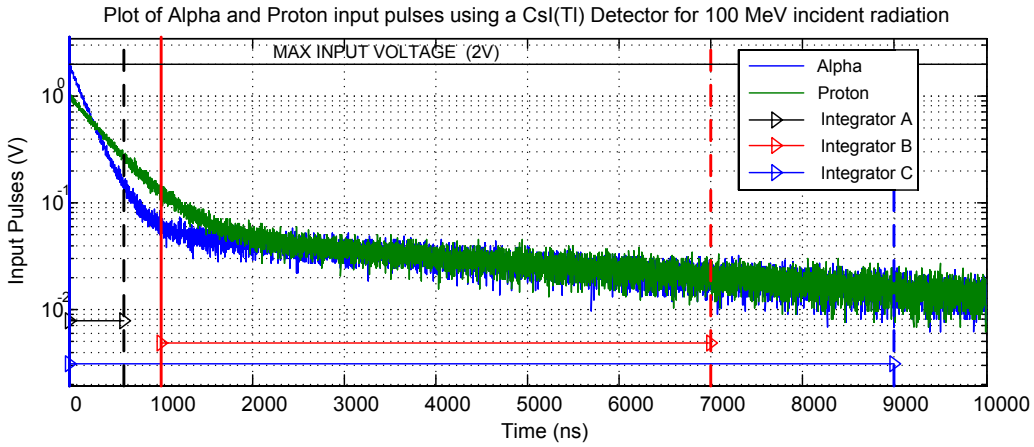

Fig. 1: Representative "noisy" waveforms.

In addition to Poisson noise (due to the random arrival of discrete electrons) the following sources of noise for the integrator circuit illustrated in Fig. 2 were identified:

- ***Jitter*** – noise created by an uncertainty in the integration start time and in the width of the integration period
- ***RI*** – thermal noise from the integrating resistor sampled onto the integrating capacitor
- ***OTA*** – thermal noise of the op amp sampled onto the integrating capacitor
- ***OTA (+)*** – continuous additive input-referred thermal noise of the op amp
- ***1/f*** – 1/f noise of the op amp sampled onto the integrating capacitor
- ***1/f (+)*** – continuous additive input-referred 1/f noise of the op amp

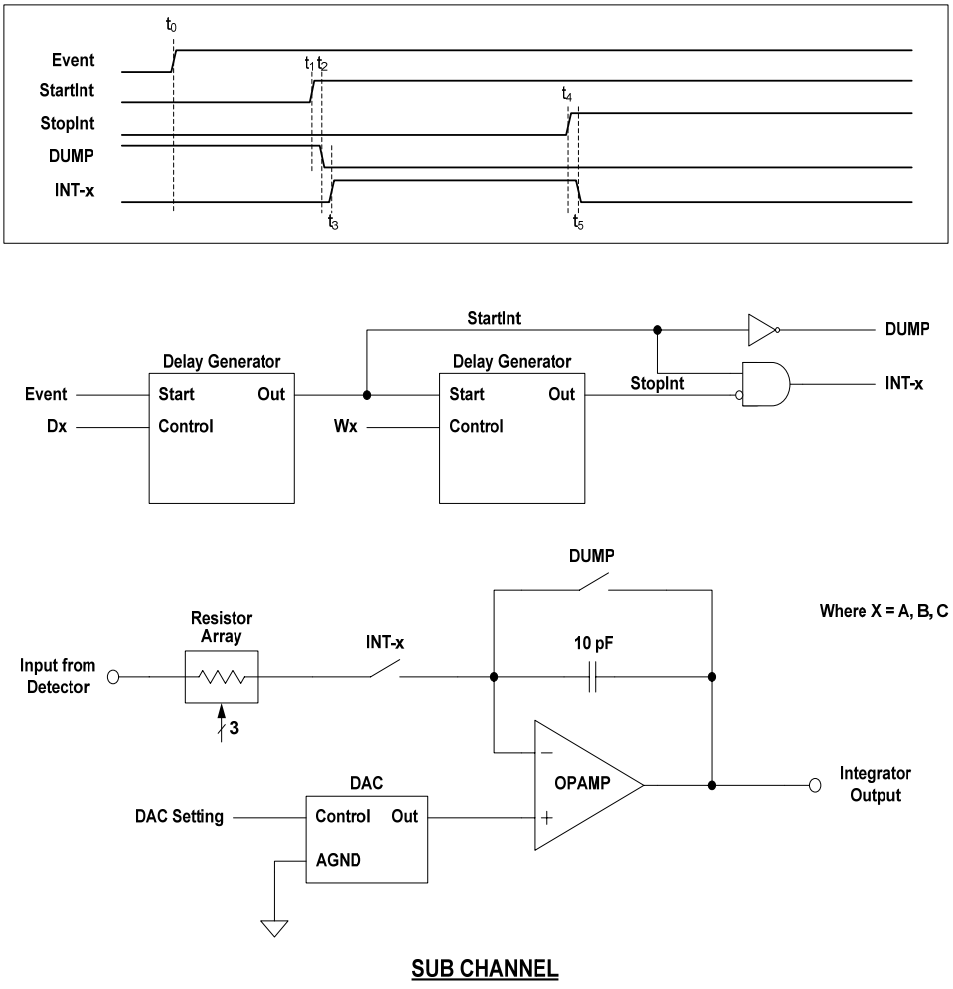

Fig.2: Sub-channel integrator circuit

MATLAB code was written to generate time-domain realizations of the various noise sources and the noise at the integrator output observed and quantified. We then derived analytical expressions for the noise that we would expect to observe at the integrator output based on the statistical properties of the various input noise sources. For the interested reader, analytical expressions for the noise expected at the output can be found on our website. The agreement between the level of noise observed in the time domain simulations and those predicted analytically based on the input noise properties and the circuit transfer functions was *excellent*.

A careful study of the relative importance of each noise source was conducted. Histogram style plots (presented in Fig. 3) were generated for the expected noise at the integrator outputs in each of the three sub-channels. In Fig. 3 we consider a CsI detector. Similar plots were generated for a liquid scintillator detector.

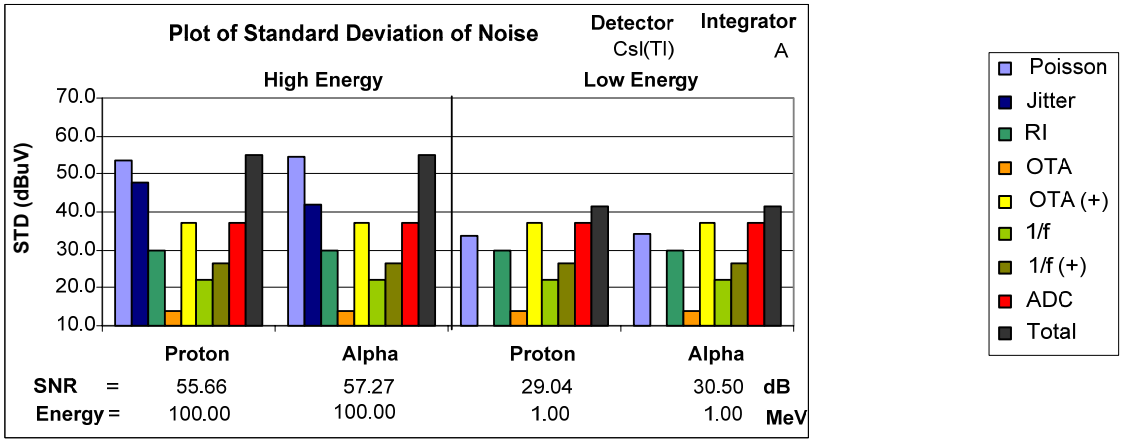

Fig. 3 (a): Sub-channel A

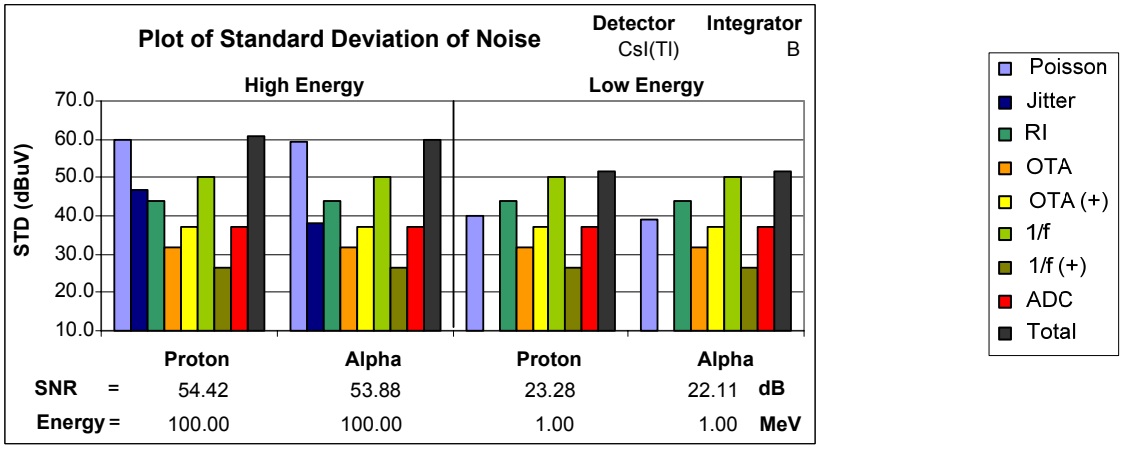

Fig. 3 (b): Sub-channel B

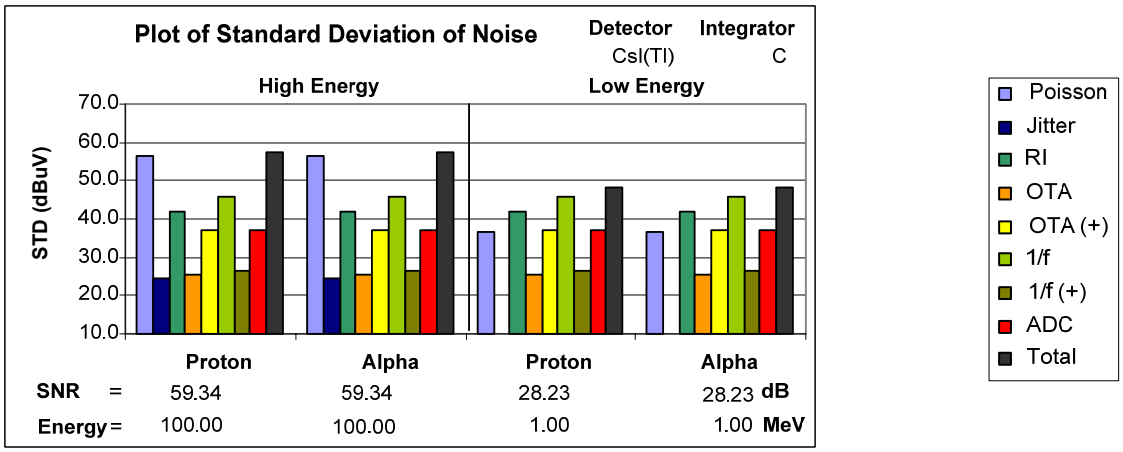

Fig. 3 (c): Sub-channel C

For the case of the CsI detector (alpha-proton discrimination) we concluded the following:

- Poisson noise dominates for high-energy particles, but tends to be on par with electronics noise (10 pf integrating capacitor) for low-energy particles.
- Jitter induced noise is not a dominant noise source, but is on par with Poisson noise for the **A** sub-channel (*early* gate) at high energy.
- 1/f noise dominates for low-energy particles in the **B** and **C** sub-channels (*late* gates)
- Electronics noise is on par with the quantization noise of a 12-bit ADC except for 1/f noise in the **B** and **C** sub-channels which tends to dominate at low energy.

For liquid scintillator detectors, we find that:

- Poisson noise no longer dominates *except* in sub-channel **A** (*early* gate) in which the integration begins before the start of the pulse.
- Jitter becomes important in the **B** and **C** sub-channels (*late* gates) and dominates at high energy levels.
- Electronics noise (especially for the **B** and **C** sub-channels) is significantly larger than the quantization noise of a 12-bit ADC but still on par with Poisson noise.
- 1/f noise is on par with the thermal noise for low-energy particles in the **B** and **C** sub-channels.

As discussed in the "Activities" section of this interim report, angular PSD plots were generated and used to quantify the chip's ability to discriminate particles. The angle,θ, is defined as

$$\theta = \tan^{-1}(A/B) \qquad \text{Eqn. (1)}$$

where A is the output of sub-channel A, and B is the output of sub-channel B A detailed analysis was performed and (in the presence of noise) we were able to determine analytically that the variance of the angle is given by

$$\mathrm{var}(\theta) = \frac{\sin^2 2\theta}{4} \cdot \left[\frac{1}{SNR_A^{\,2}} + \frac{1}{SNR_B^{\,2}} \right] \qquad \text{Eqn. (2)}$$

The SNRs used in Eqn. (2) were also computed using analytical expressions which we derived based on the statistics of the input noise sources and circuit transfer functions.

In short, we find that:

- The mean of the angle, θ, is a function only of the signal levels associated with the integrator outputs.
- The variance of the angle, θ, in the angular PSD plot depends primarily upon the signal-to-noise ratio of the integrator outputs.
- Small signal-to-noise ratios, which correspond to low-energy particles, result in a larger variance in angle which is consistent with simulation.

A Figure of merit (FOM) was defined as the difference between the means divided by the square root of the sum of the variances of the two angles.

$$FOM = \frac{|\theta_1 - \theta_0|}{\sqrt{\text{var}(\theta_1) + \text{var}(\theta_0)}} \qquad \text{Eqn. (3)}$$

A representative plot for a CsI detector (alpha-proton discrimination) is shown in Fig. 4. The histogram plot of Fig 4 was produced using MATLAB simulations. The smooth curves that "envelope" the histogram data, however, were generated using Eqn. (2). As one can clearly see, the agreement between the MATLAB simulations and the analytically derived expressions is excellent.

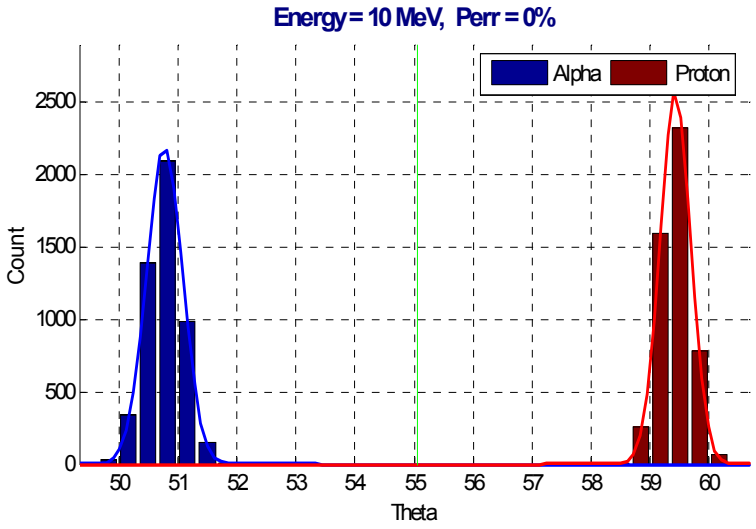

Fig 4: Angular plot

As mentioned earlier we developed code to find the optimal integration windows in each of the three sub-channels. We compared the integration regions found by the optimizer with regions suggested by researchers at Washington University based on past work. For the CSI detector a significant improvement in performance was obtained by using the optimizer:

- FOM was improved by the optimizer by
  - Separating the means
  - Narrowing the variances
- This was accomplished by improving the SNR at low energy while decreasing the SNR at high energy. After optimization, the noise is predominantly Poisson. Electronics noise was made less significant.
- Jitter related noise was actually increased, but at a rate lower than the rate at which the signal increased.
- The optimizer revealed that integrating deep into the tail region is sub-optimal.
- The energy at which the probability of error was 1%
  - Before optimization: 1.05 MeV
  - After optimization: 145 keV

For the liquid scintillator detector only a modest improvement in performance was obtained:

- Unlike with the CsI detector, the optimizer was unable to improve the FOM by separating the means and improving SNR.
- SNR decreased slightly even though we saw a decrease in noise.
- FOM was improved by shifting the means to the left
- This resulted in a decrease in θ for the two particles which gave us a decrease in the variance of θ.
- The energy at which the probability of error is 1%
  - Before optimization: 650 keV
  - After optimization: 400 keV
- In order to get a real improvement, we would need larger charging rates so as to achieve more gain. This is not practical on the IC for the current CMOS process employed.

In summary, we find that

- Proposed PSD IC will work very well with CSI detectors with performance limited by Poisson noise. Particles differing in energy by as much as 40 dB can be easily discriminated.

- Proposed PSD IC will work reasonably well with liquid scintillator detectors. Performance will be most likely by the level of timing jitter (associated with the off-chip CFD circuits). Particles differing in energy by less than 20 dB will have little probability of misclassification.

- While the electronics noise is significant for the **B** and **C** integrators for both detectors at low energy, it is clearly worse for the liquid scintillator detector where it is significantly higher than the quantization noise of a 12-bit ADC.

- Correlated double sampling to deal with 1/f noise does not appear necessary.

- Poisson noise dominates in sub-channel **A** for both CsI(Tl) and liquid scintillator detectors at all energies except for CsI(Tl) at low energies.

- We have developed code that can help ensure the best performance possible from the chip by providing researchers who use **PSD8C** with appropriate integration windows for each of the sub-channels. All the researchers must provide are models for the signals that the IC will be presented with.

With regard to our findings at the circuit-level, we will be brief. While the design of the IC at the electrical level is complete, the circuits have not been fully characterized at this time. The performance data needs to be put into a format more suitable for presentation. For each circuit in the IC, however, the following tasks have been completed:

- A VerilogA model of the circuit has been written and simulated.
- An electrical circuit has been designed and successfully simulated.
- Scripts have been written to characterize the circuit across many process, supply voltage, and temperature corners.
- The circuit was physically layed out and then design rule checked and verified against the schematic for correctness.
- We are currently working on simulations that demonstrate that the IC as a whole functions correctly

.
We include only a brief synopsis of circuit performance at this time. For the interested reader, a complete set of schematics of the IC has been placed on our website. Once we get the performance data in a format suitable for presentation, we will place this data on the website, also.

PSD8C consists of 8 identical processing channels along with a common channel. The common channel hosts the bandgap voltage reference, biasing circuits, buffer amplifiers (that permit us to drive off-chip electrical loads), readout electronics, and a 48-bit configuration register. The readout electronics are the same as used in our existing ASIC.

The bandgap reference has been designed, simulated, and physically layed out. Here is a summary of performance.

- Supply current (typical): 1.5 mA (“fast”), 0.75 mA (“slow”)
- Noise at output: 100 μV (10 Hz - 10 MHz)
- Nominal output: 1.233 Volts (27 C)
- Tempco: +125 μV / C

The time-to-voltage converter (TVC), the voltage-time-converters (VTC) which are used in the delay generators, and the DACs used for offset compensation all require a constant current. It is important that the current display little, if any, temperature dependence. The bandgap voltage is applied across a temperature independent resistor. The temperature independence of the resistance is accomplished through a series combination of a resistance with a positive temperature coefficient (ny polysilicon) and a resistance with a negative temperature coefficient (hy polysilicon). The temperature dependence of the current used in the TVC for charging has a temperature coefficient of +850 pA / C.

Analog signals will be brought off the chip differentially. The op amps used in the single-to-differential conversion circuits were designed to comfortably drive off-chip loads of 25 pF and 10 kΩ. A folded cascade topology with a class AB output stage was used. The op amp has complementary (NFET and PFET) input stages. The op amp exhibits the following performance (nominal) characteristics:

Settling time (14-bit accuracy): < 1 μsec
Total integrated noise: < 180 μVolts

A processing channel consists of 3 sub-channels, a time-to-voltage converter (TVC), channel-level readout electronics, and triggering logic. Each sub-channel, in turn, consists of a bank of 8 gain-setting resistors (500 Ω, 1 kΩ, 2 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 50kΩ, 100 kΩ), an integrating capacitor (10 pF), an integrating op amp, a 5-bit DAC (used for offset cancellation of the integrating op amp), and two delay generators

The 5-bit DAC is of the current scaling type where a binary array of cascaded current sources is used to sink/source current into a temperature independent resistor (see above discussion). The full-scale range of the DAC is 20 mV (nominally). Of the 5 bits, 4 are used to control the magnitude of the current with the 5^{th} bit determining polarity.

The core amplifier used in the integrator also employs a two-stage topology. The first stage is a folded cascode followed by a class-AB output stage. The gain-bandwidth product of the op amp is 50 MHz and it can sink/source currents of several milli-amps.

A more detailed report on the performance of all **PSD8C** circuits will be provided in the next year's final report.

The layout of **PSD8C** (nearing completion) as of Aug 20, 2007 is presented on the next page in Fig. 5. We anticipate submitting the IC for fabrication in the near future. We are optimistic that we will make the October fabrication run. The area of the die is estimated at 2.8 mm by 5.8 mm. The anticipated cost of the IC (40 parts) is around $17,000. Total power consumption should not exceed 150 mW.

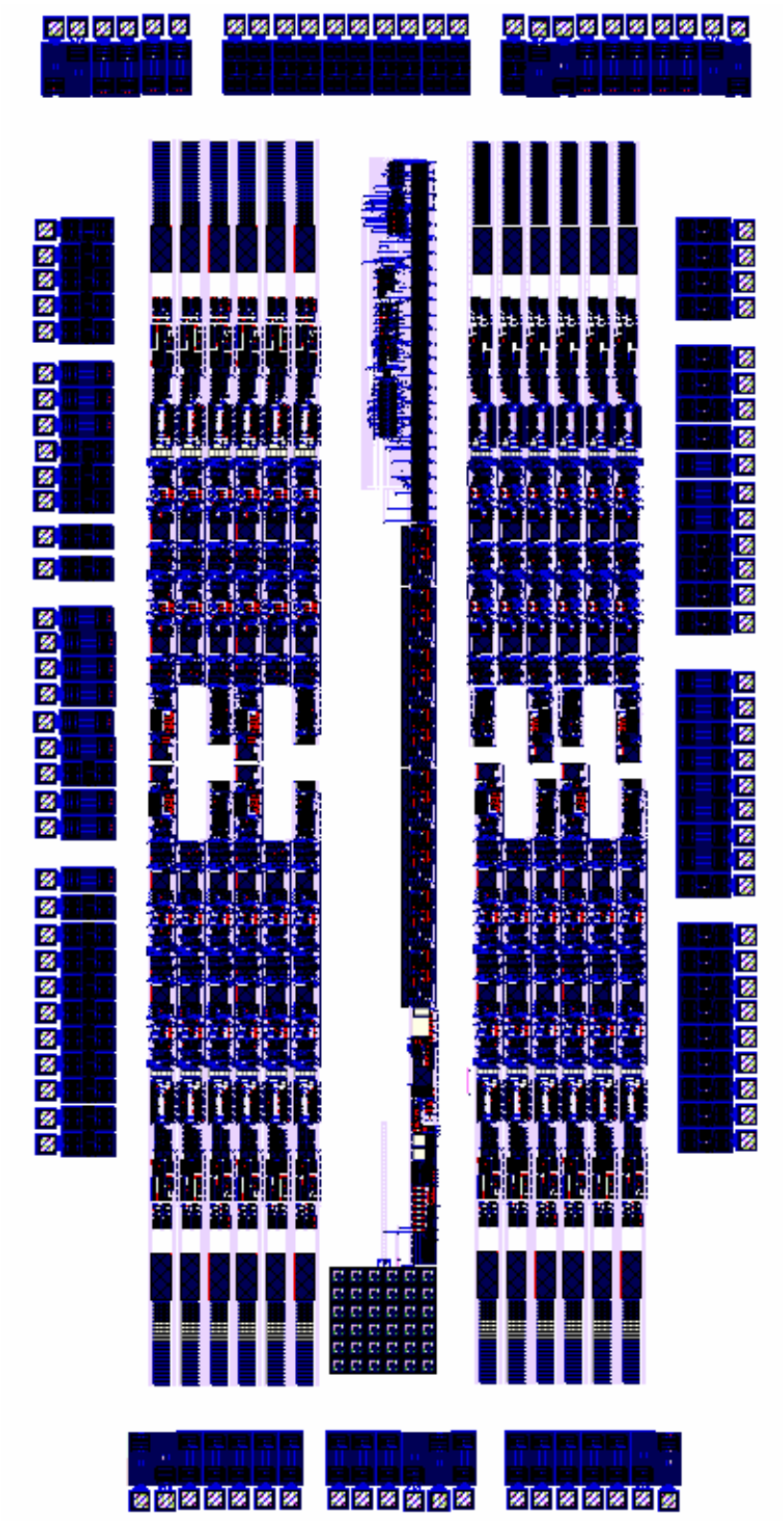

Fig. 5: PSD8C IC layout (under construction!)