Design of a RAM Buffer for Multi-channel Integrated Circuits Used in the Detection of Ionizing Radiation

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ABSTRACT

DESIGN OF A RAM BUFFER FOR MULTI-CHANNEL INTEGRATED CIRCUITS USED IN THE DETECTION OF IONIZING RADIATION

by

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Advisor: Dr. George L Engel

The thesis presents the design, simulation, and layout of a 32 location by 18-bit static Random Access Memory (SRAM). The RAM buffer is intended for use in a family of integrated circuits (ICs) that are being designed by the IC Design Research Laboratory at Southern Illinois University Edwardsville for use in science experiments where the detection of ionizing radiation is needed.

The RAM buffer described will be integrated along with a 12-bit, 2 MSample/sec analog-to-digital converter onto a custom micro-chip, previously designed by our research group, called PSD8C. PSD8C is an eight channel integrated circuit, with analog pulse train outputs, which is to be used in nuclear physics experiments where particle identification is required. Storing the data in a digital format on-chip before transmittal to a host computer over an 'I2C-like' bus will result in improved system performance.

The memory design described herein uses a compact standard six-transistor memory cell, and a fast pseudo-NMOS address decoder. The RAM is small, occupying an area of only 543 μm x 394 μm. The RAM layout was performed in a manner that it makes it easy to enlarge for inclusion in future designs. The SRAM will be fabricated in the AMIS 0.5-micron n-well process (C5N). This work was initiated by the heavy-ion nuclear chemistry and physics group at Washington University in Saint Louis but is currently funded by NSF Grant #06118996.

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CHAPTER 1

INTRODUCTION

Background and Significance of Research

The IC Design Research Laboratory at Southern Illinois University Edwardsville (SIUE) is part of an interuniversity collaboration which has as its long-term aim the development of a suite of multi-channel custom integrated circuits (ICs) suitable for use in a wide variety of nuclear physics experiments where the detection of ionizing radiation is needed. The greater collaboration includes researchers at Washington University in Saint Louis, Western Michigan University, Indiana University, and Michigan State University.

Frequently in nuclear physics experiments the type of radiation incident on the detector must be classified, the energy of the particle must be determined, and the position of interaction within the detector must be accurately estimated. A typical array of silicon strip detectors used in nuclear physics experiments is pictured in Figure 1.1.

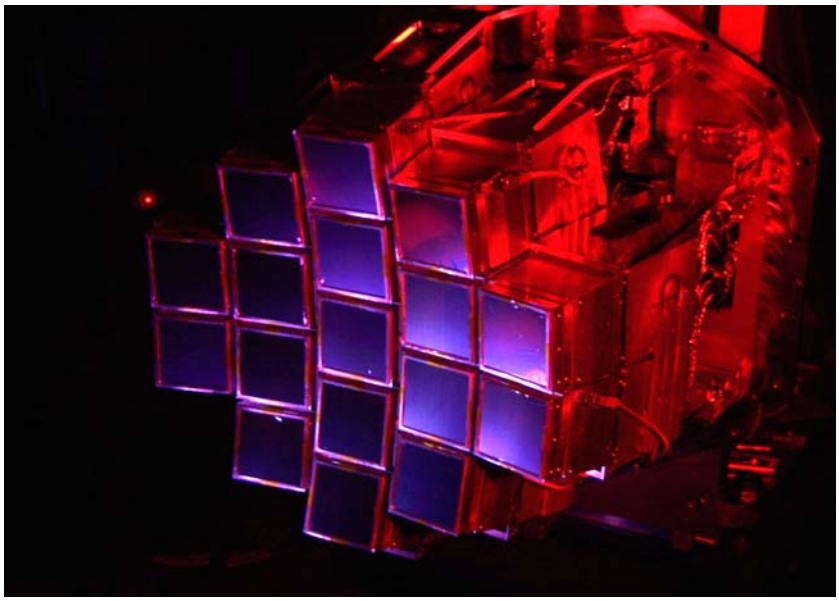

Figure 1.1 An array of silicon strip detectors

The ICs that have already been designed and fabricated, as well as those currently under development, contain analog electronics which make the accomplishment of the scientific objectives enumerated above possible. It should be note that in Figure 1.1 each of the 17 (blue-colored) panels actually contains 32 detectors (16 in the horizontal and 16 in the vertical direction). Therefore, the electronics servicing the array in Figure 1.1 must be able to support 544 independent channels. A Si strip detector is a reversed-biased p-n junction. Incident radiation impinging on the detector releases a packet of electron-hole pairs. The size of the packet is proportional to the energy of the incident radiation.

Preliminary work on the ICs began in the year 2000 [Gan:00]. Initially the development was funded through support from the nuclear reactions group in the Department of Chemistry at Washington University in Saint Louis; however, because of the success of the project over the years, the work is now funded by the National Science Foundation (NSF Grant #06118996).

The reasons why the collaboration became interested in developing a family of custom multi-channel integrated circuits include: (1) the need for high density (hundreds if not thousands of independent channels) signal processing in low- and intermediate-energy nuclear physics community is widespread, (2) no commercial chip was found to do exactly what the researchers wanted, and (3) the scientists deemed it necessary for the "experi-menter" to be in the "designer's seat".

While the initial intent was to use the chips in nuclear physics experiments, we are now proposing to create a mini-center that will work on different aspects of nuclear threat detec-tion systems for the United States Department of Homeland Security. One aspect of the most recent proposal to NSF, concerns the development of a suite of analog ASICs (based on the work we have completed to date) for use with scintillation (Sc) and semiconductor solid-state

(SS) detectors. Standard signal processing components will be developed in addition to novel elements including single, few, and "round-robin" charge integrators, chip-level filtering and on-chip digitization. The latter is related to the topic of this thesis.

Our goal is to achieve a great simplification in digital-signal processing (DSP) by doing as much as possible in the front-end CMOS ASIC (Application Specific Integrated Circuit). Compact low-power CMOS digitizers are slow. A full-blown DSP-based approach would require a digitizer with 14-bit resolution and a sample rate in excess of 100 MSamples/sec. We plan to overcome this limitation by using one of two analog schemes (one each for Sc and SS detectors) to reduce the time dependence of the signal to a few analog voltages that can be sampled and **subsequently digitized on-chip**. We refer to the economical (low power, size, and money) strategy as Analog-Assisted Digital Signal Processing (AA-DSP).

It is the on-chip digitization of these analog output signals, and in particular the storage of the digitized data, which is the focus of this Master's Thesis. In the following section, we briefly discuss in more detail the integrated circuits that we *have* developed, *are* developing, and *will* develop over the next few years. In the subsequent section, we will enumerate the advantages of digitizing the analog signals on-chip as opposed to bringing the analog signals off-chip for digitization and the need for a small static RAM (Random Access Memory) to store the digitized results.

Past, Present, and Future Work

A significant focus of the proposed mini-center will be on the design of low-noise, high-performance analog integrated circuits for use with detectors for ionizing radiation. This work will build on our past and ongoing efforts. The principal example of the former is our

HINP16C chip [Eng:07a, Sad:02]. An example of the latter is our current project to develop an eight-channel Pulse-Shape Discrimination chip (PSD8C) [Eng:07b, Hal:07, Pro:07].

In the near future, we plan to integrate an on-chip ADC onto the PSD8C chip. The digitized data will be stored in a small on-chip RAM before being transmitted back to a host computer. It is the design of this data storage RAM which is the focus of this thesis. The PSD project will then be extended in the future to an AA-DSP scheme with information compaction, as well as the digitization, done on the front-end chip. The former is necessary as the on-chip ADC will be relatively slow (a few Msamples/sec). We now discuss each of the three chips (HINP16C, PSD8C, and AA-DSP) in more detail.

Our collaboration has successfully developed and fabricated the HINP16C chip, now in wide use. In addition to our own group, groups at the Western Michigan University, Indiana University, Oak ridge National Laboratory (ORNL), and National Superconducting Cyclotron laboratory (NSCL) use this chip. Nuclear Physics (NP) groups at Louisiana State and Florida State are building programs around this chip.

The HINP16C ASIC, based on prior work by Spieler and Britton [Spi:05, Sim:95] is described in detail in [Eng:07a, Sad:02] and its integration into a large-scale system is presented in [Wal:07]. A sampling of the science (from our group) using this chip, can be found in [Cha:07b,Cha:07c]. The HINP16C chip produces sparsified pulse trains for both linear (pulse height) and timing (relative to an external reference) and allows the use of one of two internal charge sensitive amplifiers or an external amplifier. A block diagram for a single channel from the HINP16C chip is depicted in Figure 1.2.

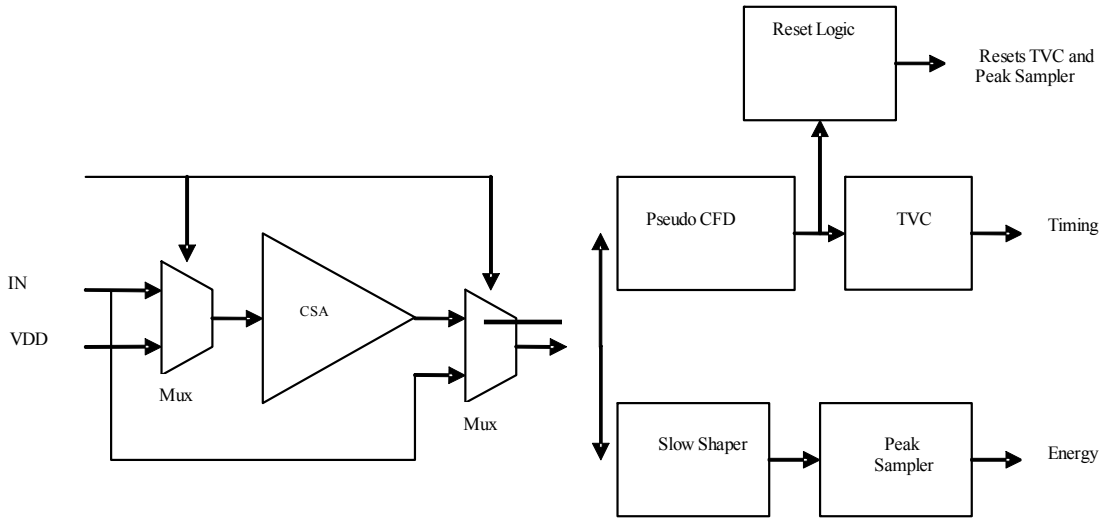

Figure 1.2 Block diagram of single channel from HINP16C chip

A shaper and peak detector are implemented on the linear branch and a pseudo constant-fraction discriminator and time-to-voltage converter are implemented on the logic/timing branch. The internal plus external gain options and the preparation of both pulse height and timing pulse trains makes the HINP16 well-suited for many applications. This chip, however, has no pulse-shape analysis capability and ***relies on an external ADC*** (Analog-to-Digital Converter). The chip, shown in Figure 1.3 was fabricated in the AMI 0.5 μm n-well (C5N) process available through MOSIS (MOS Implementation Services). It is a revised/improved version of the original HINP16C IC. The chip returned from fabrication in January 2008 and will likely be used in experiments before the end of this year.

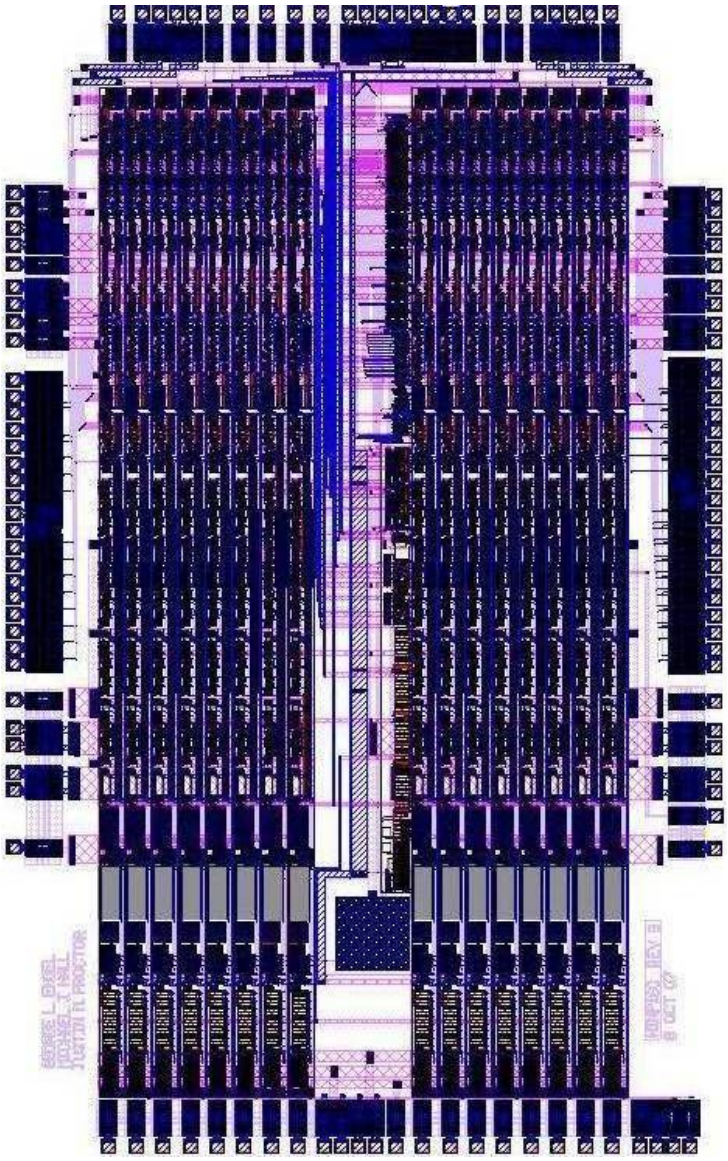

Figure 1.3 Revised HINP16C layout

The "Timing" and "Energy" outputs in Figure 1.2 are analog pulse trains which are currently digitized by an off-chip ADC. The ADC described in a companion thesis [Das:08] could be integrated into a future generation HINP16C chip. An on-chip ADC for HINP16C is desirable for many reasons as we will discuss in the following section of this thesis. If an on-chip ADC is used, however, the data must be stored on-chip until the time that it can be transmitted back to a host computer.

Signal-shape analysis capability (not possible with the HINP16C chip) is desirable in order to distinguish γ-rays, n's, α-particles from cosmic or other background events (and thus reduce false positives) from scintillator-based systems. The shape analysis is also needed for tracking applications in large volume Ge or any size CZT detector . A now nearly completed NSF-funded project moved the project into the PSD realm for scintillators. An eight channel chip we call PSD8C, described in detail in [Hal:07] and [Pro:07], makes use of CMOS technology to provide: a) integration of several regions of the analog signal, b) time-to-amplitude conversion, and c) generates pulse streams from each of the above for an off-chip ADC.

PSD8C is to be used in nuclear physics experiments where particle identification, total pulse height, and relative timing information are needed. The design employs a technique known as pulse shape discrimination (PSD) to classify the incident radiation. Each of the eight channels is composed of a time-to-voltage converter (TVC) with two time ranges (0.5 μsec, 2 μsec) and three sub-channels. Each of the sub-channels consists of a gated integrator with eight programmable charging rates and an externally programmable gate generator that defines the start (with four time ranges) and width (with four time ranges) of the gate relative to an external discriminator signal. The chip also supports 3 triggering modes.

The IC produces four sparsified analog pulse trains (3 integrator outputs and 1 TVC output) with synchronized addresses for off-chip digitization with a pipelined ADC. PSD8C, with two bias modes occupies an area of approximately 2.8 mm x 5.7 mm and has an estimated power dissipation of 135 mW in the high-bias mode. The PSD8C chip, shown in Figure 1.4 was fabricated in a 0.5 μm technology (AMIS C5N) available through MOSIS (MOS Implementation Services). The chip returned from fabrication in May 2008 and is currently undergoing testing and performance characterization.

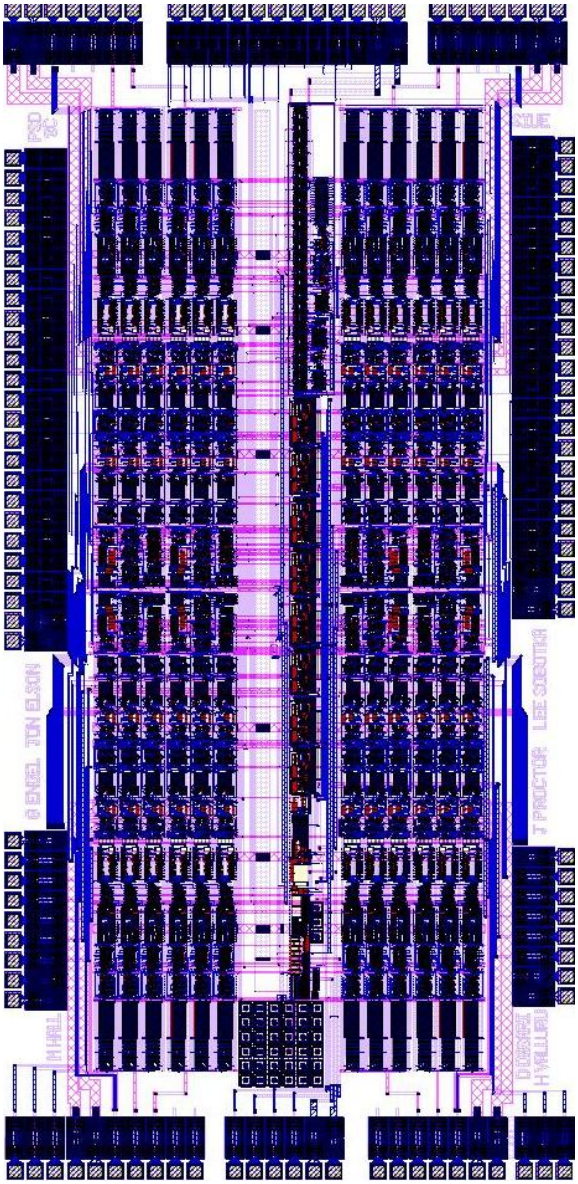

Figure 1.4 PSD8C layout

While in basic science experiments, there is no problem with coupling this chip with conventional power hungry (VME) ADCs, the same cannot be said of homeland security applications. We imagine an array of scintillators (e.g. CsI(Na), but perhaps ultimately a LaHalide) attached to the new generation of compact photomultiplier tubes (PMTs). The chip we just described, with a single ADC and data storage RAM of the type described in this thesis integrated into the chip, along with a new generation of compact low-power CFD's

would provide a compact, low-power and easily portable system suitable for homeland security applications

Adding an on-chip ADC to the existing PSD8C chip is the first of two projects that we propose in order to fill one of the central aims for the proposed mini-center *i.e*. to extend the CMOS–ASIC capability into the realm of extracting ***full*** pulse-shapes. While it is true that traditional DSP accomplishes this, traditional DSP is not transportable to a high-density, front-end CMOS ASIC. This is due to its need for fast (> 100 MSampl/sec) many-bit digitizers (> 12 bits) in conventional DSP. In the second project, we propose to develop a technique that is more efficient in every regard than conventional DSP.

In principle, a signal waveform encodes for a small set of quantities that are truly important. These are the answers to the: "what" (particle type), "where" (x,y,z) and "when" (t) questions. Using a traditional DSP, the waveform is collected, digitized and stored over a long period of time. This digitization is an intensive operation that puts extreme demands on the downstream computation. Our proposed approach is to provide analog compaction on the front-end ASICs, analog storage of this information on the front-end ASIC, and then "slow" digitization with a single on-chip ADC. In short, the ultimate "front-end" objective of this proposal is to push the analog CMOS possibilities as far as they can go to aid and simplify DSP operations.

We call our design to accomplish this Analog-Assisted DSP (AA-DSP) and its logic is shown in Figure 1.5. This chip could be used to extract position information from a large segmented Ge or from pixilated CZT. This logic is an extension and improvement on that reported by Pullia et al. [Pul:00].

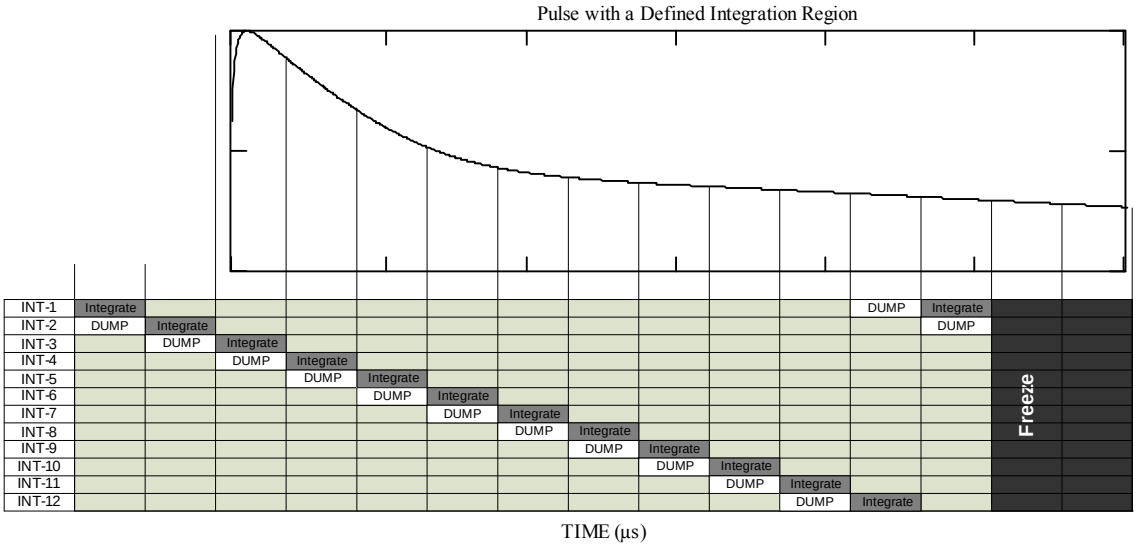

Figure 1.5 AA-DSP logic

Analog-assisted DSP is a mix between charge integration and traditional digital capture methods. It utilizes multiple analog "round-robin" charge integrators to integrate under each region of a pulse. Then using digital signal processing, the position of interaction in the detector, deposited energy, and timing information can be determined. In order to characterize a pulse, there will be, for example, 12 fast charge integrators and 12 slow charge integrators. The fast charge integrators are used to capture the fast rising portion of the pulse whereas the slow charge integrators are used to capture the slow decaying portion of the pulse [Hal:07].

The timing logic (CFD + TVC) and the two banks of round-robin "integrate and hold" circuits (*fast* and *slow*) are fed by one of several CSA options. The adjectives *fast* and *slow* refer to the duration of time that each integrator is gated on. For our initial simulations, the (individual) period of integration is 62.5 ns in the *fast* bank and 500 ns in the *slow* bank. Since this is a round-robin scheme, the 12 fast and slow charge integrators are continuously running. However, when a new pulse arrives, a counter is started which will stop the round-

robin integrators after 10 integrations have occurred past the arrival of the pulse [Hal:07]. The values of these integrators will then be held, digitized, stored in an on-chip data RAM, and then transmitted to a host for off-line analysis.

Need for On-Chip ADC and RAM

Cleary, all three multi-channel ICs discussed in the previous section could be enhanced by the addition of an on-chip ADC. The transmission of sensitive high-speed analog pulse trains to an off-chip VME ADC is a very difficult task. Low-level analog signals are easily corrupted. Moreover, even if the system is correctly designed, it is the nuclear physicists who set up and conduct the experiments. It is easy to degrade the performance of an analog system through improper grounding or shielding. The transmission of high-speed digital signals even over long distances is, on the other hand, relatively easy. Digital signals have high noise immunity.

Furthermore, VME ADCs are relatively expensive, large, and power-hungry. As described in an earlier section, it is important that systems proposed for use in security detection systems to be used by the Department of Homeland Security be compact and low-power. These attributes can only be achieved in an on-chip ADC. Since the ICs described in the previous section are all fairly large (15 mm^2 – 50 mm^2), the proposed ADC and companion RAM will increase the overall chip area by only 10 – 30%.

In the case of HINP16C since there are 16 channels and two analog pulse streams ("Energy" and "Time"), a 2 MSample/sec converter could complete the digitization of in a maximum of 16 μs. In addition to the ADC, a small 32 location memory is needed to store the results. Generally, only a small subset of the channels actually are impacted by radiation

and need to be read out so the digitization would take even less time, typically just a few microseconds. The resolution of the converter need not exceed 12 bits.

For the PSD8C chip where there are 8 channels and each channel consists of 3 sub-channels and a timing output per channel, the digitization could once again be completed in a maximum of 16 μs. Once again only small 32 location memory is needed to store the digitized values. Even for the AA-DSP chip with 8 channels the digitization could be completed in a maximum of 125 μs. Even in this case only around a 256 location memory is required to store the data.

To minimize the system-level interconnect, we propose to transmit the contents of the RAM storing the ADC results back to a host computer via a serial "I2C-like" interface. This greatly simplifies the system level design and in particular the design of mother-board and associated chip-boards.

The on-chip ADC will be integrated for the first time in a second generation PSD8C chip. The IC is expected to be fabricated and ready for field testing by December 2009. The ADC will then be used in the AA-DSP chip described in the previous section. While there are no immediate plans to integrate an on-chip ADC and on-chip storage RAM with HINP16C, this may well happen at some point in the future.

Object and Scope of Thesis

The object of this thesis is to describe the design of a RAM which can be used to store data from an on-chip ADC suitable for integration with a series of custom ASICs developed or currently under development by the IC design research laboratory at SIUE. The ASICs are intended for use in the detection of ionizing radiation both in instruments intended for

experiments in low- and intermediate-energy nuclear physics and (perhaps someday) in real-time homeland security nuclear threat detection systems.

Specifically, this thesis describes in detail a 32 location, 18-bit RAM that can be incorporated (along with an on-chip ADC) onto the PSD8C chip useful in applications where the type of radiation incident on the detector must be correctly classified. In the future, the RAM may be modified so that it may be included on an AA-DSP chip and perhaps on a revised HINP16C IC.

There are five chapters in this thesis. Brief descriptions of the ASICs which might benefit from the integration of an on-chip ADC and RAM were presented in this chapter In Chapter 2 we will discuss RAM architectures and discuss the difference between static (SRAM) and dynamic (DRAM) memories. READ and WRITE operations for a static RAM cell are discussed in detail. Chapter 3 presents the schematics and simulation results for the SRAM sub-circuits. In Chapter 4 we present the layout of the RAM along with electrical simulations using Cadence's Spectre® program on the extracted layout netlist which demonstrate correct operation of the RAM at several process corners, supply voltages, and temperature. Finally, Chapter 5 will give conclusions and discuss the future direction of this research work.

CHAPTER 2

RAM ARCHITECTURES

Background

In this chapter, an overview of how memories in general operate and different classifications of memory is presented [Che:02]. Memory elements form critical components in the implementation of CMOS systems. In many digital designs, large portions of the silicon area are dedicated to the storage of data and program instructions. Electronic memories are classified in different forms and styles. The details of which mainly depend on the specific application requiring the memory. The specifications include required memory size, time it takes to store the data, access pattern and the system requirements.

The basic unit for expressing the size of memory is *bits*. Usually the size is expressed in bytes, where a byte is equal to 8 bits, or its multiples like kilo *bytes* (Kbyte), *megabytes* (Mbyte), *gigabytes* (Gbyte) *etc*. Two bytes is generally referred to as a *word* and 4 bytes constitute a *long word*.

Figure 2.1 presents a timing diagram for a typical memory. The time taken to retrieve data from the memory is a called *read access time* and the time taken to write data in to the memory is called the *write access time*. The minimum time required between two successive read or write operations is referred to as the *cycle time*.

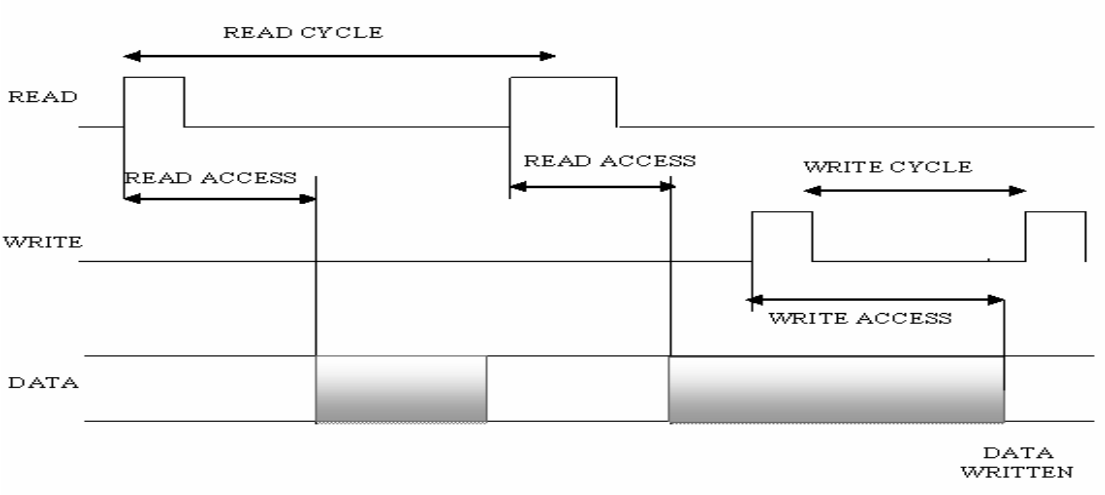

Figure 2.1 Memory timing definitions

Classification

Semiconductor memories are classified based on functionality, access patterns and storage mechanisms [Che:02]. They are divided into Read Only Memories (ROM), Read-Write Memories (RWM) and Non Volatile Read-Write Memories (NVRWM). The ROM belongs to the class of nonvolatile memories. It encodes information in the circuit topology *i.e.* by adding or removing transistors. Since this topology is hardwired, the data cannot be modified; it can only be read. Disconnection of the power supply from the device does not result in the loss of data. Nonvolatile read-write memories can perform read–write operations but will retain data even when power is removed. EPROM (Erasable Programmable Read Only Memory), E^2PROM (Electrically Erasable Programmable Read Only Memory) and Flash Memory come under this category.

Read-Write Memory

As the name suggests, these types of memories have both the read and write capabilities. They use active circuitry to store information. Therefore, data is lost when the power supply

is turned off to the memory. Read-Write memories are subdivided based on the access patterns. Based on the access patterns, memories are classified in to the following categories

- Random Access Memory
- Serial Access Memory
- Content Access Memory

The RAM acronym is used to describe Random Access Read-Write memories. Data can be accessed from a random location in any order. In a RAM, the data is stored either in flip-flops or in capacitors. Depending on which method is used, they are classified as either Static RAM (SRAM) or Dynamic RAM (DRAM) respectively. The SRAM retains data as long as power is applied to the circuit while the DRAM needs constant refreshing to account for the loss of charge on the capacitor storing the data.

In serial access memories, the data is accessed in a serial fashion. Serial memories like FIFOs (first in first out), LIFOs (last in first out), and a shift register array come under this category. Content Access Memories (CAMs0 use a word of data as a query and if it matches a data word in the memory then the MATCH flag is raised.

Figure 2.2 depicts a generic RAM circuit with just one row and one column. The row decoder is a 1 of (n-k) decoder while the column decoder is 1 of k decoder where k is less than n. One of the 2^{n-k} rows is accessed at a time. The bit lines normally run as complementary signals (bit and bit-bar). Sense amplifiers speed up the reading process. They are merely differential amplifiers which amplify the difference between the bit and the inverted bit (bit-bar) lines and push them to the supply rails. The memory required in this project is a SRAM.

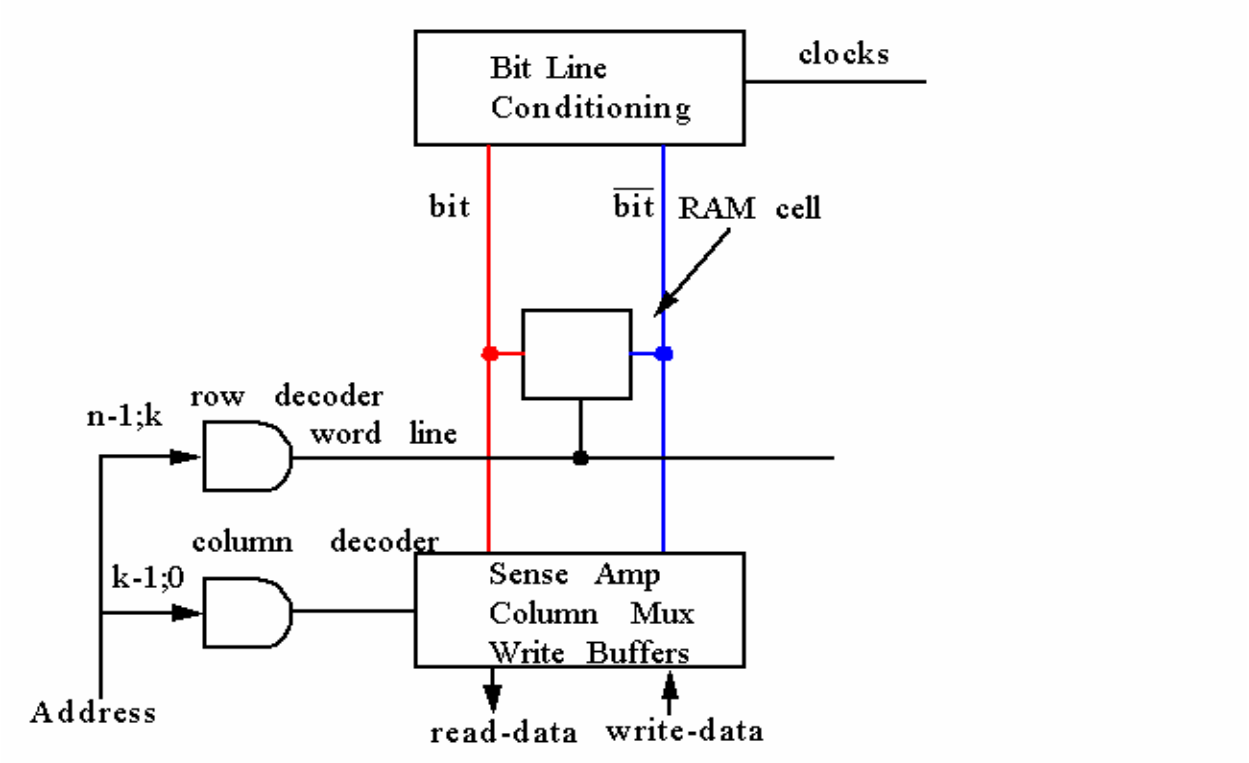

Figure 2.2 Generic RAM circuit

Static Random Access Memory (SRAM)

Figure 2.3 illustrates a widely-used six-transistor implementation of a SRAM cell. Each cell is used to represent a single bit [Wes:93]. Access to each cell is enabled by a word line and it controls the two pass transistors M_5 and M_6. There are two bit lines transferring both the stored signal (BL) and its inverse (BLbar). Providing both polarities improves noise margin during both read and write operations.

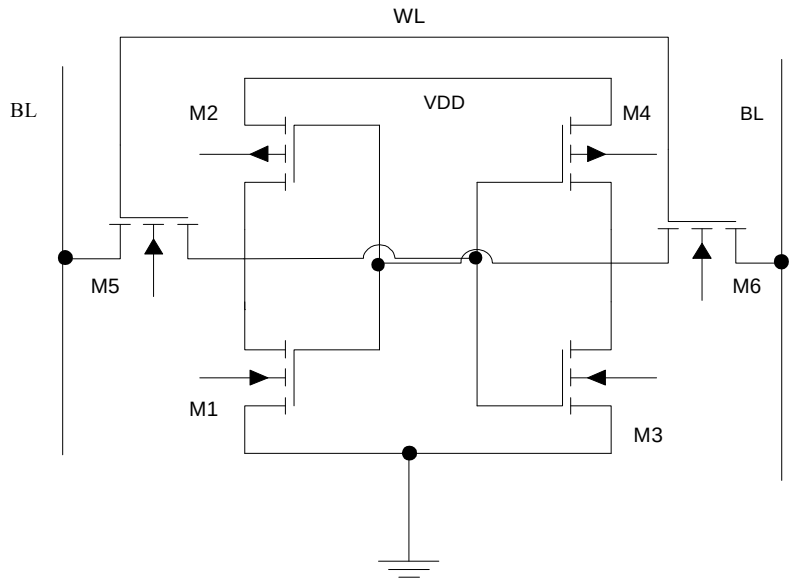

Figure 2.3 SRAM cell

Figure 2.4 shows an alternative implementation of the SRAM cell in which the p transistors are replaced with two resistors. The value of the resistors is usually high so that to prevent the leakage from changing value stored in the RAM. Integrated resistors occupy a lot of area on a chip so the implementation in Figure 2.3 where a pull-up FET is used is generally preferred.

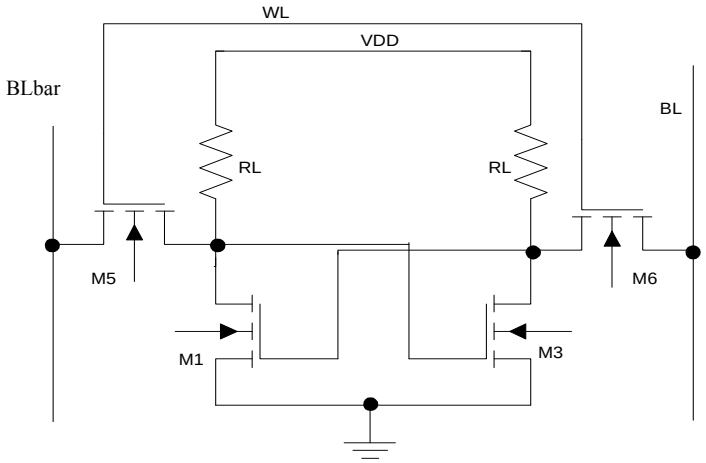

Figure 2.4 Resistive load SRAM cell

SRAM Read Operation

In the 6-transistor circuit depicted in Figure 2.3 during the read operation, one node of the RAM cell pulls the bit line up through the access transistor and the PFET-load and another node pulls the bit line down through the pass transistor and NFET load. This is further illustrated in Figure 2.5. Since NFETs are poor in passing a '1' and the p-transistors are generally made small, the RAM circuit design of Figure 2.3 is based on pulling the bit line from high to low. During a read operation both bit lines (BL and BLbar) are precharged to V_{DD}. The word line (WL) is initially help low. Assume a '1' is stored at the Q output *i.e.* the drain of NFET M_6. If the word line transitions high, it enables both transistors M_5 and M_6.

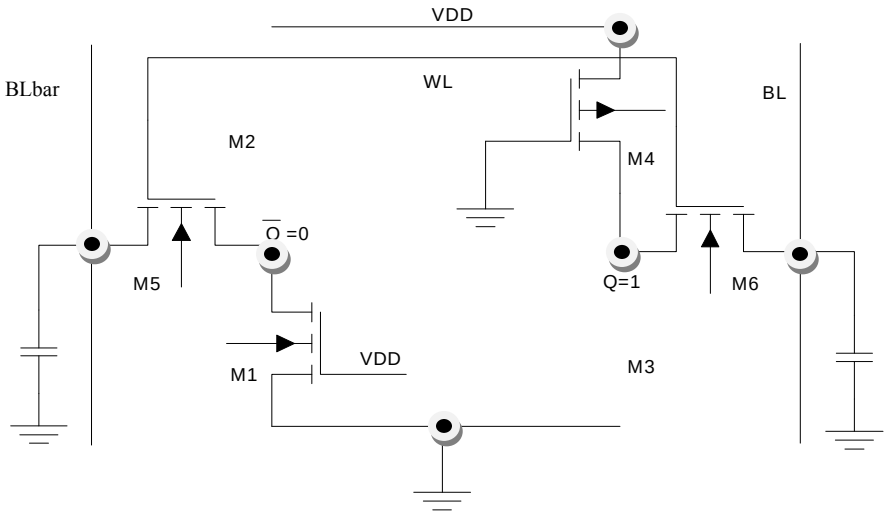

Figure 2.5 Simplified SRAM cell during READ operation

Figure 2.5 shows the simplified model of the SRAM cell during READ operation. Since Q| =1, Q-bar=0 are assumed, transistors M_3 and M_2 are "OFF" while M_1 and M_4 are "ON". During the read operation, the values of Q and Q-bar are transferred to the bit lines BL and BLbar. The bit line is left at its precharge value while the BL-bar line is discharged through

FETs M_5 and M_1. The transistors must be sized very carefully to avoid writing into the RAM instead of reading from the RAM.

As we have just demonstrated, the process of reading data from a cell can destroy its contents. This is known as a *Destructive Read* or *Read Upset* operation and will occur when the cell is selected and both bit lines are at logic 0. Hence, there is a need for need a pre-charge circuit. Transistors M_5 and M_1 should be sized as small as possible to result in a slow discharge of the bit–bar line. In general for larger memories the difference between the bit and bit-bar lines is amplified by the using a sense amplifier. This will accelerate the reading process.

Initially upon the rise of the WL line, the intermediate node between the two NMOS transistors Q-bar is pulled up towards the precharge value of the BL-bar line. The resistance of M_5 should be larger than that associated with M_1 to prevent flipping of the cell. The ratio of sizes of M_5 and M_1 is important for correct read and write operation.

SRAM Write Operation

Assume initially that a 1 is stored in the cell (Q = 1). A 0 is written in the cell by setting the bit-bar line to 1 and bit line 0 which is identical to applying a reset pulse to an SR latch. The SRAM cell during a WRITE operation is depicted in Figure 2.6.

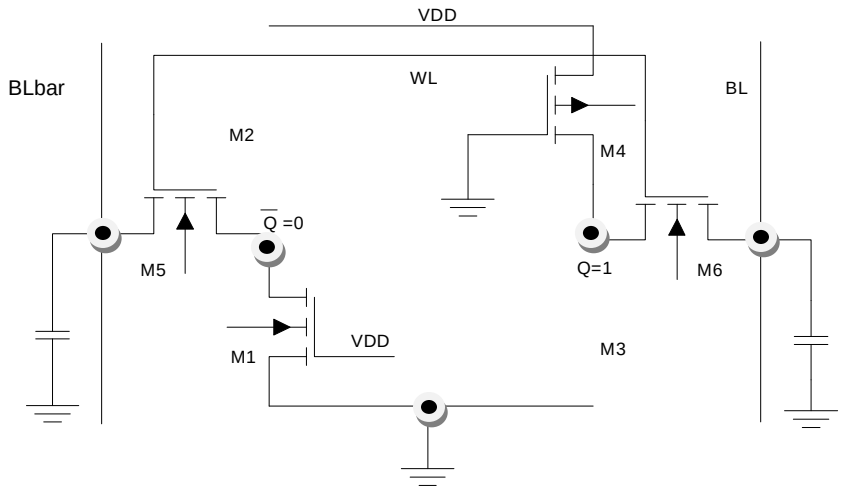

Figure 2.6 Simplified SRAM cell during WRITE operation

Precharge Circuit

The precharge circuit is a bit line pull-up circuit which can use either PFETs or NFETs. When one uses NFETs in the pull-up circuit, the bit lines are precharged to the supply voltage minus the threshold voltage of the NFETs. This improves the speed of the RAM access. The NFET load transistors pull up the bit lines statically. When the word line is asserted, the bit line being pulled down by the RAM cell falls to a value that is a function of pull-up size, the pass-transistor size and the RAM inverter pull-down size. At the same time the pull-up must not be able to flip the RAM cell.

Figure 2.7 illustrates the equivalent of the pull-down circuit during read operation. Voltage V_1 must be above the input threshold of the inverters in RAM. The value of V_1 is the result of the resistor divider action between the pass transistor and the RAM cell pull-down.

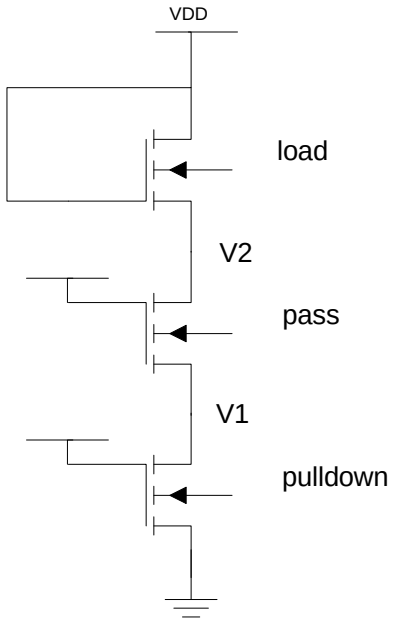

Figure 2.7 Pull down circuit

The voltage V_2 must be amplified by the bit line capacitance. The voltage V_2 is given by

$$V_2 := (Vdd - V_{TN})\left(1 - \sqrt{\frac{1}{1 - \frac{\beta_{pullup}}{\beta_{driver\_eff}}}}\right)$$

Where β_{pullup} is the gain of load and β_{driver_eff} is the gain of the combination of the pass and pull-down transistor in series. V_1 is roughly given by

$$V_1 := V_2 \cdot \frac{\beta_{pass}}{\beta_{pass} + \beta_{pulldown}}$$

The voltage V_1 is generally kept approximately at 0.5V-1V.

Sense Amplifiers

Sense amplifiers play a major role in the performance and functionality of memory circuits. As semiconductor memories become large, they suffer from large capacitance on the bit lines. Hence, in order to accelerate the read operation sense amplifiers are used. Sense

amplifiers are merely differential amplifiers which amplify the difference between the bit lines and push them to the supply rails. The differential approach has an advantage over the single ended approach because of high CMRR (Common Mode Rejection Ratio). The sense amplifier rejects the noise equally injected in to the inputs. The differential approach can be applicable to SRAM's only as they provide differential outputs. There are different types of sense amplifiers:

1. Voltage Sense Amplifiers
2. Semi-Latch Sense Amplifiers
3. Full-Latch Sense Amplifiers
4. Current Sense Amplifiers

Figure 2.8 shows the most basic voltage differential sense amplifier which is nothing but a Miller OTA (Operational Transconductance Amplifier). The bit and the bit-bar lines are heavily loaded and are driven by the SRAM cells. The swing on the bit lines is very small. The inputs are fed to the input of M_1 and M_2. M_3 and M4 form a current mirror and the amplifier is enabled by a Sense Enable (SE) signal. Initially, the inputs are precharged and made equal to a common value, while SE is made low disabling the sensing circuit. Once the read operation is initiated, the voltage one of the bit lines drop. SE is enabled when a sufficient differential signal has been established, and the amplifier evaluates.

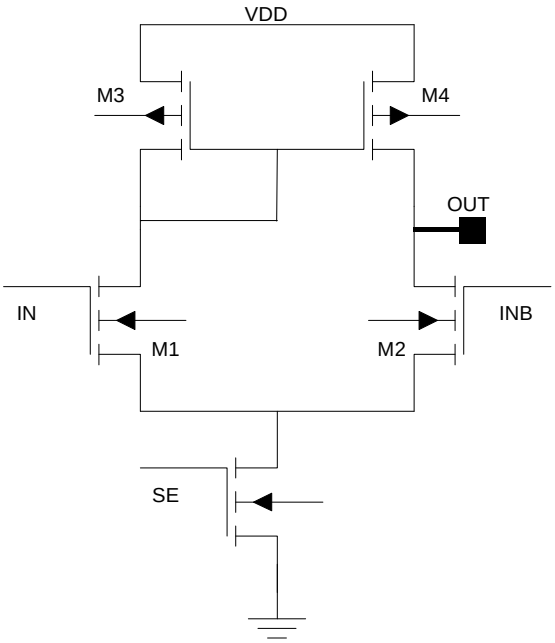

Figure 2.8 Miller OTA

Figure 2.9, 2.10, 2.11 shows a semi-latch, full-latch and current sense amplifiers respectively.

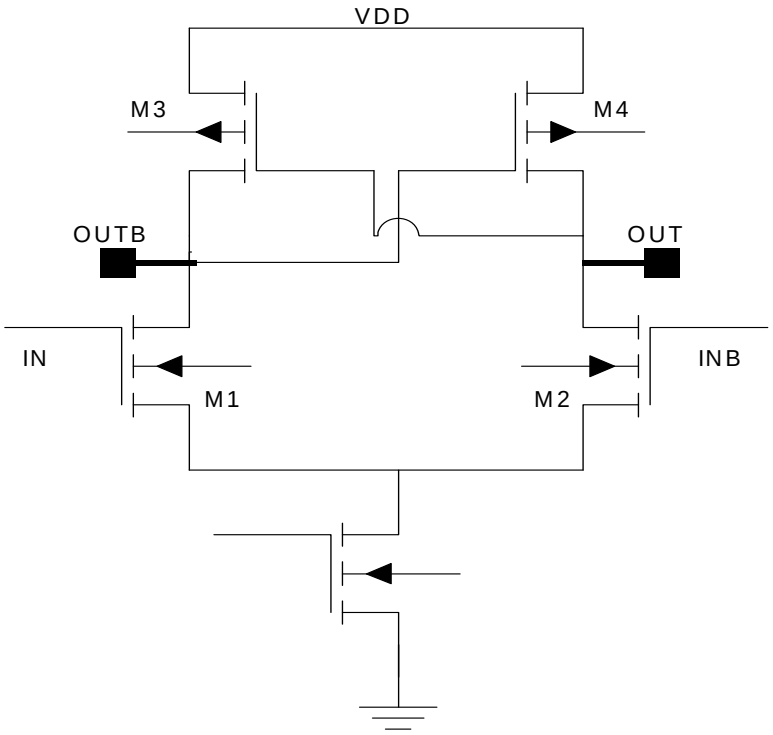

Figure 2.9 Semi-latch sense amplifier

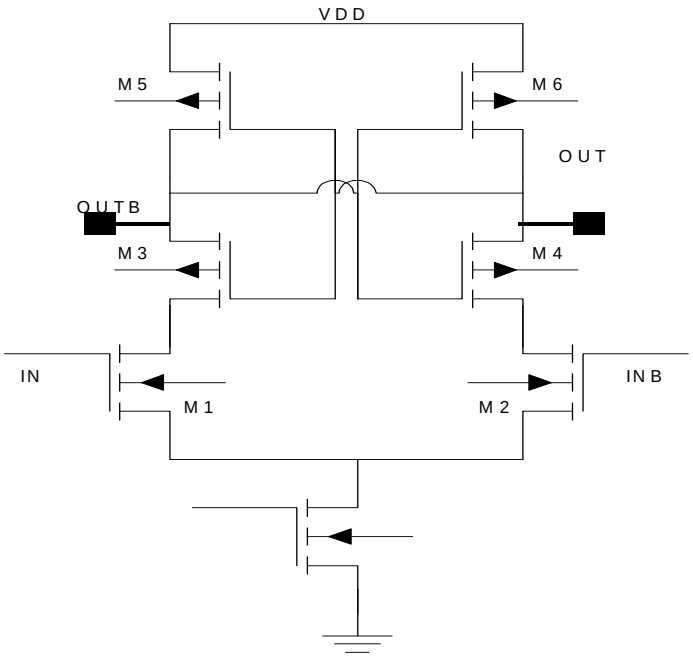

Figure 2.10 Full-latch sense amplifier

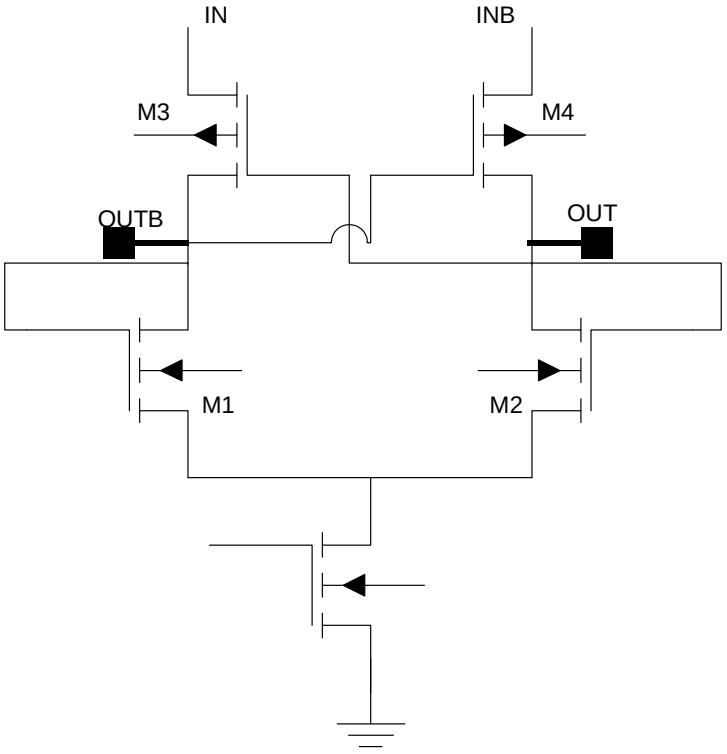

Figure 2.11 Current sense amplifier

The voltage sense amplifier is a stable sense amplifier. The semi-latch is improved version of the voltage sense amplifier. The full-latch sense amplifier is faster than the other two. The current sense amplifier is the fastest but has a disadvantage of high power consumption. Sense amplifiers can be cross-coupled (positive feedback) to increase speed.

Dynamic Random Access Memory

The resistors in the resistive load SRAM cell replenish the charge lost due to the leakage currents. One option is to eliminate these resistors and just account for the loss of the charge. This is done in the implementation of the Dynamic RAM (DRAM). The most generally used DRAM cell is a three-transistor cell with a capacitor.

Figure 2.12 shows the three-transistor implementation of the DRAM cell. The cell is written by placing data on the BL1 line, and this value is stored as charge on the capacitor. The BL2 line is precharged to V_{DD} or (V_{DD}-V_{TN}). The storage transistor M_2 is either ON or OFF depending on the stored value. The series combination of M_2 and M_3 pulls BL2 low when a '1' is stored otherwise it stays at V_{DD}.

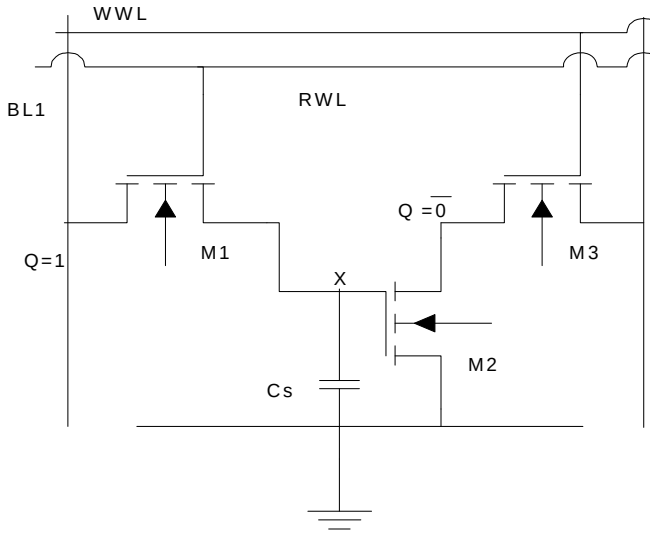

Figure 2.12 DRAM

The cell is inverting *i.e.* the inverse of the written bit is sensed, and the most common method to refresh the cell is to put the inverse bit on the BL1 line and assert WWL.

The advantages of the DRAM over the SRAM are

- Less Area
- No constraints on the device ratio
- The read operation is non-destructive.
- The storage capacitance is nothing but the gate capacitance of the storage device.

Another implementation of the Dynamic RAM is a one-transistor DRAM. Figure 2.13 depicts the one-transistor DRAM design.

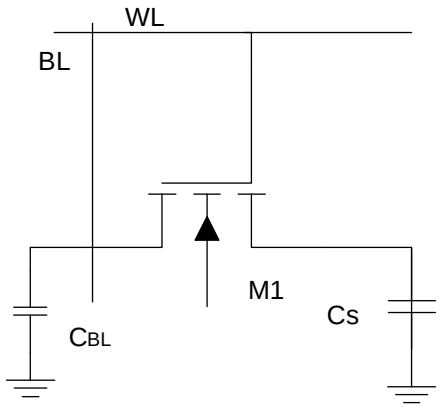

Figure 2.13 1T DRAM cell

During a write cycle, the data to be written is placed on the bit line and the charge in the cell capacitor is changed depending on the data bit. During the read process the bit lines are precharged to a voltage and the word line is asserted. Charge redistribution takes place between the bit line capacitance and the storage capacitance. This results in the change in the voltage levels of the bit line.

CHAPTER 3

RAM SCHEMATIC AND SIMULATIONS

The RAM required in this project is a 32 X 18 static RAM where 32 is the number of locations and 18 is number of bits per location. The process used is the AMI 0.5µm process (C5N). This process supports two poly layers and three metal layers. The minimum transistor length that can be used is 0.6µm.

The reason why the RAM has 32 locations is because the PSD8C chip has 8 channels and each channel contains 3 sub-channels. This means that there are 24 analog voltages that must be digitized by the on-chip ADC. Moreover, each of the 8 channels has a TVC (Time-to-Voltage-Converter) output that must also be digitized. Therefore a total of 32 analog voltages will be digitized (12-bit resolution) when the on-chip ADC and buffer RAM are integrated onto the PSD8C chip.

The width of 18 bits arises from the fact that it takes 3 bits to encode the 8 possible channel addresses. An additional 2 bits is required to encode the 3 possible sub-channel addresses. We must store the channel address, the sub-channel address, and the associated 12-bit data word. While this implies a 17-bit wide memory, one additional bit was added since it is possible that PSD8C might be extended to 16 channels in the future.

SRAM Cell Used in This Design

The basic SRAM cell used in the project is the 6-transistor version described in the previous chapter. Figure 3.1 shows the implemented six-transistor SRAM cell design.

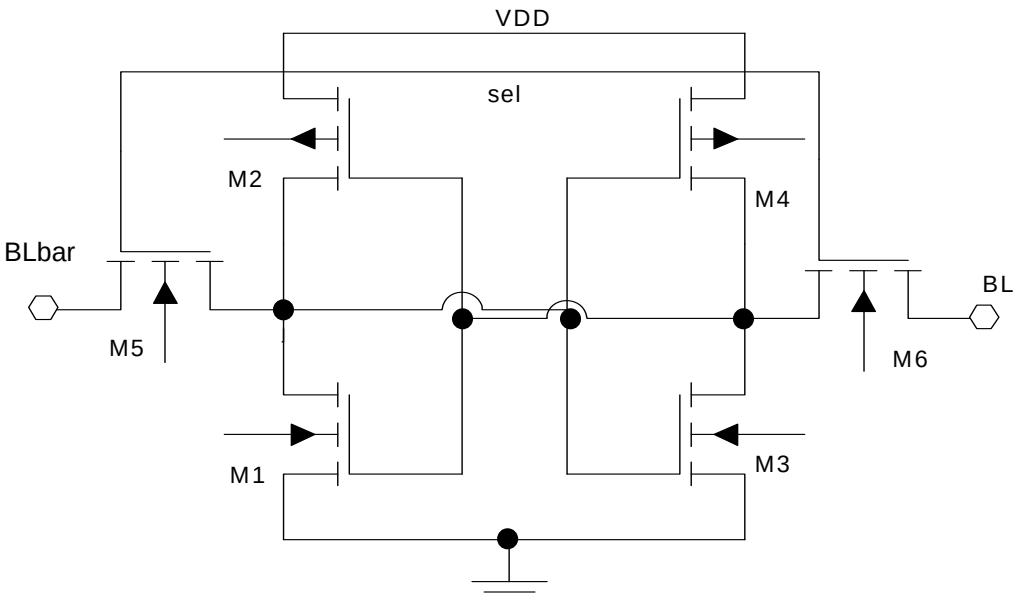

Figure 3.1 SRAM cell schematic

The RAM cell is sized to be as small as possible. The inverters in the RAM schematic have minimum length of 0.6 μm. The pass transistors act like switches and are minimum size. As the minimum width that can be allowed in layout is 0.9 μm, the W/L ratio of the pass transistors is 0.9 μm/0.9 μm. The sizing of the transistors was done carefully that so as not to allow any read upsets. It is important that transistor M_5 be 'weaker' (i.e. smaller W/L ratio) than transistor M_1.

Precharge Circuit

For the read operation of the RAM cell, the bit lines have to be precharged to a voltage near V_{DD}. Figure 3.2 illustrated the precharge circuit implemented. NFETs are used (as opposed to PFETS) as the pull-up transistors. This has the added advantage of improving the speed of the SRAM. Rather than pulling the bit and bit-bar lines all the way up to V_{DD}, the lines are pre-charged to ($V_{DD} - V_{TN}$). The transistor sizes are given in Table 3.1

REF	W(μm)	L(μm)	M
M1-M4	1.2	0.6	1
M5,M6	0.9	0.9	1

Table 3.1 Transistor sizes in RAM cell

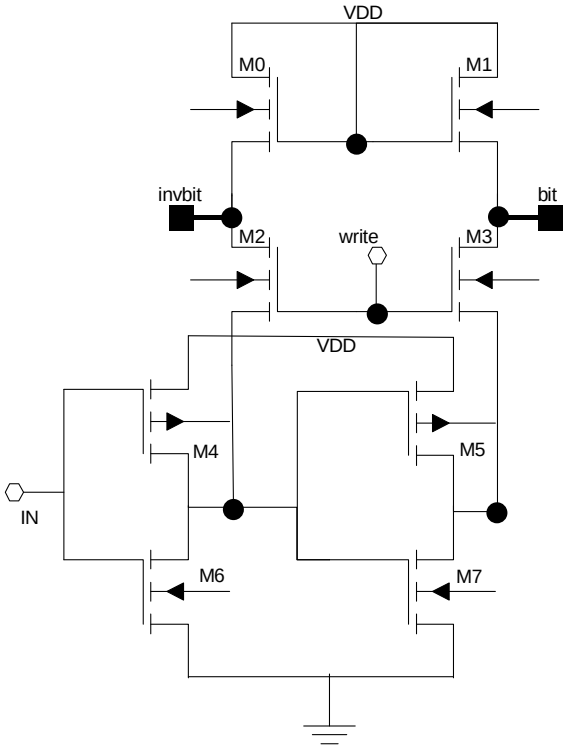

Figure 3.2 SRAM precharge schematic

Transistors M_2 and M_3 (in Figure 3.2) act as switches through which input bits are written onto the bit and bit-bar lines. The important part of sizing is sizing the pull-up transistors M_0

and M_1. The sizing of which is discussed in the previous chapter. There is a large capacitance on the bit lines which need to be discharged through the switches M_2 and M_3 and the NFETs of the inverters. So the sizing of the transistors is done so the resistance of the FETS is low enough to discharge the large bit-line capacitance quickly. Table 3.2 gives the transistor sizes of the RAM precharge circuit.

REF	W(μm)	L(μm)	M
M0-M1	0.9	1.8	1
M2,M3,M6,M7	3.6	0.6	1
M4,M5	4.8	0.6	1

Table 3.2 Transistor sizes in RAM precharge circuit

The inverters in the precharge circuit are designed so that when the input and output are connected they settle closer to V_{DD} /2. Figure 3.3 gives the test circuit for the inverter in the above mentioned case of the inverters, and the waveform in Figure 3.4 shows the output settling to 2.28V which is approximately equal to $V_{DD}/2$.

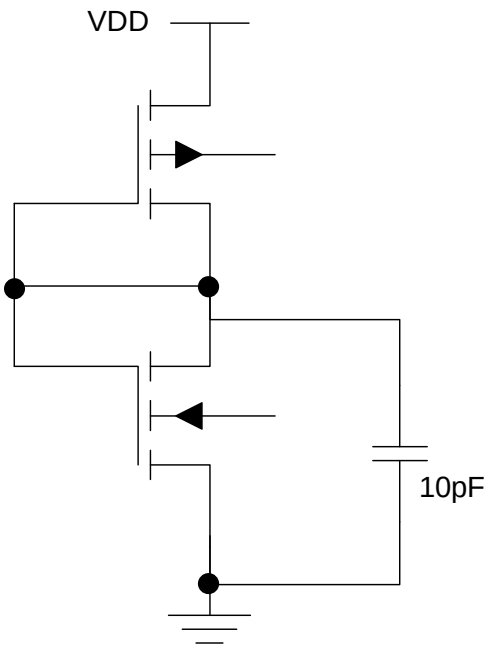

Figure 3.3 Inverter in precharge circuit

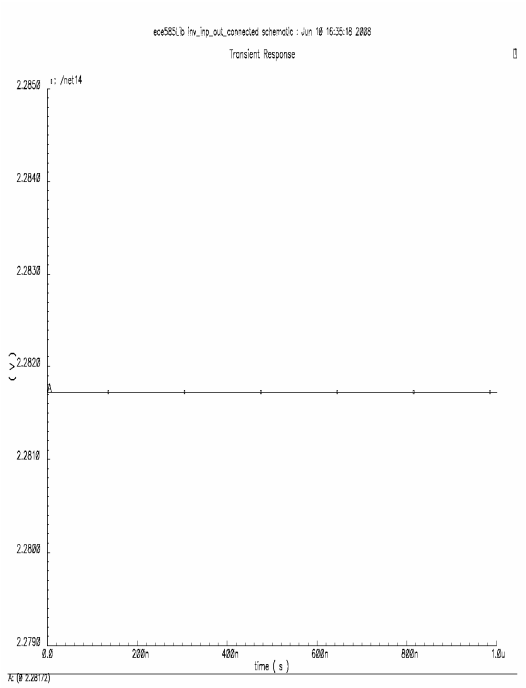

Figure 3.4 Output waveform of inverter in precharge circuit

Figure 3.5 shows the precharge circuit in a simplified form which helps convey the functions of the transistors.

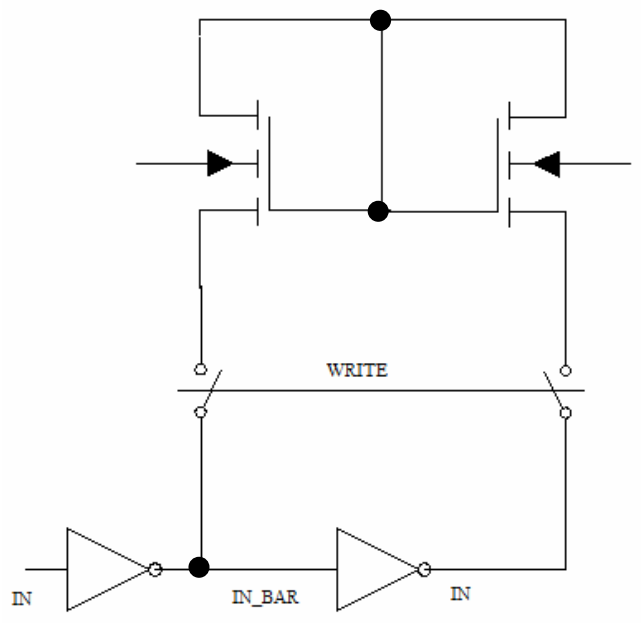

Figure 3.5 Simplified precharge circuit

Decoder

As there are 32 locations in the RAM the address decoder designed is a 5 x 32 decoder. For example the 0 and 31 locations are enabled by the following logic functions

$D0=\overline{A0}\,\overline{A1}\,\overline{A2}\,\overline{A3}\,\overline{A4}$ and $D31=A0A1A2A3A4$

which can be represented by use of 5-input NAND gates but it slows down the decoding process (NFETS are inherently faster). The functions can also be implemented as

$D0=\overline{A0+A1+A2+A3+A4}$ and $D31=\overline{\overline{A0}+\overline{A1}+\overline{A2}+\overline{A3}+\overline{A4}}$ which can be implemented by using a NOR gate. The normal fully complementary NOR gate occupies a large area and is slow, hence our decoder uses pseudo-NMOS NOR gates. Figure 3.6 illustrates the implementation of a pseudo-NMOS NOR gate.

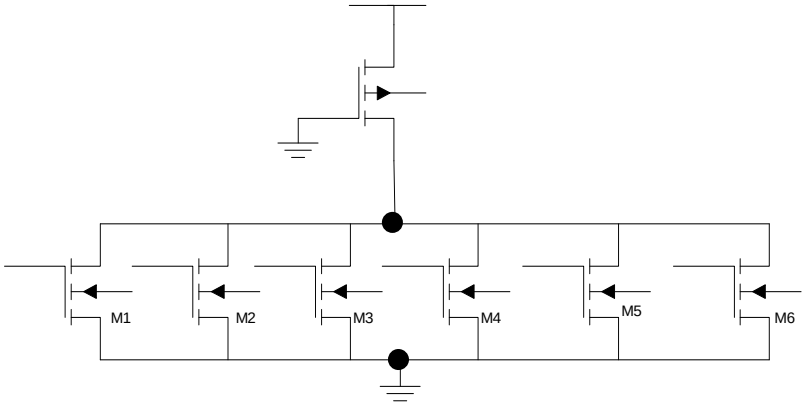

Figure 3.6 Pseudo NOR schematic

Table 3.3 gives the sizes of the transistors of the pseudo-NMOS NOR.

REF	W(µm)	L(µm)	M
M0	3.6	2.4	1
M1-M7	3.6	0.6	1

Table 3.3 Transistor sizes in pseudo NOR schematic

Simulations

The results of simulations performed on the circuits of the SRAM described herein are included in this section of the thesis. Simulations were run for the typical, worst case speed and worst case power corners. The RAM was tested at several different supply voltages 4V, 4.5V, 5V, 5.5V, 6V and at different temperatures from 0 degrees to 60 degrees.

A Verilog testbench was written which constantly wrote data into the RAM randomly until all the locations of the RAM were filled. The data is written at a constant rate of 200 ns *i.e.* at a 5MHz frequency. The address bits are changed every 200 ns and each of the 32 locations is written. After 4.5µs the write signal is disabled along with the decoder during which the bits lines are precharged to V_{DD}. Figures 3.7 and 3.8 show one of the bits (INP<17>) written into and read from the RAM. The write signal is high until all the loca-

tions are selected by the decoder. INP<17 > is the most significant bit (MSB) of the data from the testbench.

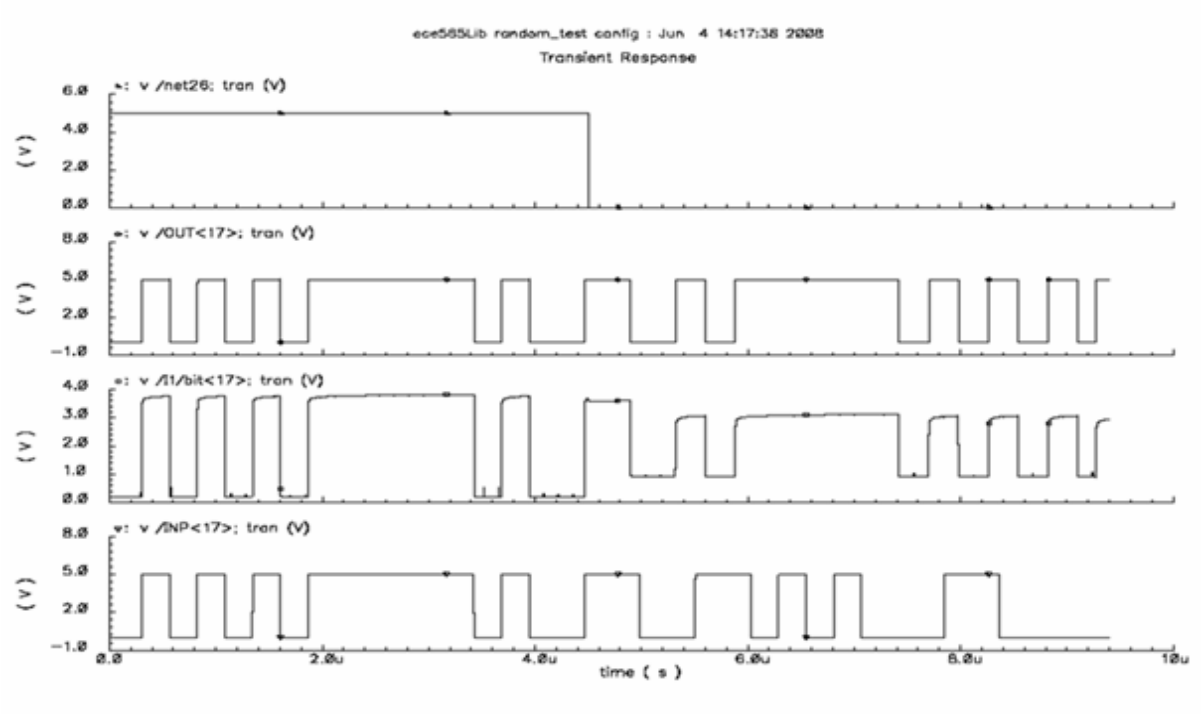

Figure 3.7 Waveform 1

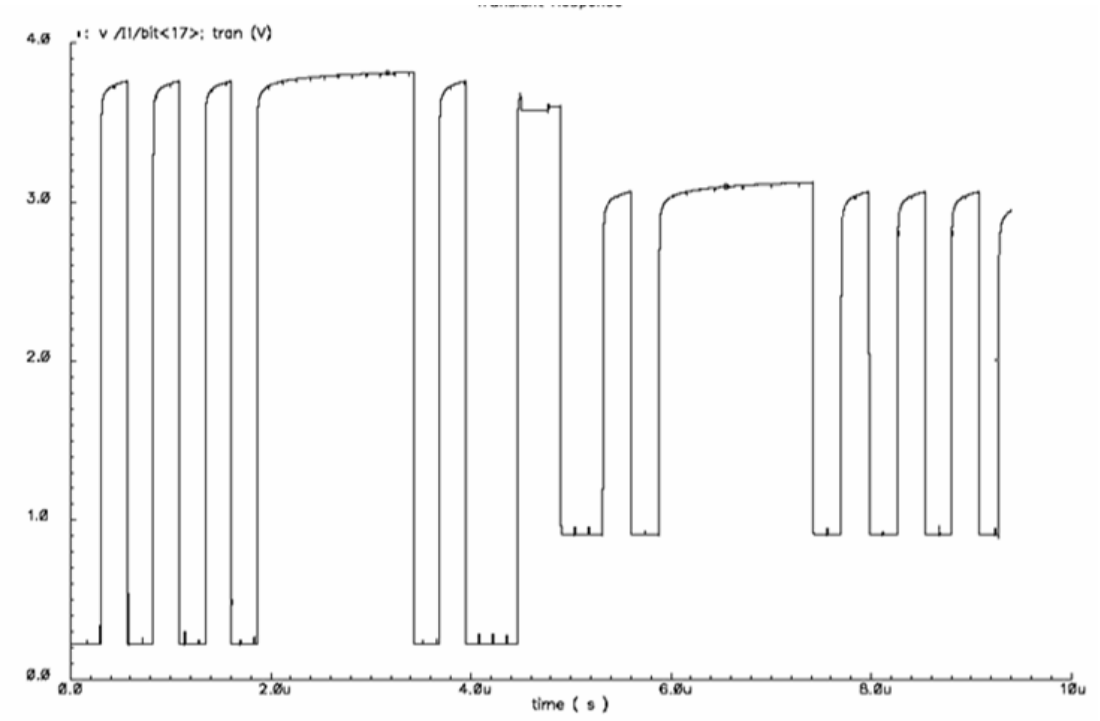

Figure 3.8 Waveform 2

CHAPTER 4

RAM LAYOUT

RAM 1-bit Layout

The layout of the memory should be compact. The central component of the layout is the array 1-bit RAM cells. Hence it is important that the RAM 1-bit layout be as small as possible. Figure 4.1 shows the layout of the 1-bit RAM cell. The select lines are drawn in such a way that when two cells are abutted together these lines are connected together to form the select line. The bit lines are also connected when two cells are abutted vertically.

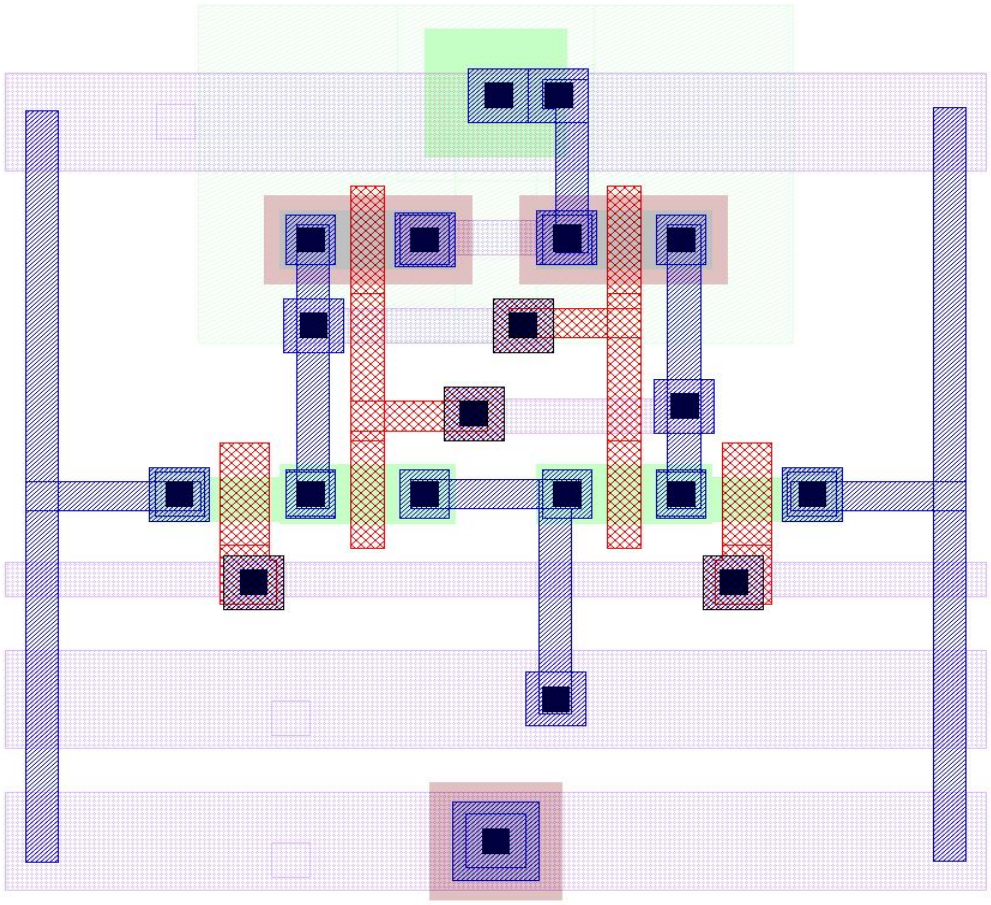

Figure 4.1 RAM 1-bit layout

RAM Precharge Circuit Layout

The figure 4.2 gives the layout of the RAM precharge circuit used in the memory.

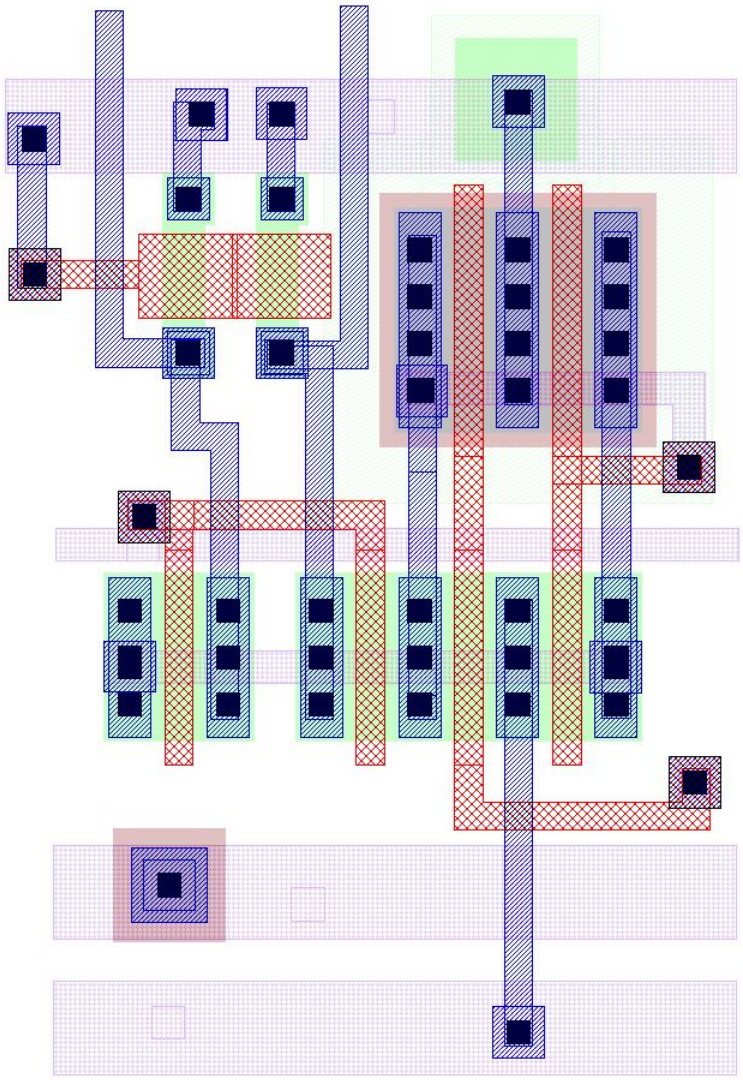

Figure 4.2 RAM precharge layout

Decoder Layout

Another important part of the layout is the decoder. The decoder layout should also be as compact as possible. As the select lines come across the RAM cell, the decoder is laid

out such that its height is almost equal to that of the RAM array so that the address select lines from the decoder also may come across. The decoder circuit is composed of pseudo-NOR gates. The pseudo-NOR gates are laid out horizontally with “NMOS” and “NMOS_bar” cells lined up horizontally for input and input-bar respectively. The drains and sources are all joined together when the cells are butted together. Figure 4.3 presents the NMOS cell used in the layout of the decoder.

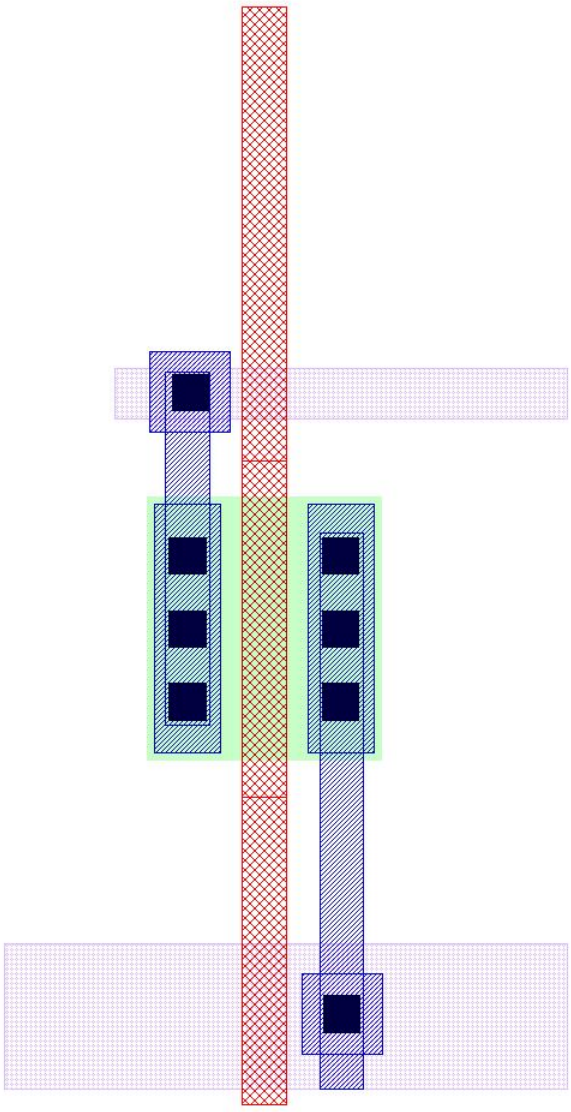

Figure 4.3 NMOS cell layout

In Figure 4.4 we see the layout of the “NMOS bar” cell used in the decoder layout.

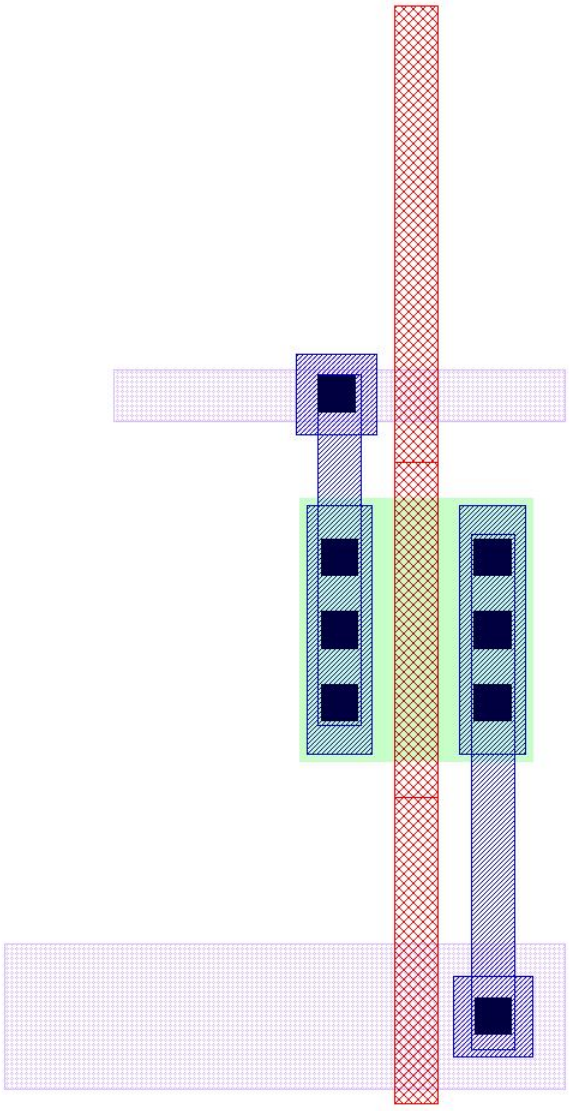

Figure 4.4 NMOS bar cell layout

When connected vertically, the gates of the transistors are joined together to form the input lines of the decoder. Figure 4.5 shows the layout of the “PMOS” cell used in the layout of the decoder.

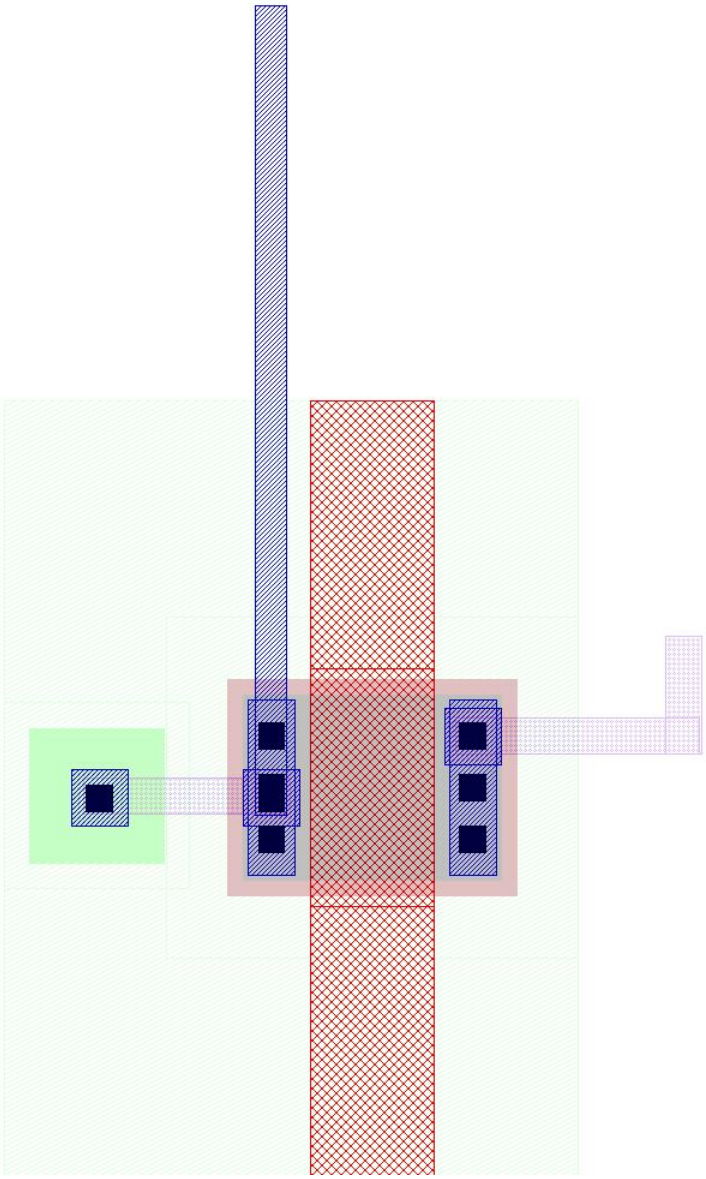

Figure 4.5 PMOS cell layout

All the sources of the “NMOS” and “NMOS bar” cells are aligned. All that the layout person needs to do is to abut these cells together and the inputs, V_{DD} and GND are automatically connected. All of the drains of the NMOS cells and the PMOS cells come across and are connected to the select lines which also come across the RAM array. Figure 4.6 illustrates the layout of the decoder.

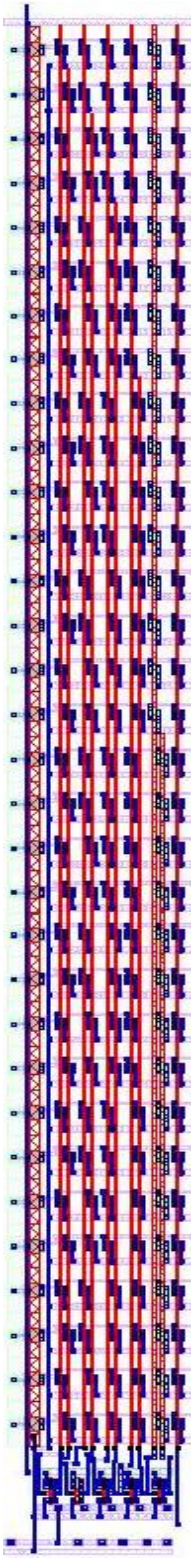

Figure 4.6 Decoder layout

Final Layout

The bit lines are vertical and join the bit lines from the RAM precharge cells. The layout of the 32 location by 18 bit SRAM (393.7 μm by 542.7 μm) is presented in Figure 4.7. The RAM cell array is located in the center. The pre-charge circuitry is located at the bottom. The decoder is located to the left, and the buffers are at the top. The RAM array can be easily extended in the future. The use of pseudo NMOS NOR gates significantly reduces the overall area occupied by the RAM.

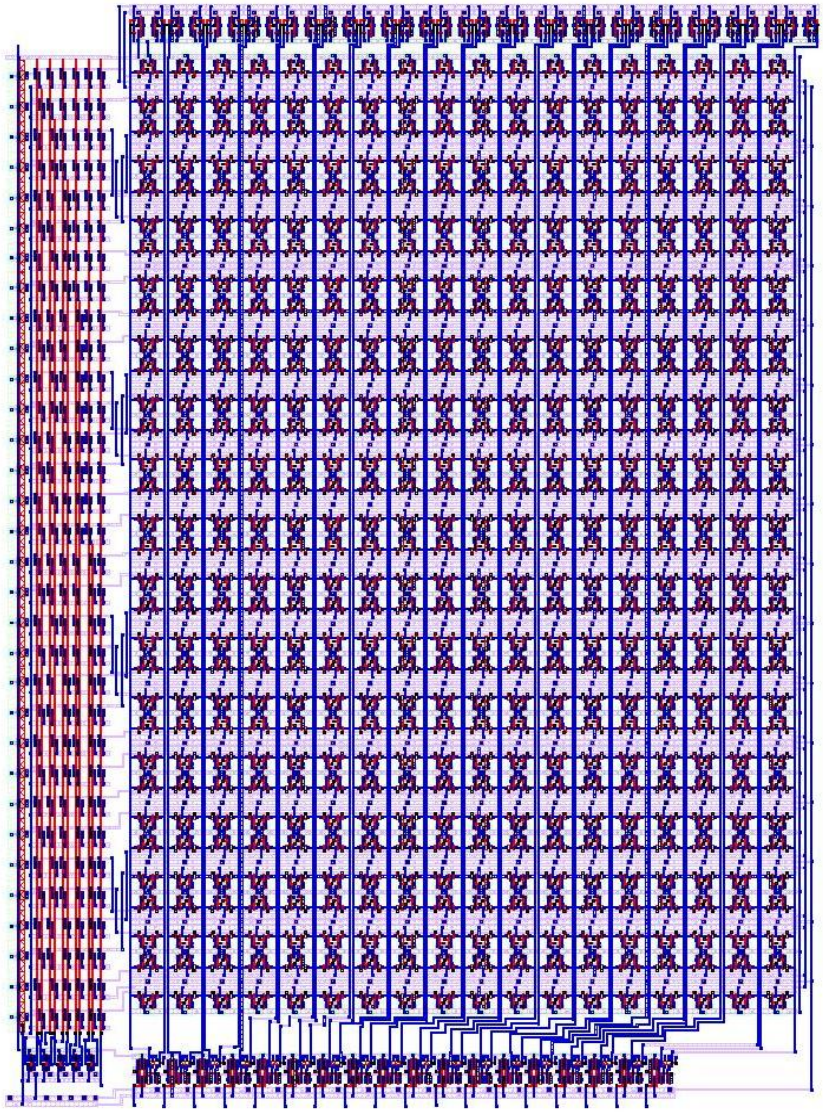

Figure 4.7 Final layout of RAM

CHAPTER 5

SUMMARY/FUTURE WORK

Summary

The PSD chip has been fabricated and is currently being tested and characterized. The next version of the chip is to integrate an on-chip ADC along with its companion RAM to store the digital outputs. The addition of an on-chip ADC will enhance its performance since sensitive analog circuits can be easily corrupted while digital data can easily and reliably transmitted off-chip.

If an on-chip ADC is used; however, then the data must be stored on-chip until the time it can be transmitted to the host computer. Therefore an on-chip memory (SRAM) is needed. To minimize the system-level interconnect, we propose to transmit the contents of the RAM storing the ADC results back to a host computer via a serial I2C-like interface. This greatly simplifies the system level design and in particular the design of mother board and associated chip boards. The design of the RAM which will store the data has been described in this thesis.

Conclusions

Simulations demonstrate that RAM should work very well when integrated onto the PSD chip along with the ADC. The RAM is simulated and layout is complete. The simulations were also performed on the extracted view of the RAM layout which yielded results that match with the simulations preformed on the schematic. The design is now ready for integration on to the existing PSD chip.

Future Work

The RAM along with the ADC layout must be integrated into the existing layout of PSD8C chip and is expected to be fabricated and ready for field testing by December 2009. The ADC when integrated on-chip on to the AA-DSP chip (discussed in Chapter 1) can be completed in a maximum of 125 μs. Even in this case only a 256 location memory is required to store the data. The RAM is laid out in such a way that extensions for future are quite easy.

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APPENDIX A

Verilog Code Test Bench for RAM

```
//Verilog HDL for "ece585Lib", "random" "functional"


     // Random Number Generator, 8-bit

      module RAM_tb(inp_bits,address_bits);
      output [17:0] inp_bits;
      output [4:0] address_bits;
      reg clk, reset,rst;
      reg [17:0] x;
      wire      feedback;
      wire      feedback1;
      wire [4:0] addr;
      reg [4:0] tmp;
      reg up_down;


      integer fid;


      // Use TAPS table from XACT 052 to make whatever length sequence you
      need.
      assign feedback = ~^{x[7],x[5],x[4],x[3]};
      assign feedback1 = ~^{x[17],x[6],x[10],x[12]};



      always @(posedge clk or rst or up_down )
      begin
         if (rst == 1'b1)
            tmp <= 5'b00000;
         if (up_down ==1'b1)
            tmp = tmp + 5'b00001;
         else if(up_down ==1'b0)
            tmp = tmp - 5'b00001;
         if (tmp == 5'b11111)
            up_down = 1'b0;
         else if (tmp == 5'b00000)
            up_down = 1'b1;

      //    #165 address_bits <=  tmp;
      end

      assign address_bits =  tmp;


      // Shift and input feedback term.  That's it!
      always @(posedge clk) begin
         if (reset) x <= 0;
         else
            #165 x <= {feedback1,x[15:0], feedback};
      end
```

```
assign inp_bits = x;


// remaining code just testbench...
initial begin
      fid = $fopen("./Random.out");
      $fmonitor(fid,$time,"   x = %h",x,  "addr = %b",  tmp, "
up_down = %b",  up_down);
 $dumpfile("./Random.dmp");
   clk = 0;
   forever begin
      #10 clk = ~clk;
   end
end

initial
begin
   reset = 0;
#9 rst = 0;
#1 reset = 1;
   rst = 1;

#25 reset = 0;
    rst = 0;
    up_down =0;
end


initial begin
   @(negedge reset);
   repeat (1024) begin
      @(posedge clk) #1;
  //    $display ("%h", x);

   end
   $finish;
end
endmodule
```