HINP16C Revision 3

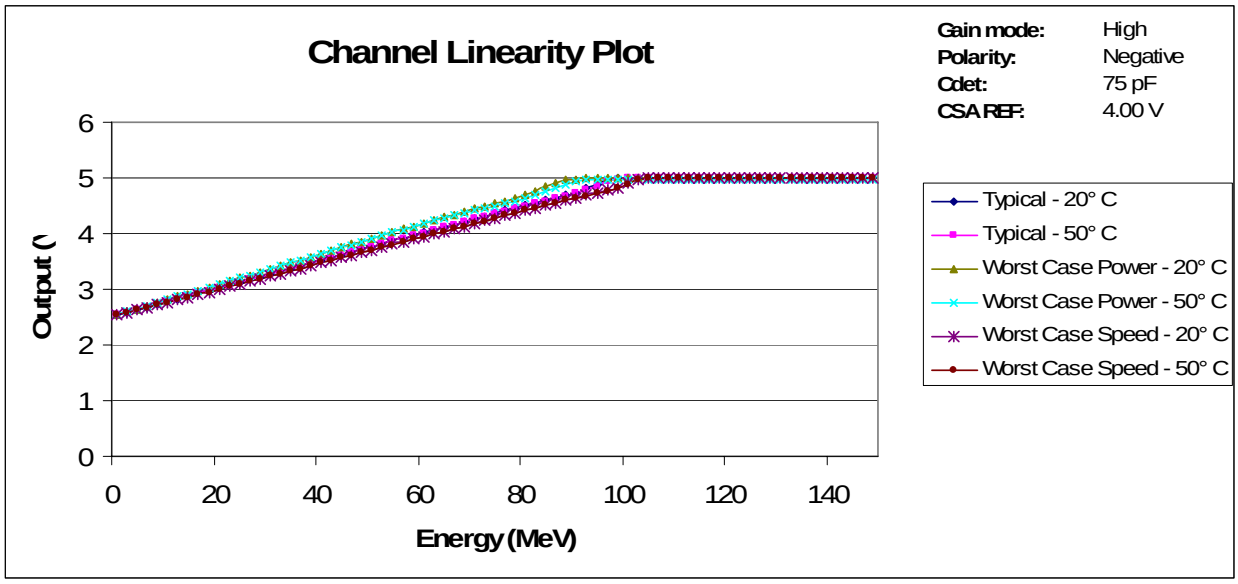
Configuration Register

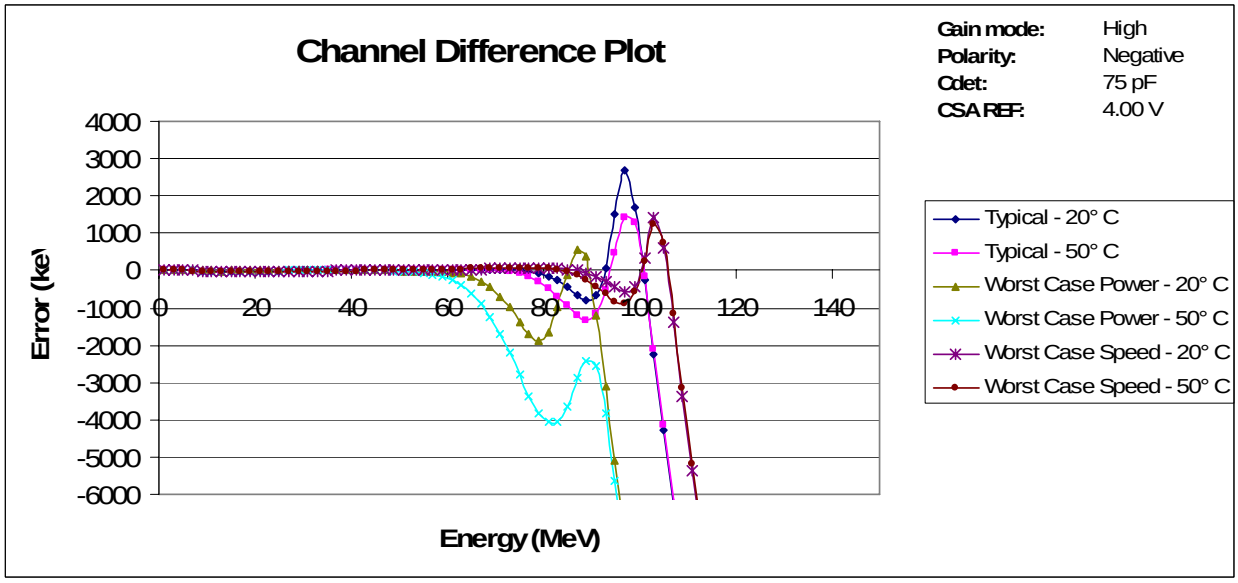
Bit Position	Function	Default
0 – 15	0 = Enable Ch X (Bit 0 = Ch 0) 1 = Disable Ch X	Ch X enabled
16 – 31	Currently unused	
32	0 = Positive Polarity 1 = Negative Polarity	Positive polarity
33	0 = 2 µsec TVC range 1 = 500 nsec TVC range	2 µsec range
34	0 = CSA high-gain mode. 1 = CSA low-gain mode.	High-gain mode
35	0 = test mode 1 OFF 1 = test mode 1 ON - CSA output for selected channel brought out to pins.	Test mode 1 OFF
36	0 = Enable internal CSA. 1 = Select external preamp.	Use internal CSA
37	0 = test mode 3 OFF 1 = test mode 3 ON - Peak sampling circuit of selected channel driven by external signal.	Test mode 3 OFF
38	0 = test mode 4 OFF 1 = test mode 4 ON - Shaper output for selected channel brought out to pins.	Test mode 4 OFF
39	0 = select 5 pF capacitor for Fast Shaper 1 = select 12.5 pF capacitor for Fast Shaper	5 pF capacitor
40 – 47	Chip ID (Bit 47 MSB)	Chip ID = 0

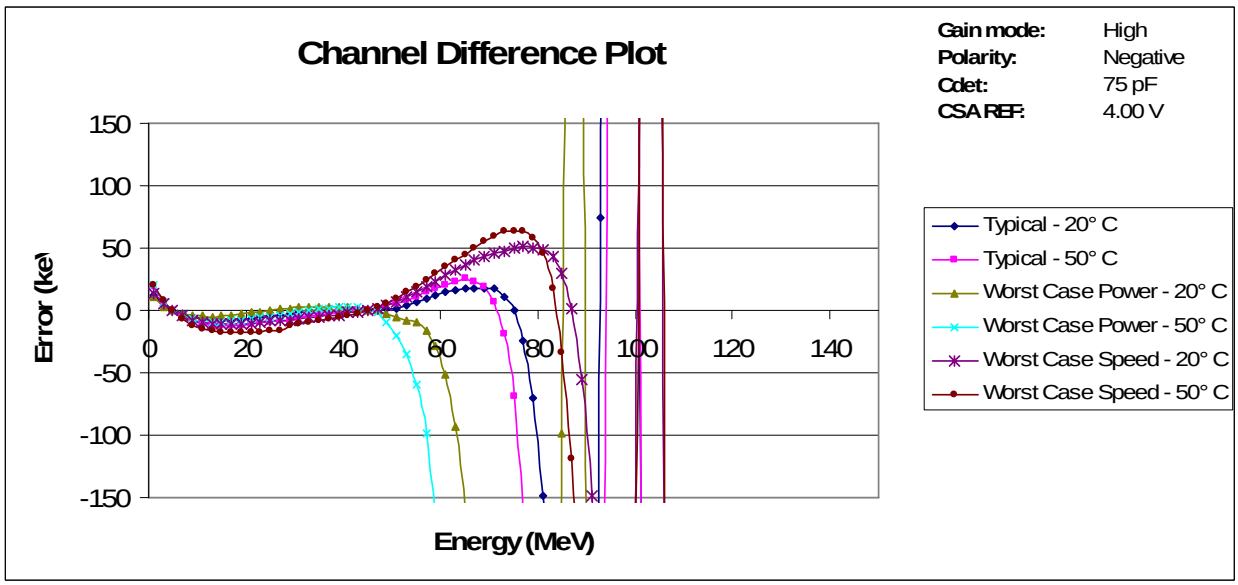
Table 1

Channel Linearity

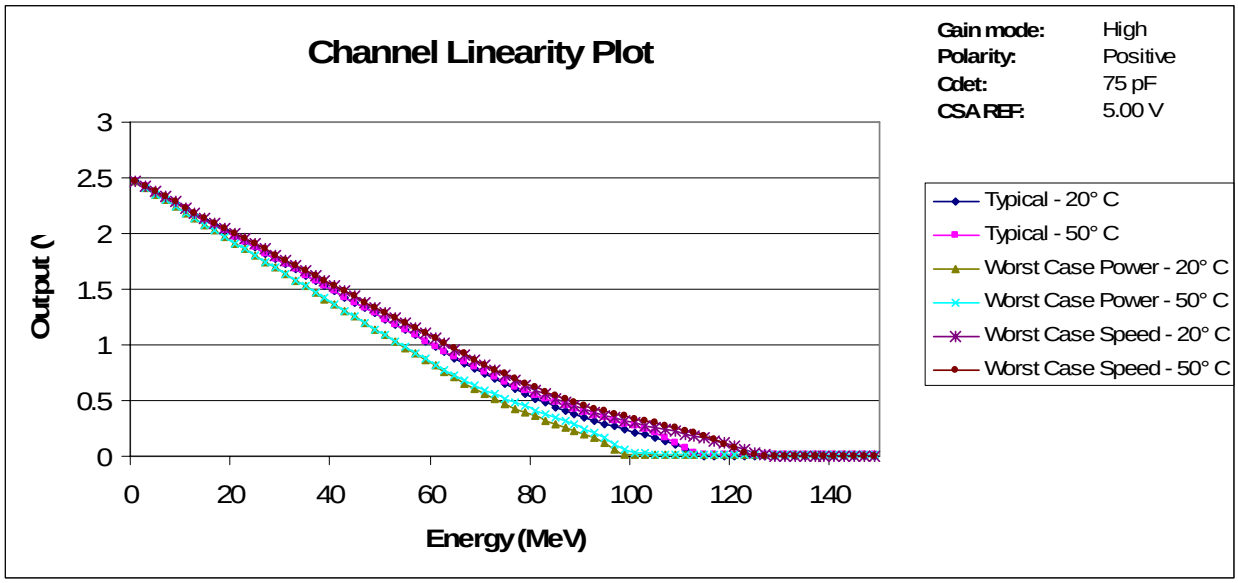
These three plots show channel linearity in ***high gain*** mode for ***negative*** polarity.

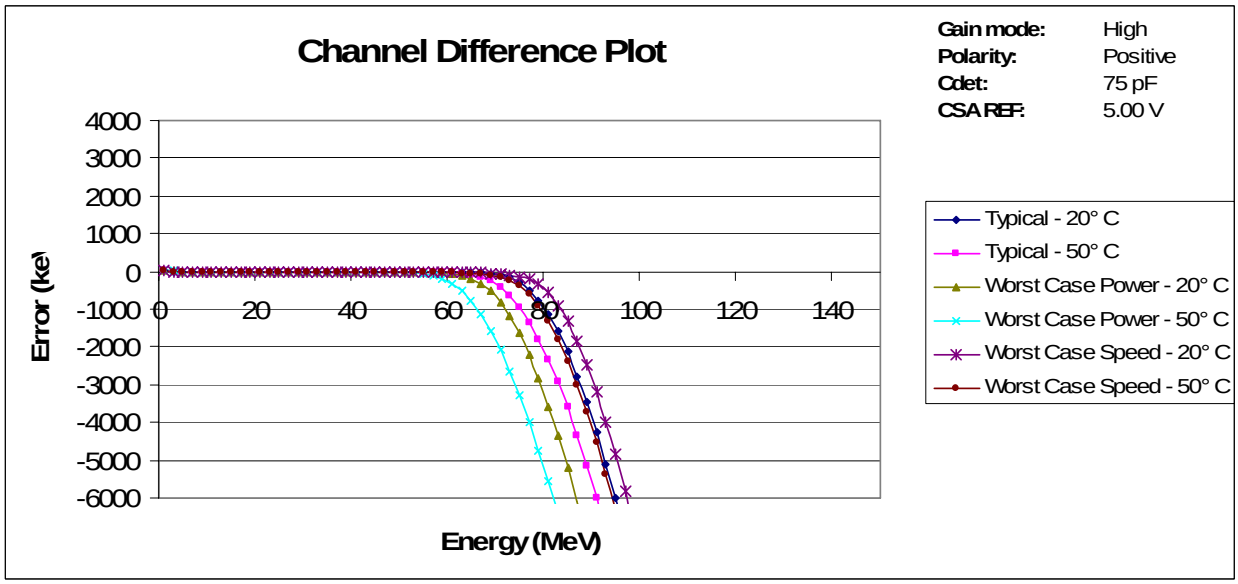


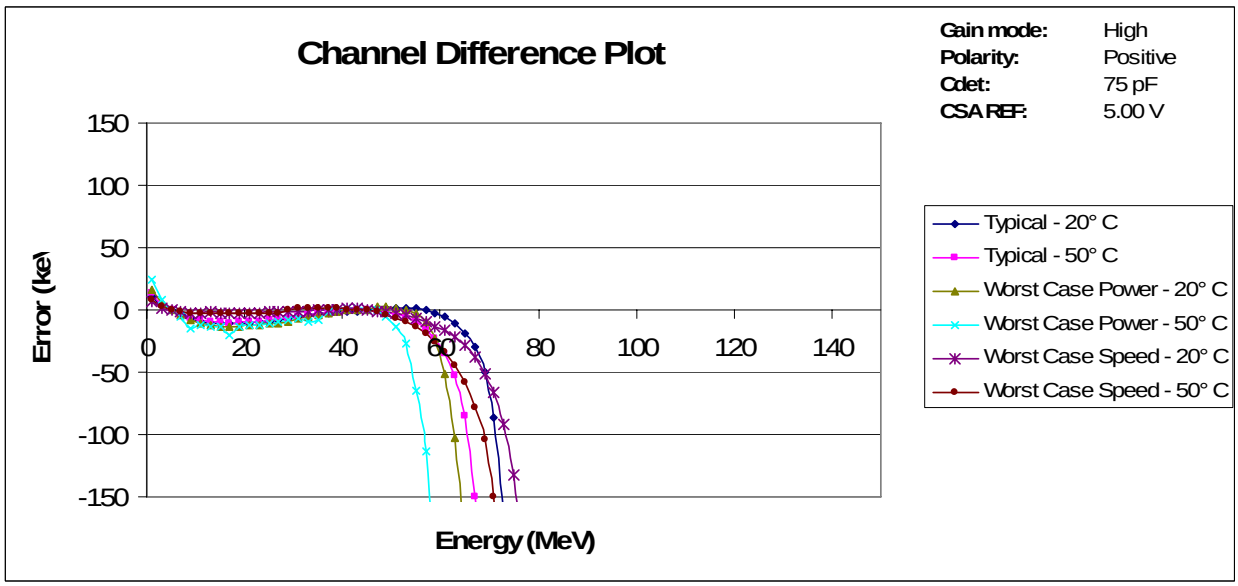




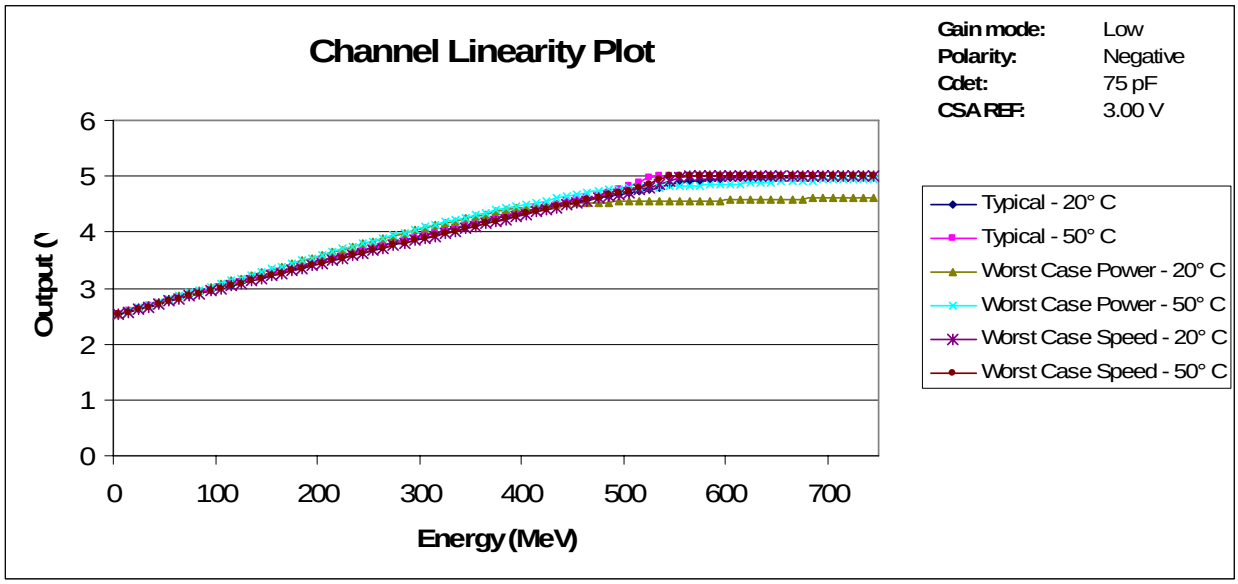
These three plots show channel linearity in ***high gain*** mode for ***positive*** polarity.

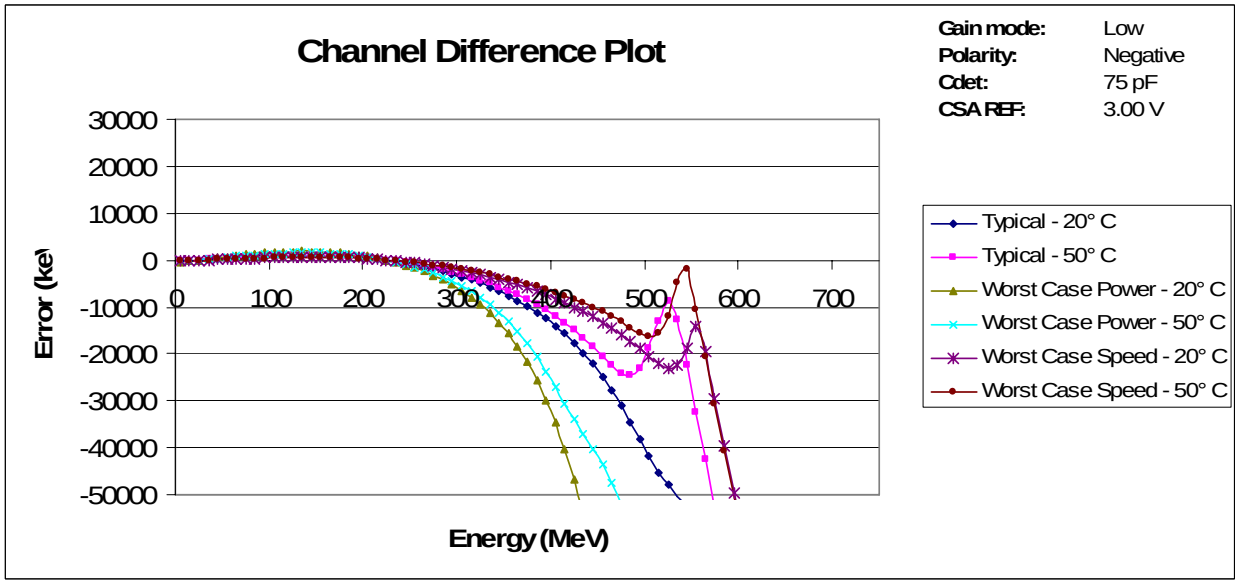


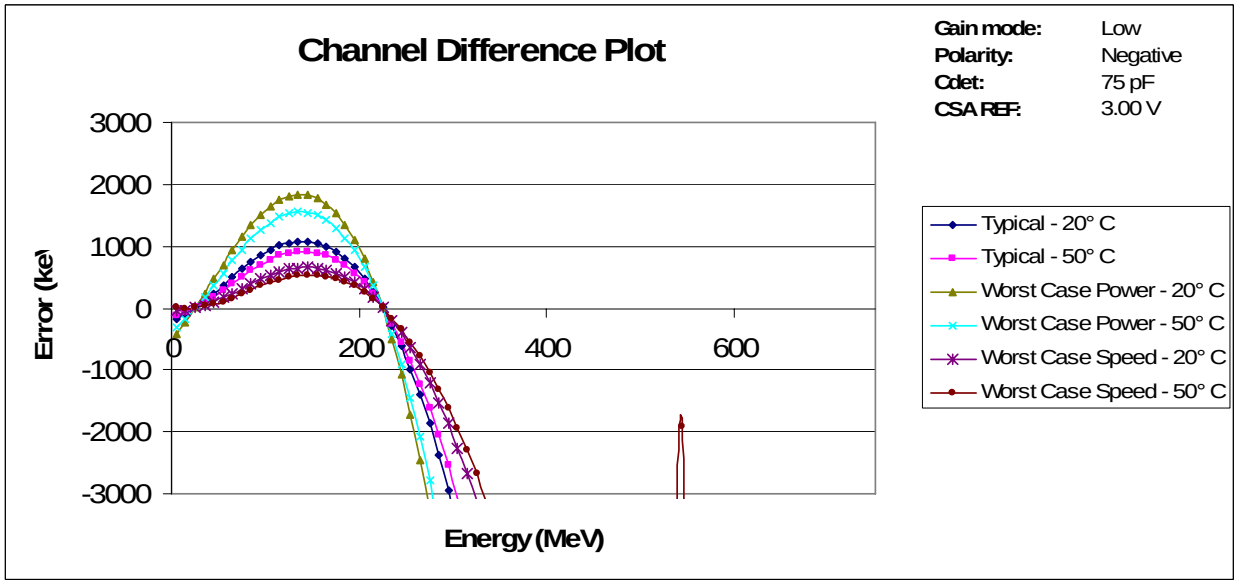




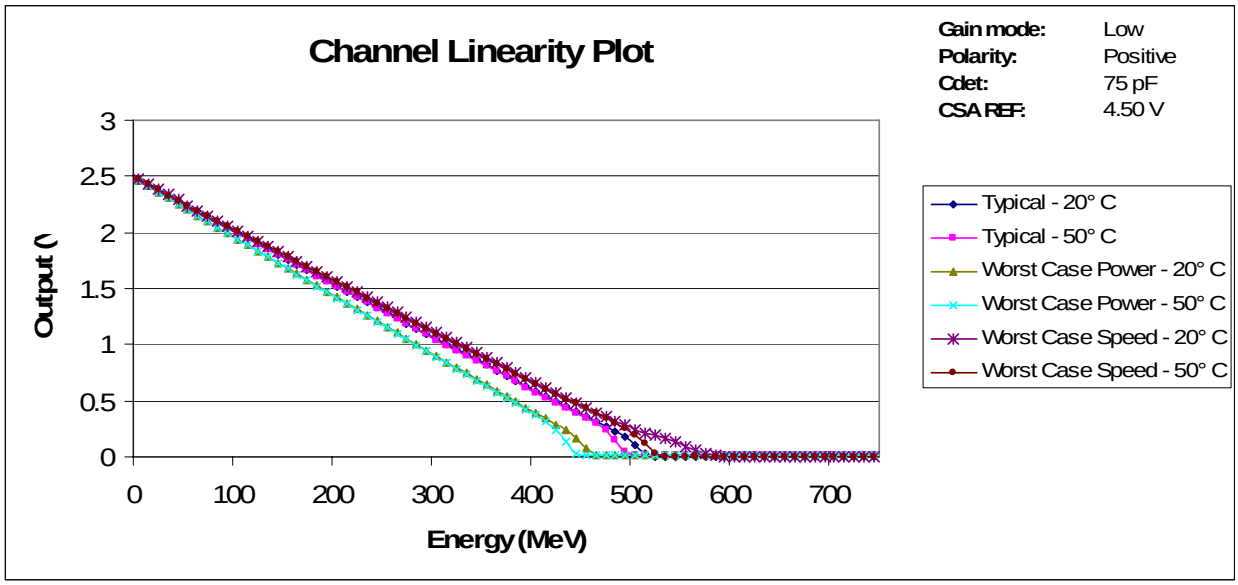
These three plots show channel linearity in ***low gain*** mode for ***negative*** polarity.

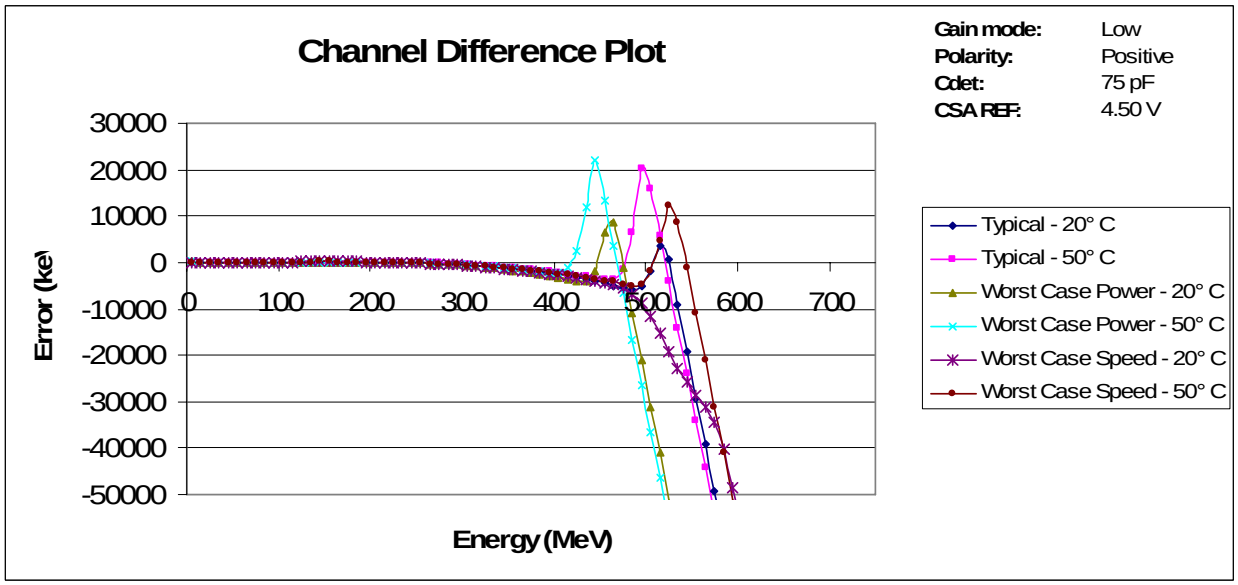


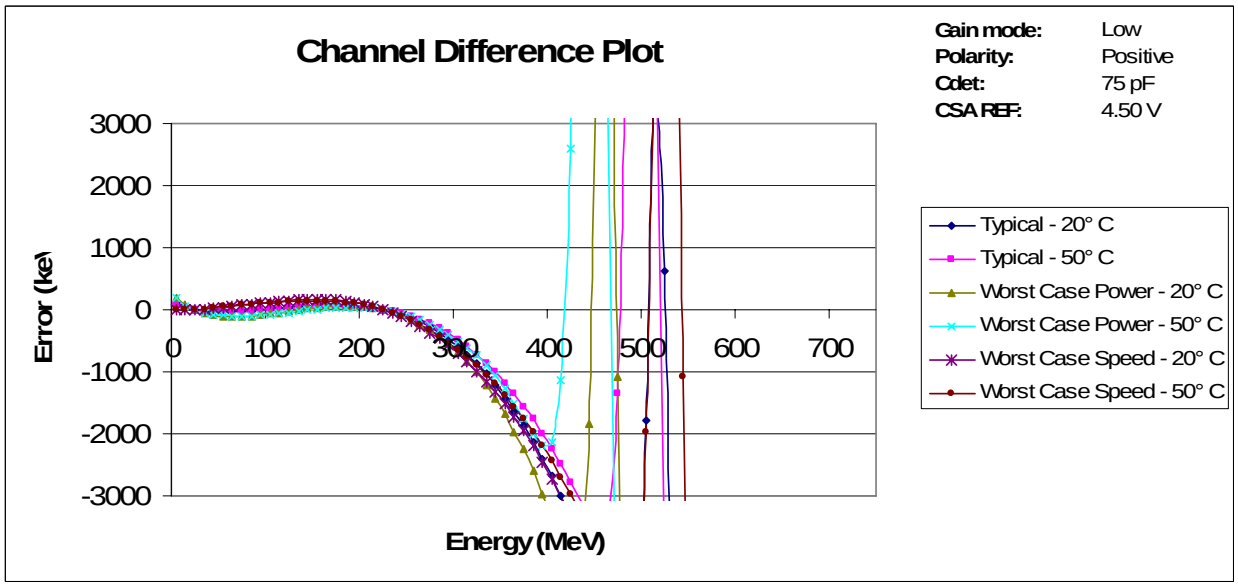




These three plots show channel linearity in ***low gain*** mode for ***positive*** polarity.



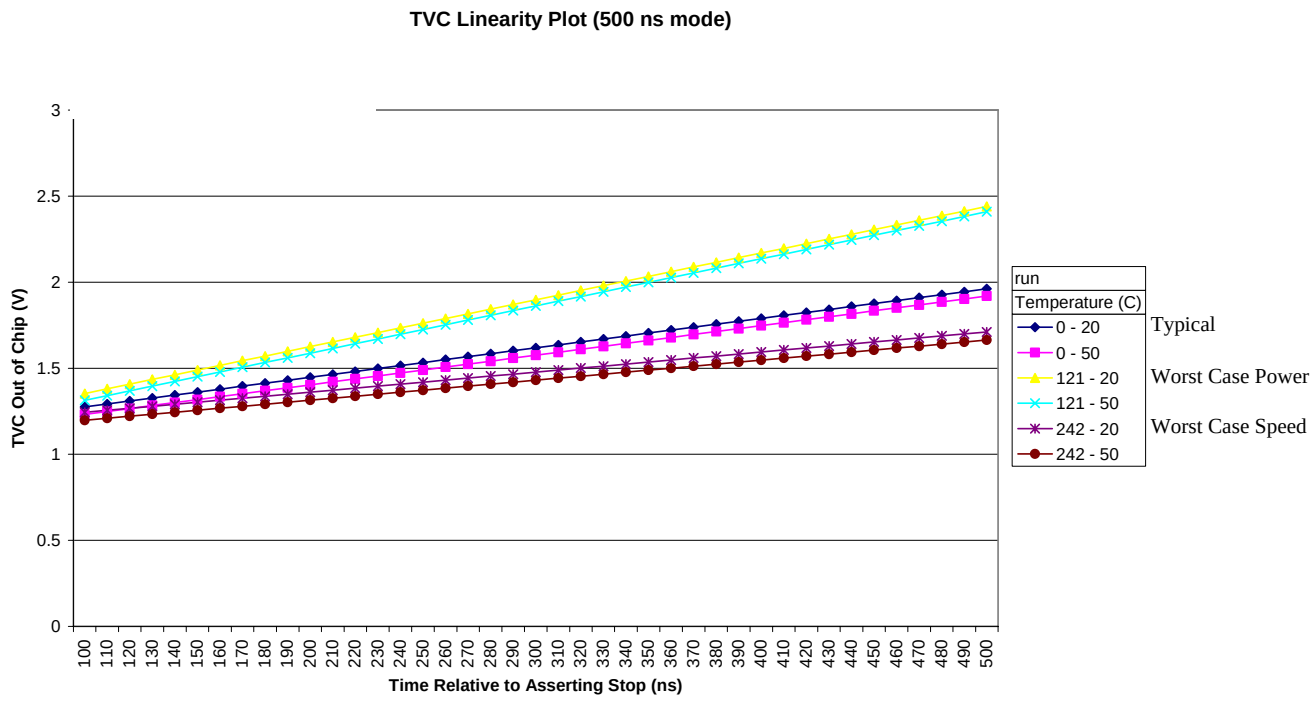




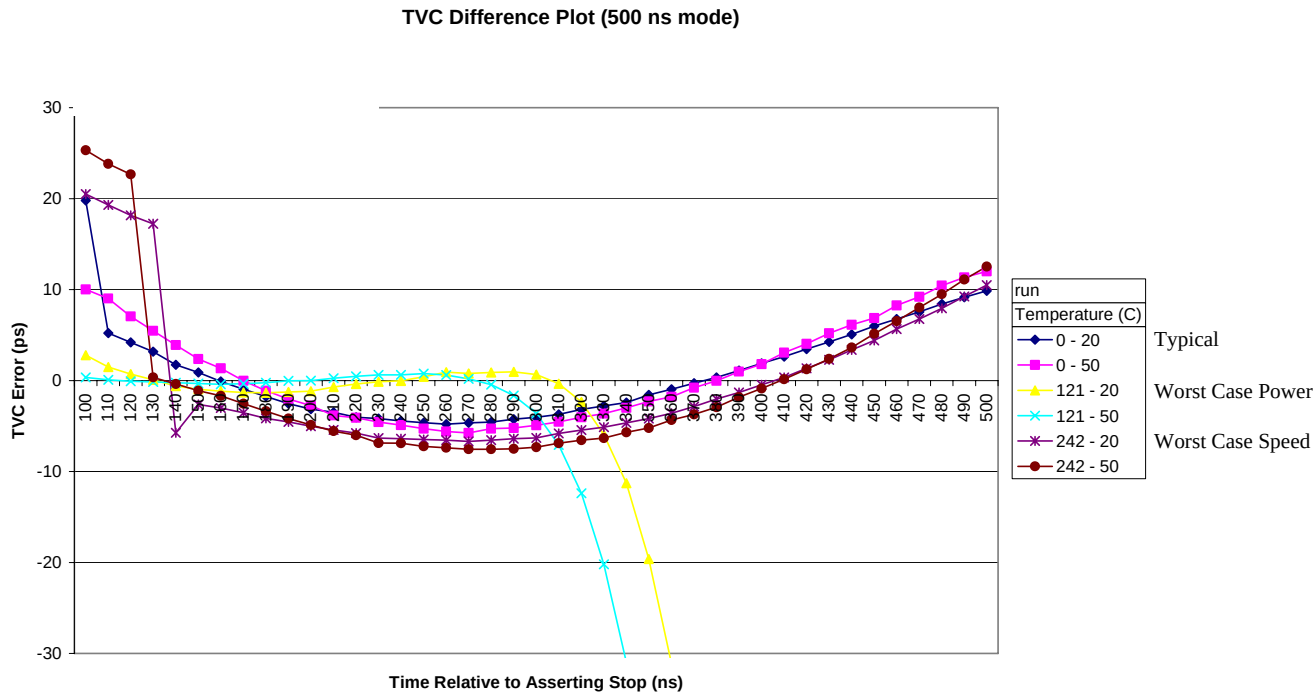
TVC Linearity

These two plots show TVC linearity in ***500 ns*** mode.

VDD	5	TVC Mode	500 ns

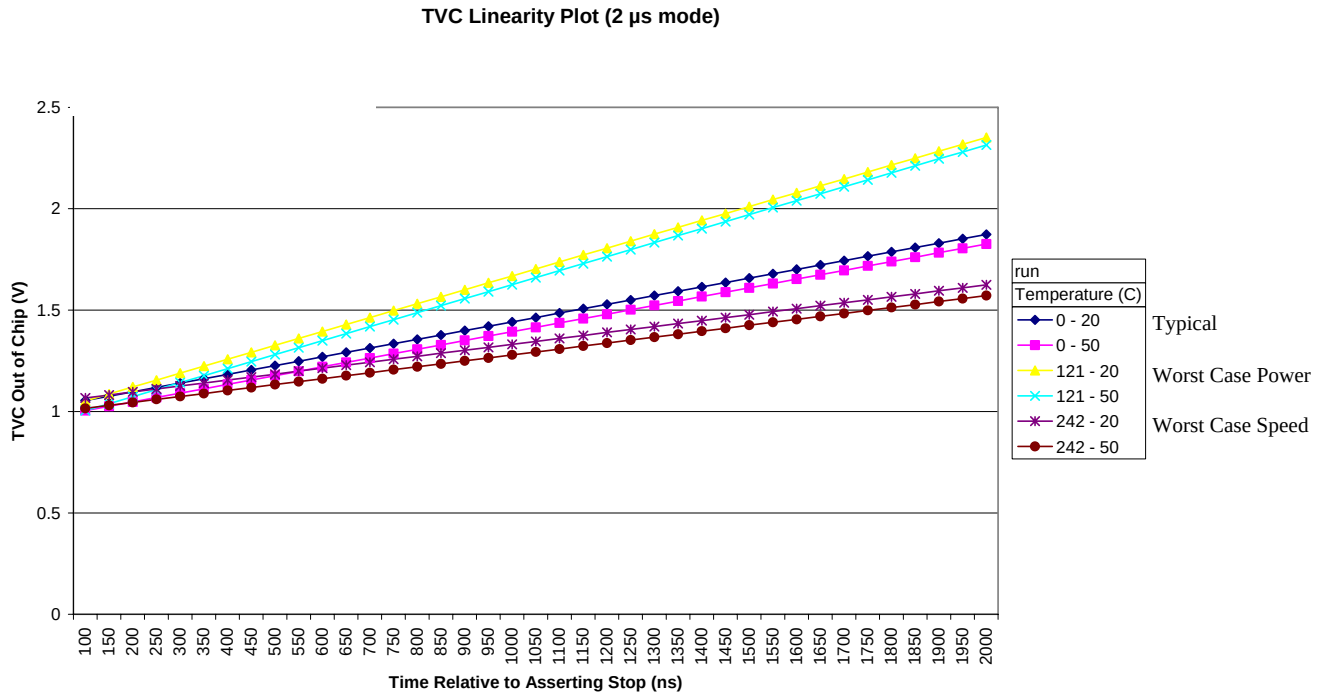


VDD	5	TVC Mode	500 ns

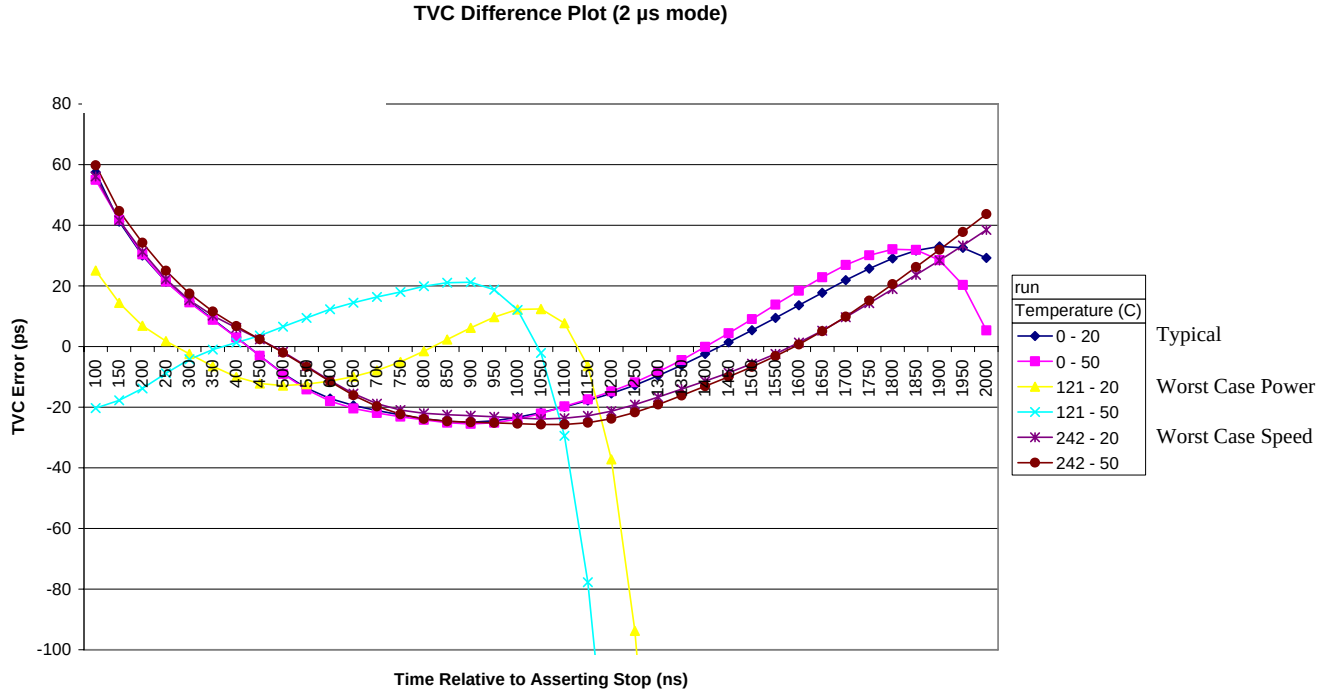


These two plots show TVC linearity in ***2 µs*** mode.

VDD	5	TVC Mode	2,000 ns



VDD	5	TVC Mode	2,000 ns



Fast Shaper Times

	Rise Time (ns)	
Capacitance (pF)	**3 dB Loss**	**6 dB Loss**
5.75	103	322
14.38	333	858

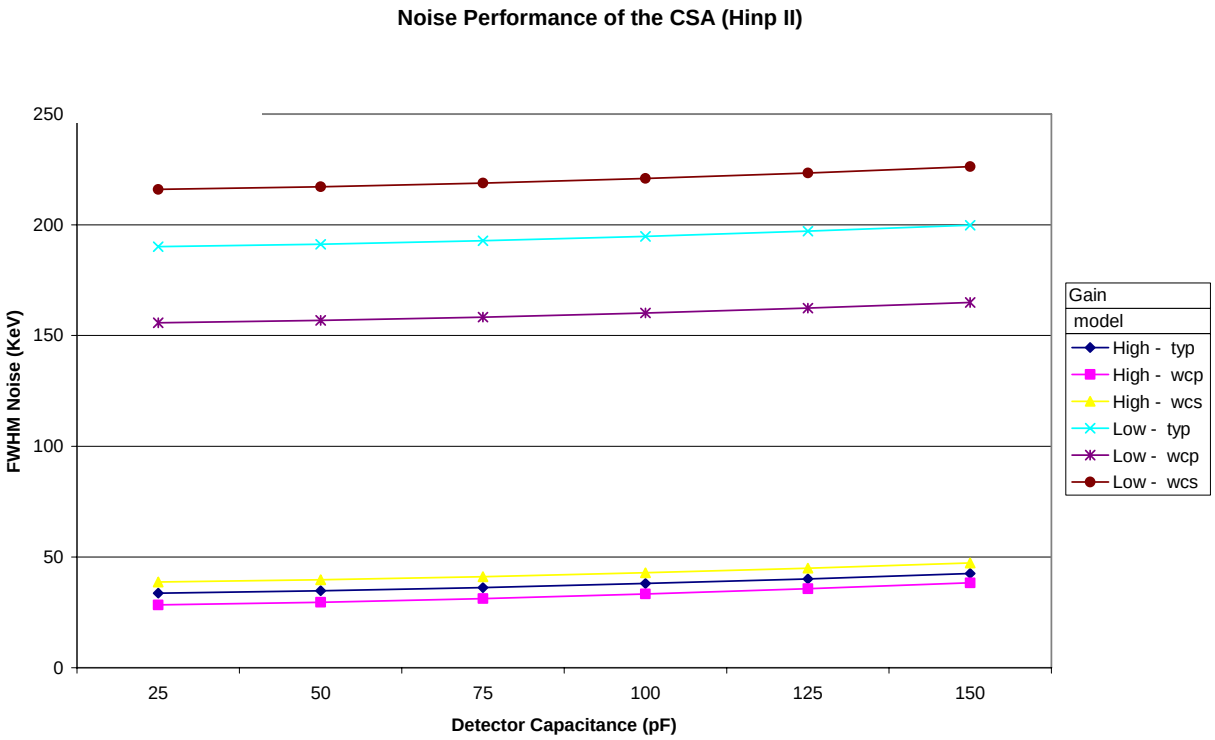
Gain Performance (Between HinpII and Hinp3)

		From Hinp II to Hinp 3
Low Gain	Negative	59%
	Positive	45%
High Gain	Negative	60%
	Positive	54%

From input pin to output pin

Noise Performance (Between HinpII and Hinp3)

csa_ref (V)	4	temp (C)	40



csa_ref (V)	4	temp (C)	40