HINP16C
(Heavy Ion Nuclear Physics, 16 Channel)

A Sixteen-Channel Integrated Circuit For Use With Silicon Strip Detectors in Colliding Particle Experiments

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1.0 Introduction

This manuscript is intended to provide *preliminary* documentation for the sixteen channel integrated circuit (IC) under development. The IC is designed for use with an array of silicon strip detectors in a wide variety of colliding particle experiments scheduled for Fall 2002. Only very simple explanations concerning the operating principles of the various subsystems will be provided at this time. Emphasis is placed on simulation results predicting performance.

The simulation results demonstrate that the IC will be capable of providing both high resolution energy and time measurements. The IC is referred to as the HINP16C (Heavy Ion Nuclear Physics)IC throughout this document.

2.0 Bias Circuits

Several circuits are required to correctly bias the analog subsystems. These consists of a bandgap voltage reference, a constant current reference, and a reference for the digital-to-analog converter used to correct offsets associated with the leading edge discriminator.

2.1 Bandgap Voltage Reference

The core of the bias circuitry is a simple bandgap voltage reference. The bandgap reference produces a relatively stable voltage (1.23 volts) with respect to both power supply and temperature variations.

The bandgap circuit makes use of parasitic bipolar vertical PNP transistors. A PTAT (Proportional to Absolute Temperature) current is created by forcing equal currents through two diode-connected transistors whose area differ by a factor of ten. A 60 mV voltage exists across a 590 Ohm resistor, producing a current of approximately 125 μA. The current is mirrored and passed through a 5.3 KΩ resistor to yield a voltage and summed with a base-emitter voltage. The base-emitter voltage displays a negative temperature coefficient and compensates the positive temperature dependence of the voltage developed across the 4.5 KΩ resistor.

Through the use of current mirrors, bias voltages corresponding to several different bias currents are also created. These bias voltages are then heavily filtered in order to greatly improve noise performance.

Summary of bias voltages and associated currents at 27C:

```
BANDGAP_VOLT      =     1.2331E+00 Volts
BANDGAP_CURRENT   =     1.2106E-01 mA

VBN_CSA           =     1.3694E+00 Volts (0.91164 in LOW GAIN mode)
I_CSA             =     9.0598E-01 mA

VBN_SHAPER        =     1.8519E+00 Volts
I_SHAPER          =     6.0567E-02 mA

VBN_10UA          =     1.9829E+00 Volts
I_10UA            =     1.0094E-02 mA

VBN_DISC          =     2.6245E+00 Volts
IB_DISC           =     6.0551E-02 mA

VBP1_DAC          =     3.3796 Volts
VBP_HIT           =     3.4597 Volts
VB_TVC            =     3.3650 Volts
```

Variations of the bandgap output with respect to temperature are illustrated in Figure 1. The bandgap voltage varies only by 5 mV over a temperature range of 40 Celsius. Performance is summarized below:

Supply current (typical):	1.5 mA (high-gain mode) 0.75 mA (low-gain mode)
Area:	
Noise at Vref output:	100 µV (10 Hz - 10 MHz)
Nominal Output:	1.233 Volts (27 C)
Tempco:	+125 µV / C

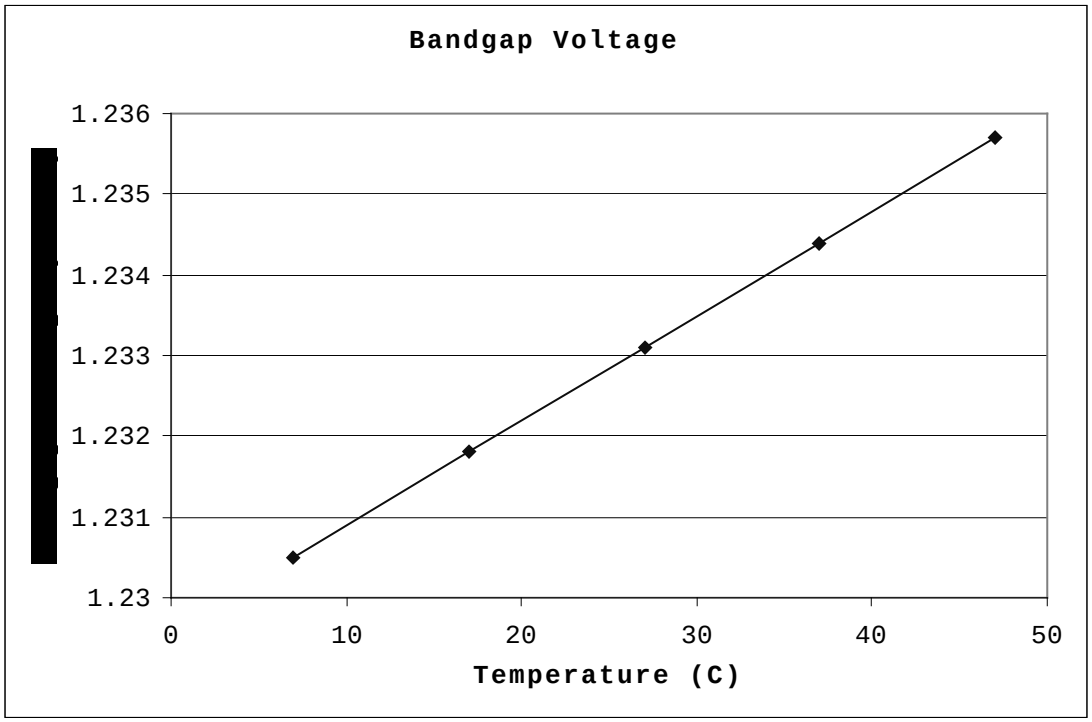


Figure 1: Bandgap Reference Temperature Dependence

2.2 Constant Current Source

The time-to-voltage converter requires a constant current to charge a capacitor, thereby, producing a voltage that varies linearly with time but independent of temperature or supply voltage. It is important that the charging current display little, if any, temperature dependence. The bandgap voltage, described in section 2.1, is applied across a temperature independent resistor. The temperature independence of the resistance is accomplished through a series combination of a resistance with a positive temperature coefficient (ny polysilicon) and a resistance with a negative temperature coefficient (hy polysilicon). See Figure 2.

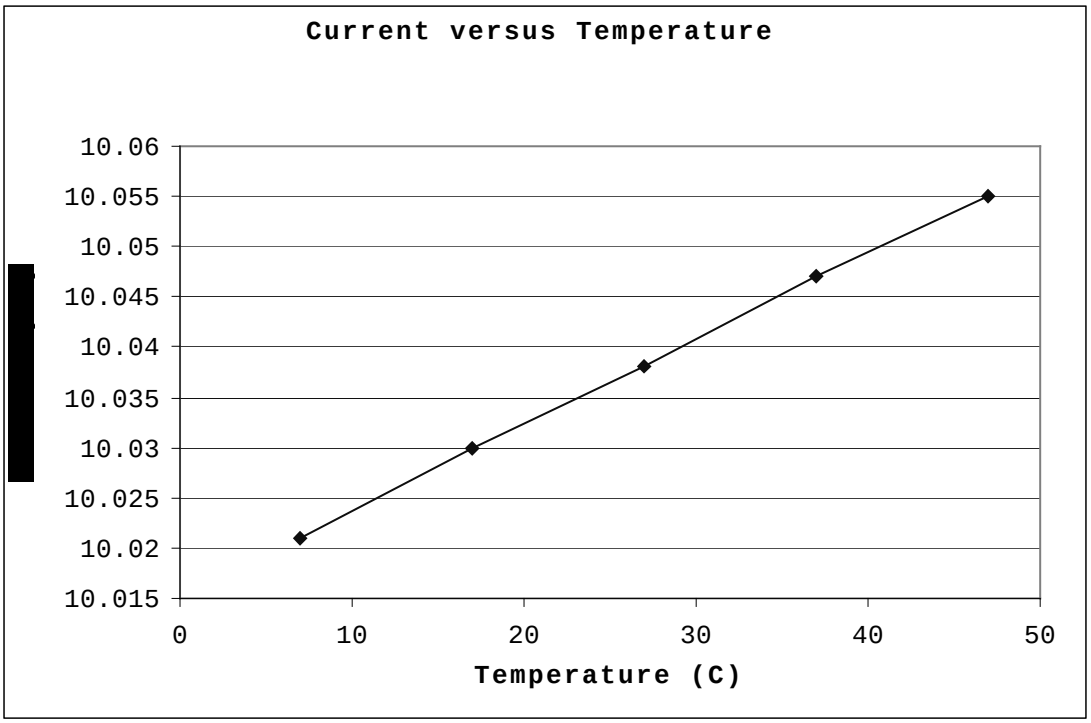


Figure 2: Constant Current Temperature Dependence

Performance is summarized below:

Nominal Output: 10.038 uA (27 C)

Tempco: + 850 pA / C

Current varies by +/- 0.17% around the nominal temperature of 27 C. Since the capacitor has virtually a zero temperature coefficient, this will also be the relative error in time measurements. We see by comparing Figures 1 and 2 that the temperature dependence of the current source is almost completely due to the temperature dependence of the bandgap reference.

2.3 DAC Reference

The bandgap reference is also used as a reference for the DACs used to offset compensate the leading edge discriminators. The 1.233 Volt reference is used in a feedback loop along with a 60 KΩ resistor to generate a 20 μA current. Further details will be provided when DAC operation is discussed later in this report.

3.0 Charge Sensitive Amplifier (CSA)

The charge sensitive amplifier (CSA) is used to convert the charge packet originating at the silicon strip detector into a voltage. A single-ended folded cascode amplifier topology was used. A source follower buffers the output. A feedback capacitor sets the gain. A large feedback resistor, effectively in parallel with the gain setting capacitor determine the decay time constant.

The CSA can be placed in one of two gain modes: C_f equal 2.5 pF (referred to as the *high-gain* mode) and C_f equal 12.5 pF (referred to as the *low-gain* mode). The decay time constant is nominally the same (25 μsec) in both gain settings. Moreover, the internal CSA can be bypassed and the succeeding electronics can be driven by off-chip, external preamps. When this mode is selected by setting bit 36 in the configuration register to a '1', the internal CSA is effectively shut down. The gate of the PFET input device is connected to the positive supply rail. This drives the output of the CSA near the negative rail.

3.1 CSA Transfer characteristic

The response of the CSA is illustrated below in Figure 3. The simulation was performed with the following parameters:

High-gain mode:	Feedback capacitance 2.5 pF, Feedback resistance 10 MΩ
Detector capacitance:	75 pF
Input:	10 mA, 80 psec current pulse (5 million electrons)
CSA ground voltage:	2.5 Volts

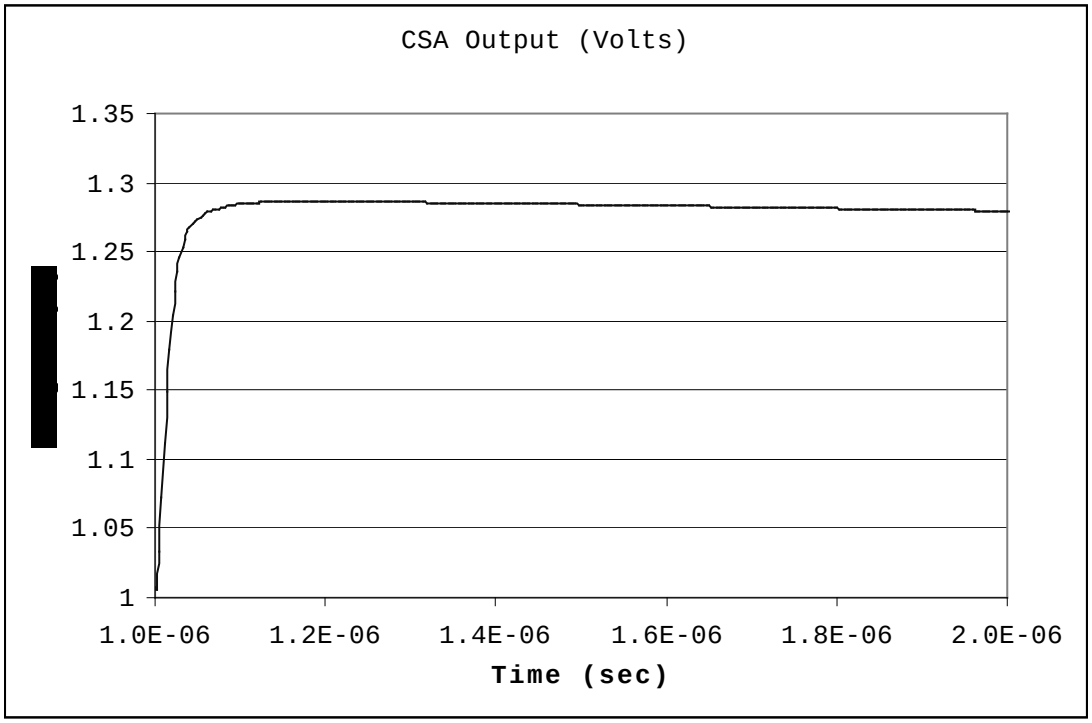


Figure 3: CSA output (high-gain mode) with C_{det} = 75 pF

The response is excellent. It is summarized below:

Risetime:	22 nsec
Decay time:	49 usec
Actual peak amplitude:	280 mV
Expected peak amplitude:	320 mV
Transfer function:	1 Volt = 17.86e+06 electrons

The discrepancy (-1.15 dB) between the actual and the expected value of the peak is primarily due to the loss associated with the NFET source follower (bulk modulation effects) used to buffer the CSA output.

With a detector capacitance of 30 pF, the response begins to deteriorate, displaying ringing. The risetime is 11 nsec. For comparison purposes, the response is presented in Figure 4. At 10 pF, the ringing is severe and not acceptable.

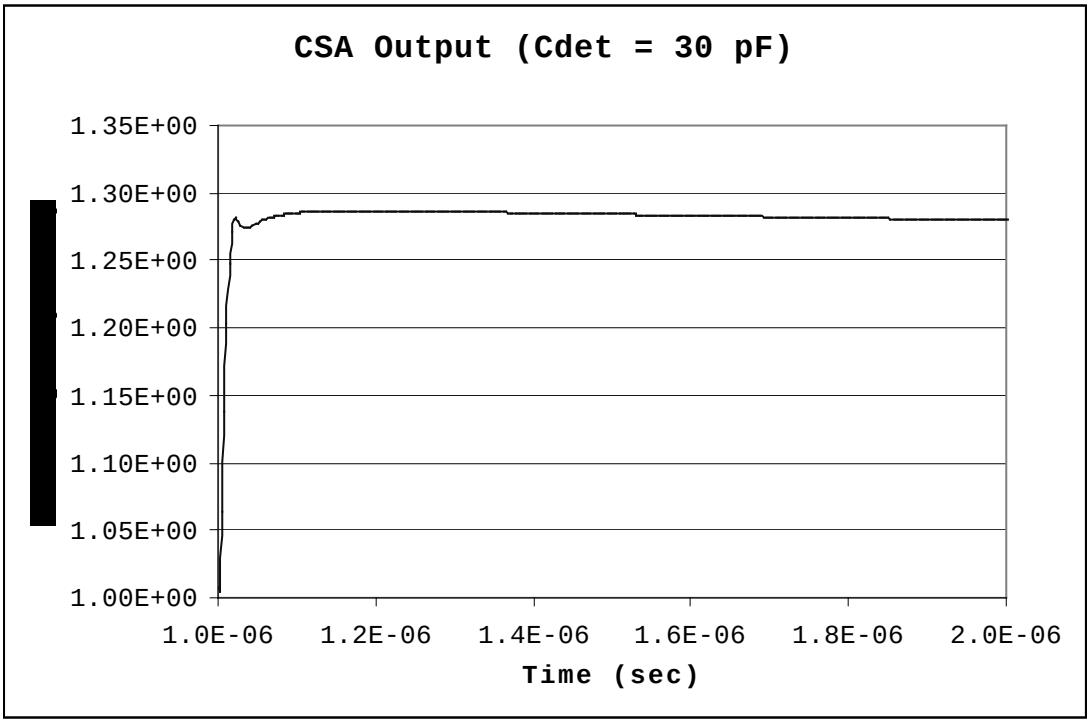


Figure 4: CSA output (high-gain mode) with C_{det} = 30 pF

The CSA was re-characterized for the low-gain mode.

Low-gain mode:	Feedback capacitance 12.5 pF, Feedback resistance 2 MΩ
Detector capacitance:	75 pF
Input:	50 mA, 80 psec current pulse (25 million electrons)
CSA ground voltage:	2.5 Volts

The results were:

Risetime:	140 nsec
Decay time:	66 usec
Actual peak amplitude:	280 mV
Expected peak amplitude:	320 mV
Transfer function:	1 Volt = 89.3e+06 electrons

2.2 Linearity

The CSA is linear for both positive and negative going pulses. This is illustrated in Figures 5 and 6. For the positive going output pulses, the CSA_GND voltage was 2.5 Volts. CSA_GND was held at 4 Volts when the CSA produced negative going output pulses. It is important that CSA_GND be set accordingly to achieve the maximum range over which the responses remain linear. The characterization was performed in the high-gain mode.

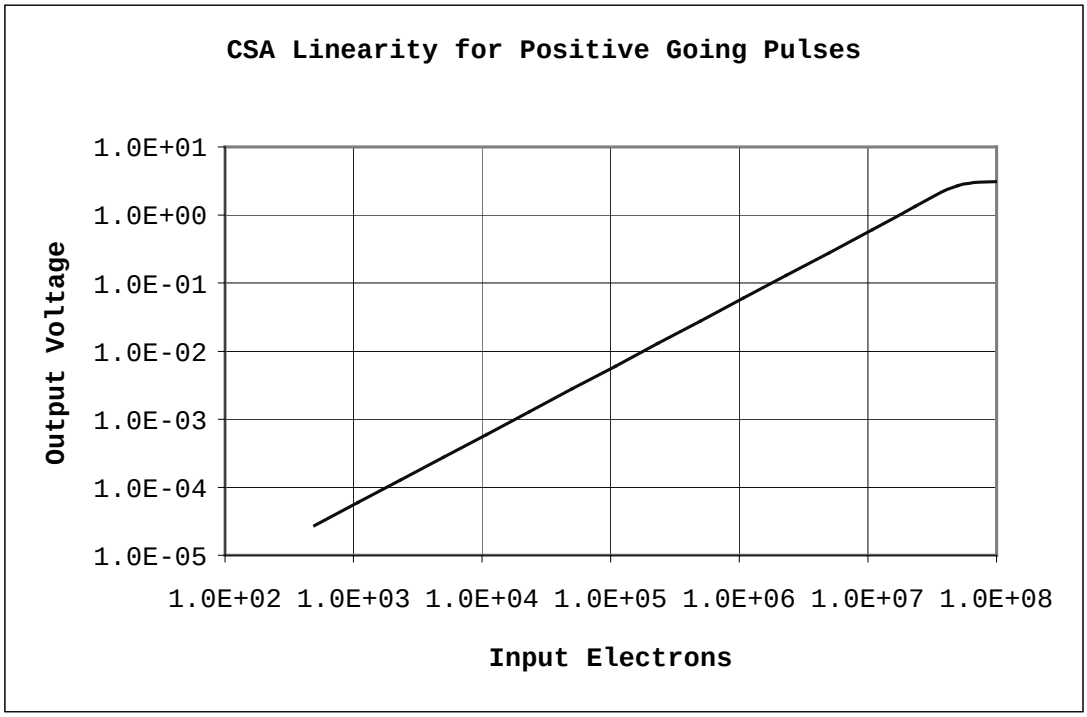


Figure 5: CSA Linearity for Positive Going Output Pulses

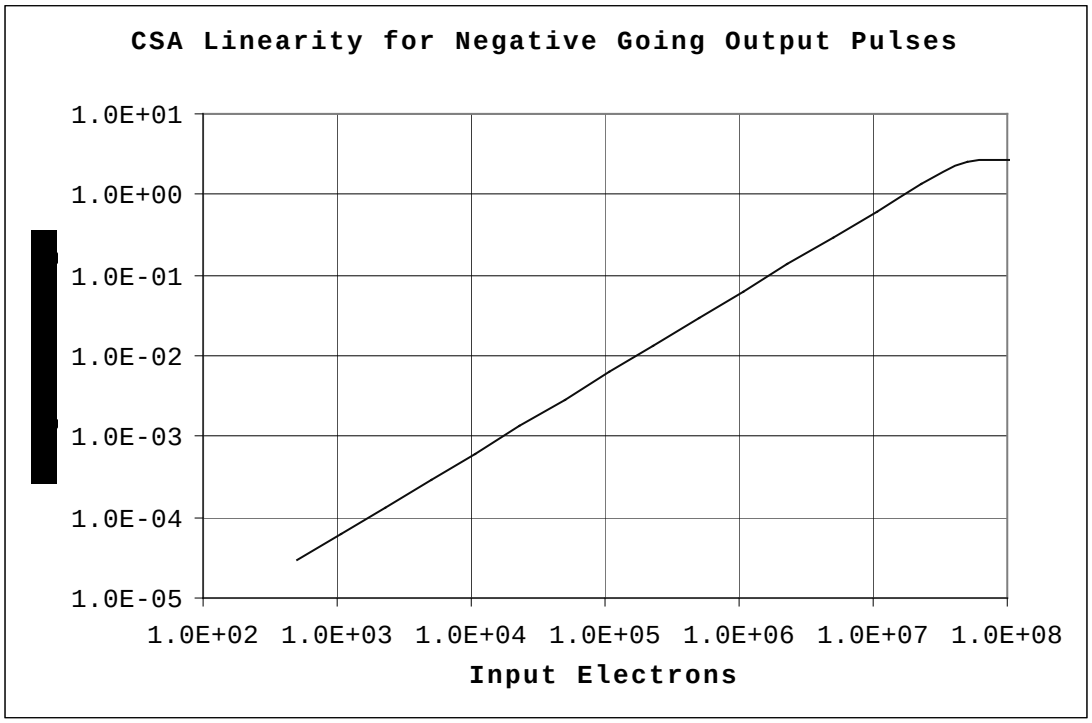


Figure 6: CSA Linearity for Negative Going Output Pulses

2.3 Noise Performance

The noise performance of the CSA (high-gain mode), as a function of detector capacitance, is depicted in Figure 7. The slope of the curve is approximately 12 electrons per pF. The graph represents the total integrated noise in a bandwidth of 10 KHz to 1 MHz (roughly the bandwidth of the shaping filter).

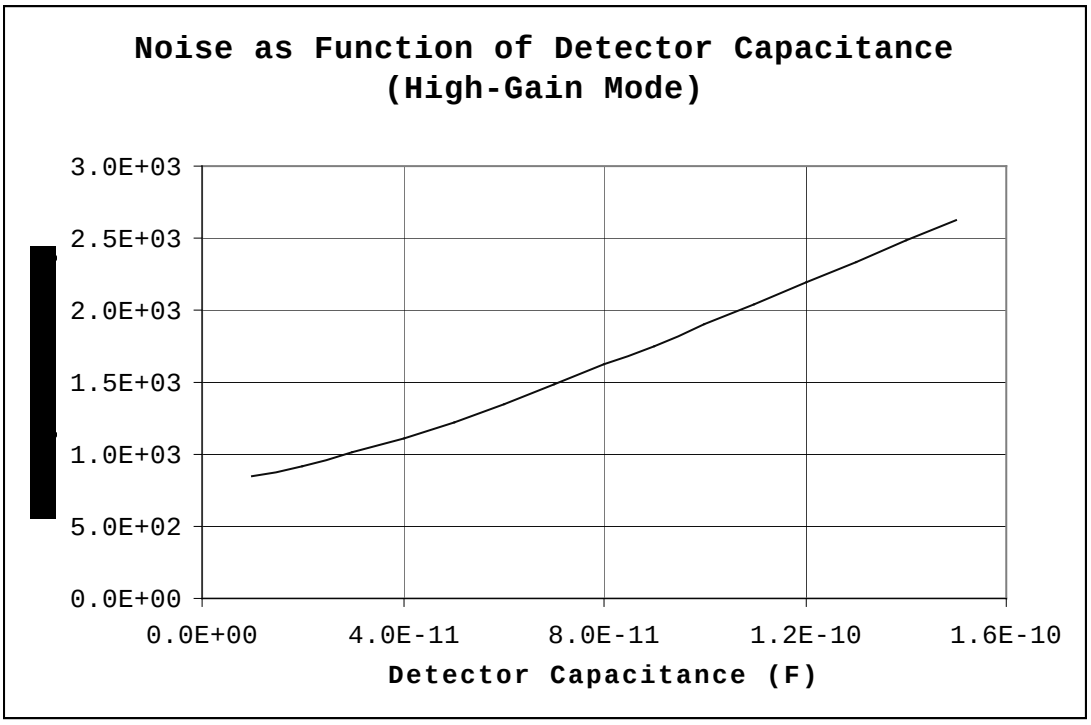


Figure 7: Noise Performance of CSA (high-gain mode) Versus C_{det}

The noise performance of the CSA (high-gain mode), as a function of detector capacitance, is depicted in Figure 8. The slope of the curve is approximately 20 electrons per pF. The graph represents the total integrated noise in a bandwidth of 10 KHz to 1 MHz (roughly the bandwidth of the shaping filter).

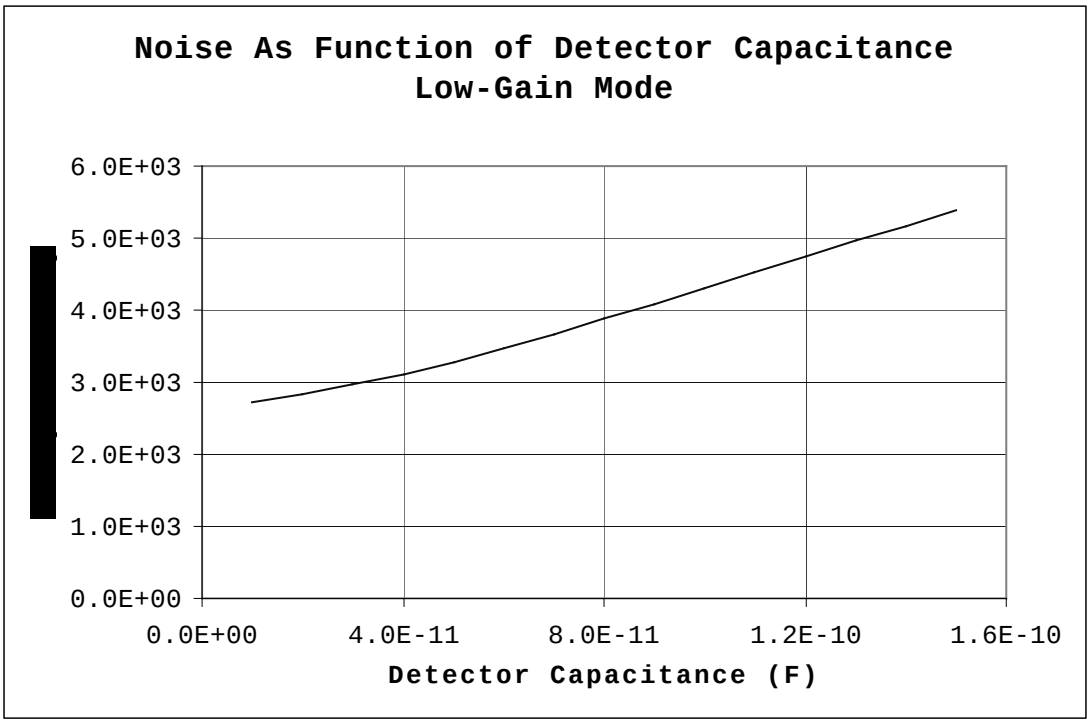


Figure 8: Noise Performance of CSA (low-gain mode) Versus C_{det}

4.0 Pulse Shaper

The exponential pulses at the CSA output are transformed into semi-gaussian shaped pulses by the pulse shaper circuit described herein.

The transfer function for the pulse shaper is

Figure 9: Pulse Shaper Transfer Function

Figure 10: Pulse Shaper Time Domain Response

4.1 Linearity

Figure 11: Pulse Shaper Linearity for Positive Pulses at Input

Figure 12: Pulse Shaper Linearity for Negative Pulses at Input

4.2 Peaking Time

Figure 13: Peaking Time As Function of Control Voltage

4.3 Noise Performance

5.0 Time-to-Voltage Converter (TVC)

5.1 Linearity

The transfer function for the time-to-voltage converter (250 nsec range) is illustrated in Figure 14. The slope of the curve below is 3.85 mV / ns. The DC offset is approximately 1 Volt and represents the threshold voltage of the source follower buffer. The range does not extend to t=0. The range over which the curves linearity is characterized is from t = 3 ns to t = 250 ns. The integral nonlinearity is 440 ps. If a range starting at t = 2 ns is used, the integral nonlinearity increases to 850 ps. If the range starting at t=10 nsec is used, the integral nonlinearity is approximately 50 ps.

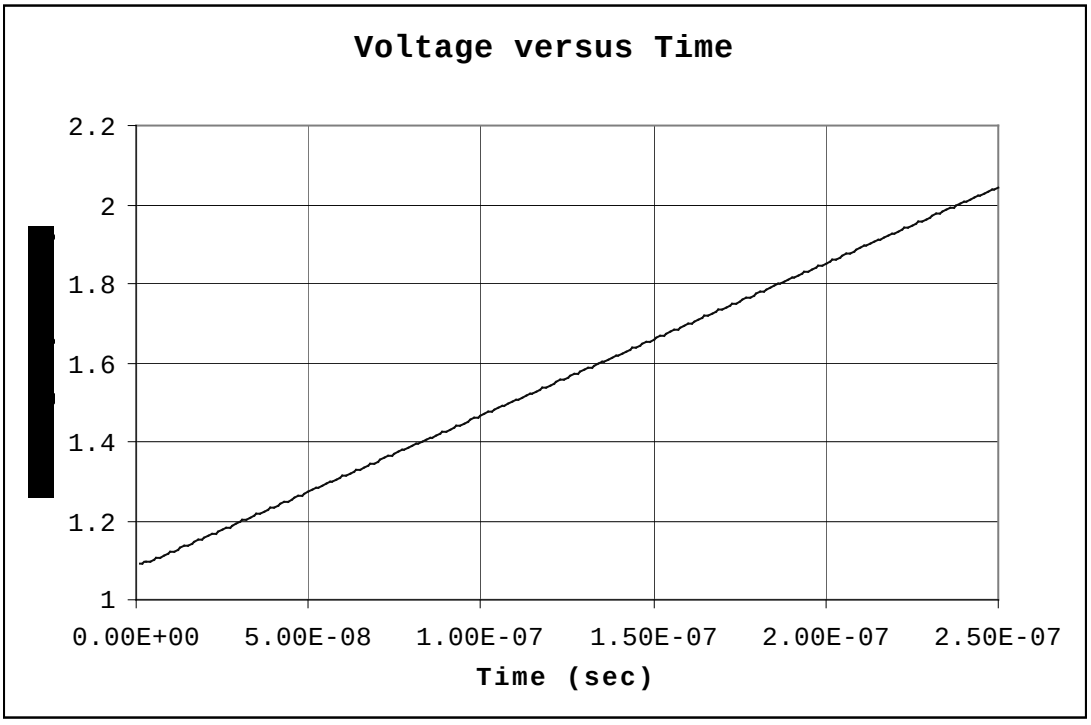


Figure 14: Linearity of TVC (250 nsec range)

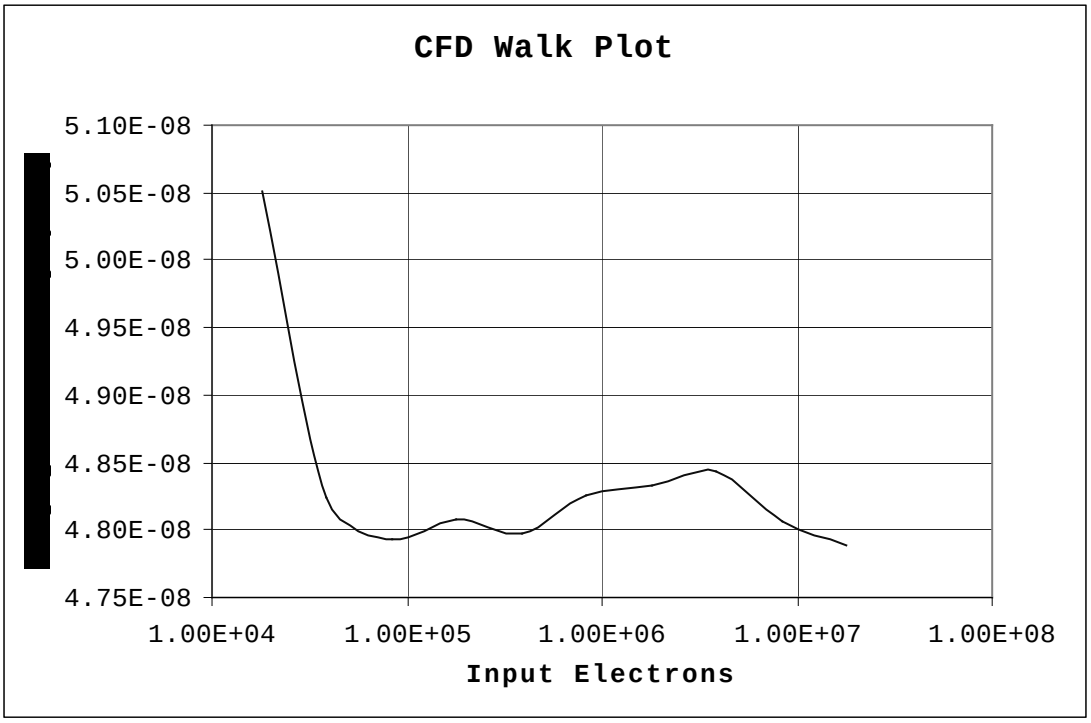
Figure 15: Linearity of TVC (1 μsec range)

5.3 Noise Performance

6.0 Pseudo Constant Fraction Discriminator (CFD)

The pseudo constant fraction discriminator (CFD) displays very good walk characteristics. The CFD was driven with exponential pulses. The risetime was 35 nsec and the falltime was 55 µsec. The pulse amplitude was varied from 1mV to 1V, corresponding to detector inputs ranging from 17,000 to 17e6 electrons.

The simulator maximum timestep was specified as 250 ps. Some of the variation in propagation delay can be attributed to this relative large timestep. The maximum timestep was not made smaller because of the excessive time required to conduct the simulations.



6.1 Zero Cross Disriminator (ZCD)

6.1.1 Differential Amplifier

6.1.2 DC Offset Cancellation

6.1.2.1 Differential-to-Single Ended Conversion

6.1.2.2 Current Attenuator

6.1.2.3 Integrator

6.1.2.4 Single-to-Differential Ended Conversion

6.1.3 Comparator

6.2 Leading Edge Discriminator (LED)

6.2.1 Digital-to-Analog Converter (DAC)

The digital-to-analog converter (DAC) is used to correct offsets associated with the leading edge detector. It consists of a binary weighted array (weights: 1, 2, 4, 8, 16) of current sources and a binary weighted array (weights: 1, 2, 4, 8) of current sinks. The most significant bit, bit 5, indicates the algebraic sign and whether the current sources or current sinks are used. In other words, the data format is sign/magnitude with 5 bits of magnitude in the postive direction and 4 bits in the negative direction.

An output voltage is created by either sourcing or sinking current through a 0.5 kΩ resistor, connected to analog ground (AGND = 2.5 VDC). A maximum positive output voltage of 19.8 mV with respect to AGND can be achieved. The most negative output is -9.9 mV (relative to AGND). The stepsize is approximately 0.625 mV. Settling time (better than 1 %) on the DAC outputs is 1 μsec. The stepsize of 0.625 mV corresponds to roughly 12,000 electrons (need to check this!). Offsets associated with the leading edge discriminator are expected to be 10 mV (3 sigma). This implies that we are guaranteed to be able to set maximum thresholds at least at the 120,000 electron level.

6.2.2 Differential Amplifier

6.3 Hit Logic

7.0 Peak Sampling Circuit

7.1 Non-linear Gain Amplifier

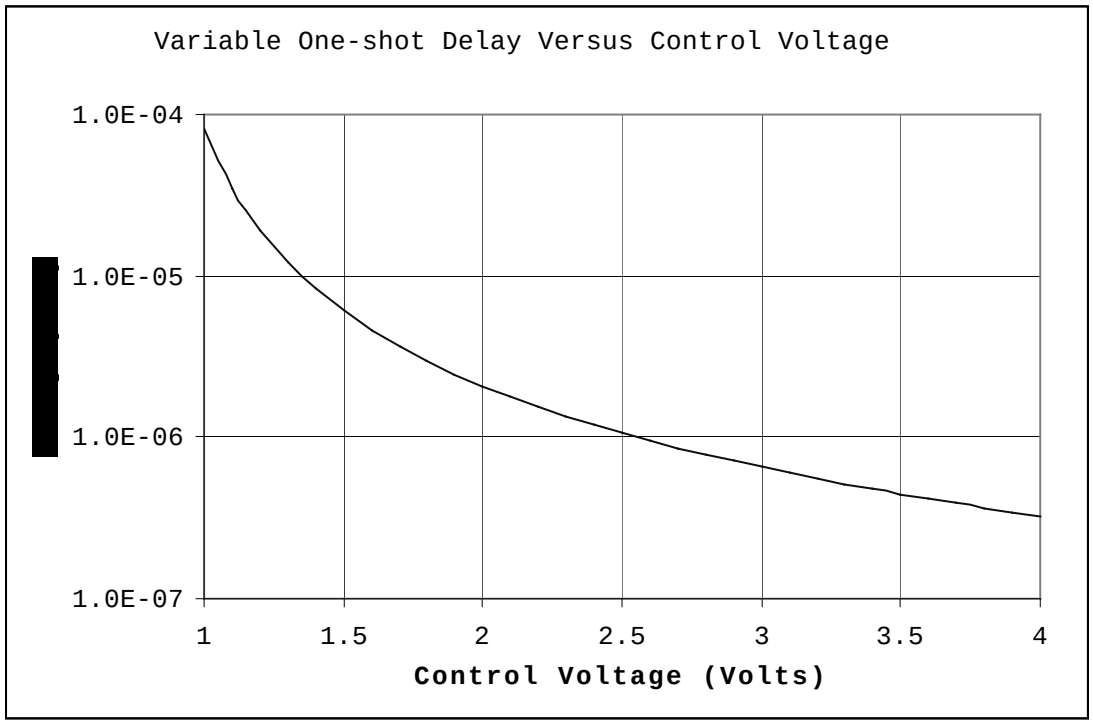
7.2 Leading Edge Discriminator (LED)

7.3 Sample and Hold

8.0 Analog Reset Logic

Automatic reset circuitry has been incorporated into each channel. As discussed earlier, when a channel is hit, the channel's CFD emits a positive-going pulse (generated by a one-shot circuit with a fixed pulse-width) that lasts for approximately 100 ns. This pulse is then used to trigger a second one-shot. This second monostable produces a negative-going pulse with a variable pulse width. The delay, common to all channels on the IC, can be varied by controlling the voltage on the DLY_VC pin. Figure x below illustrates that the delay can be reliably varied from a few hundred nano-seconds to around 100 µsec by varying the control voltage between 1 Volt and 4 Volts. A control voltage of 2.5 Volts yields a delay of 1 µsec which is approximately equal to the peaking time of the shaper.

If the "veto_rst" signal is not asserted prior to the trailing edge of the pulse from this second one-shot, the channel will reset itself. The following events will take place. The "hit" register will be cleared, the time-to-voltage converter will be reset by discharging the internal capacitor, and the peak-sampling circuit will be reset. The "veto_rst" signal must remain asserted until the variable delay time has elapsed.



9.0 Common Digital Logic

In addition to the 32 analog channels there exists a 33rd "channel"(a 9th channel in the case of our 8 channel IC). This additional "channel" contains the common bias circuits described earlier along with digital circuits "common" to all of the channels. This "common" digital circuitry will be described now.

9.1 Configuration Register

The configuration register is a serial shift register that is 48 bits (6 bytes) long. Bit 0 should be loaded **first**. Bit 47 is loaded last. Data should be applied to "sin". Shifting occurs on the **rising** edge of "sclk" and therefore "sin" data must be STABLE and VALID on each **rising** edge of "sclk". Data emerges from the configuration register at the "sout" pin. A positive pulse on the "dig_rst" pin will reset all bits of the configuration register to '0'.

The configuration register bit assignments along with the default state after a digital reset has been performed is provided below:

Bit Position	Function	Default
0	0 = Enable CFD Ch 0 1 = Disable CFD Ch 0	Ch 0 CFD enabled
1	0 = Enable CFD Ch 1 1 = Disable CFD Ch 1	Ch 1 CFD enabled
and so on ...		
31	0 = Enable CFD Ch 31 1 = Enable CFD Ch 31	Ch 31 CFD enabled
32	0 = Positive pulses at CSA out 1 = Negative pulses at CSA out	Negative pulses
33	0 = 1 µsec TVC range 1 = 250 nsec TVC range	1 µsec range
34	0 = CSA high-gain mode 1 = CSA low-gain mode	High-gain mode
35	0 = test mode 1 OFF 1 = test mode 1 ON i.e. CSA and shaper outputs for selected channel brought out to pins	CSA and shaper not brought out to pins
36	0 = Enable internal CSA 1 = Select external preamp	Use internal CSA
37	0 = test mode 3 OFF 1 = test mode 3 ON Peak sampling circuit of	Test mode 3 OFF

	Selected channel driven by External signal	
38 – 39	Currently unused	All bits 0
40 - 47	Bit 47 MS bit (8 bit ID)	Chip ID = 0

9.2 Encoder

This is a 32 – 5 encoder. The output is a binary code that indicates which of the 32 input lines is active (HIGH) *i.e.* which of the 32 channels is currently in need of attention. If none of the 32 inputs are active, the output code is “00000”. This is NOT a priority encoder. If more than one input is HIGH, the output code is UNKNOWN. In normal operation, it is not possible for more than one input to be simultaneously HIGH. One line from each of the 32 channels, encoder output, is routed to the 32-5 encoder that is located within the *common* digital block within the special *common* channel.

In the current 16channel IC, only inputs 0 – 15 are used. Inputs 16 – 31 are connected to ground.

9.3 Decoder

This is a 5 – 32 decoder. The 5 bit input address determines which of the 32 output lines is active, thereby selecting one of the 32 channels. One (and only one) of the 32 lines is always “hot’. The decoder outputs are the channel select lines. One of the 32 channels can be selected by applying the appropriate 5 bit channel code to this decoder.

In the current 16 channel IC, outputs 16 – 31 are NOT connected.

9.4 Address MUX

The address MUX is used to multiplex two 5 bit addresses. One 5-bit address is the output of the 32 – 5 encoder described above. The other 5 bit code is an externally generated address. The “sel_ext_addr” signal selects the externally generated address.

9.5 Address Latch

It is possible to latch the externally applied address. This allows the external address lines to be used as data lines for the DACs that are used for offset compensation in the leading edge detectors.

The address latch is transparent when the “dac_stb” signal is LOW. On the *rising* edges of “dac_stb”, the external address is latched. Data intended for the DACs will be latched on the *falling* edge of dac_stb. Care was taken to make sure that the delays are such that the data is latched into the DAC register before the channel select lines change.

9.6 Status Circuits

The IC has circuits that can report the current status of the IC. The IC can notify the external world that at least one of the channel *hit* registers has been set. This is accomplished by ORing the outputs of the 32 *hit* registers. The OR function is distributed across the channels. The pulldown transistors reside in the respective channels. There is one common pullup device along with an inverter located in the common digital block. The "or_out" pin when HIGH indicates that at least one channel on the IC has been hit.

In a similar manner, the "acq_ack" pin indicates whether an acquisition is currently in progress. The falling edge of "acq_ack" signals the end of data acquisition.

The acquisition process is initiated when the "token_in" pin is driven LOW.

While the "or_out" pin is an indicator of whether or not any channel on the IC has been hit, the "MULTIPLICITY" output is an analog voltage that is proportional to the number of channels that currently have there hit registers set. A 40 µA current source is switched onto a 75 KΩ resistor to AVSS in every channel whose hit register is set. These outputs are then tied together and buffered by source follower in the *common* channel. Therefore, the MULTIPLICITY output voltage is given by the following relationship:

MULTIPLICITY = (40 uA * 75 KΩ) / N + (DC offset)
= 3 Volts / N + 1 Volt

where N is the number of IC channels. For the eight channel IC, this becomes

MULTIPLICITY = 375 mV / channel + 1 Volt

10.0 Pin Descriptions

Pin number: 1
Pin name: **cfd_out**
Pin type: Digital output
Description: This is the output (for the selected channel) of the 100 ns one-shot that is triggered by the narrow output pulse from the CFD. The CFD outputs from all 32 channels are multiplexed. This is the output of the multiplexer.

Pin number: 2
Pin name: **acq_clk**
Pin type: Digital input
Description: This is the clock signal used for acquisition. The rising edge of “acq_clk” causes the active register to be set in a channel whose “hit” register is set AND whose “token_in” is active i.e. LOW. The falling edge of “acq_clk” in turn causes the “hit” register to be cleared. This is turn will potentially allow the “token_out” of the channel to be active i.e. LOW; thereby, enabling the next channel in the chain. The next rising edge of “acq_clk” will clear the active register.

Pin number: 3
Pin name: **a0**
Pin type: Bidirectional
Description: This is external address line a0. When the “sel_ext_addr” pin is HIGH, this line will be a DIGITAL INPUT and is the least significant bit of the address of the channel the user wishes to select. When the “sel_ext_addr” pin is LOW, this line will be a DIGITAL OUTPUT and will be the least significant bit of the address of the channel that is currently in need of attention.

Pin number: 4
Pin name: **a1**
Pin type: Bidirectional
Description: This is external address line a1. See discusion for address line a0.

Pin number: 5
Pin name: **a2**
Pin type: Bidirectional
Description: This is external address line a2. See discusion for address line a0.

Pin number: 6
Pin name: **a3**
Pin type: Bidirectional
Description: This is external address line a3. See discusion for address line a0.

Pin number: 7
Pin name: **a4**
Pin type: Bidirectional
Description: This is external address line a4. See discusion for address line a0.

Pin number: 8
Pin name: **or_out**
Pin type: Digital output
Description: The “or_out” pin will be HIGH if any hit register on the chip is set. A LOW on this pin indicates that NONE of the “hit” registers is set.

Pin number: 9
Pin name: **acq_ack**
Pin type: Digital output
Description: The “acq_ack” pin will be HIGH during the acquisition process and will go LOW once all channels have been acquired.

Pin number: 10
Pin name: **token_in**
Pin type: Digital input
Description: This is the token into the chip. It is active LOW.

Pin number: 11
Pin name: **token_out**
Pin type: Bidirectional
Description: This is the token_out of the chip. It is active LOW. When the line is high, an acquisition is in progress.

Pin number: 12
Pin name: **veto_rst**
Pin type: Digital input
Description: After a channel has been hit, the time-to-voltage and peak sampling circuits as well as the hit and active registers will automatically be reset UNLESS “veto_rst” is asserted (HIGH). The “veto_rst” signal must be continued to be asserted until the time when the automatic reset would have taken place.

Pin number: 13
Pin name: **force_rst**
Pin type: Digital input
Description: A positive going pulse on this line will reset the time-to-voltage and peak sampling circuits as well as the hit and active registers in ALL channels.

Pin number: 14
Pin name: **common_stop**
Pin type: Digital input
Description: When HIGH, halts the time-to-voltage converter in every channel. The time-to-voltage conversions will STOP even if the start conversion signal is still asserted.

Pin number: 15
Pin name: **global_cfd_en**
Pin type: Digital input
Description: When LOW, the CFDs for all channels are DISABLED. When HIGH, a channel’s CFD will be enabled provided the corresponding CFD enable bit is a ‘0’ in the configuration register.
IMPORTANT NOTE: After the "global_cfd_en" line is made active, it important that a reset be forced. This is accomplished by applying a positive pulse to the “force_rst” pin.

Pin number: 16
Pin name: **DGND1**
Pin type: Digital supply pin. Return currents for digital I/O pads.
Description: Connect to circuit ground.

Pin number: 17
Pin name: **DVDD1**
Pin type: Digital supply pin. Powers digital I/O pads.
Description: Connect to +5VDC.

Pin number: 18
Pin name: **id0**
Pin type: Bidirectional.
Description: Bit 0 of the chip identification code. Least significant bit. When "sel_ext_addr" is HIGH, id0 is an *input*.

Pin number: 19
Pin name: **id1**
Pin type: Bidirectional.
Description: Bit 1 of the chip identification code. When "sel_ext_addr" is HIGH, id1 is an *input*.

Pin number: 20
Pin name: **id2**
Pin type: Bidirectional.
Description: Bit 2 of the chip identification code. When "sel_ext_addr" is HIGH, id2 is an *input*.

Pin number: 21
Pin name: **id3**
Pin type: Bidirectional.
Description: Bit 3 of the chip identification code. When "sel_ext_addr" is HIGH, id3 is an *input*.

Pin number: 22
Pin name: **id4**
Pin type: Bidirectional.
Description: Bit 4 of the chip identification code. When "sel_ext_addr" is HIGH, id4 is an *input*.

Pin number: 23
Pin name: **id5**
Pin type: Bidirectional.
Description: Bit 5 of the chip identification code. When "sel_ext_addr" is HIGH, id5 is an *input*.

Pin number: 24
Pin name: **id6**
Pin type: Bidirectional.
Description: Bit 6 of the chip identification code. When "sel_ext_addr" is HIGH, id6 is an *input*.

Pin number: 25
Pin name: **id7**
Pin type: Bidirectional.
Description: Bit 7 of the chip identification code. When "sel_ext_addr" is HIGH, id7 is an *input*.

Pin number: 26
Pin name: **sel_ext_addr**
Pin type: Digital input

Description: When HIGH, this signal selects the external address as input to the 5-32 decoder used for selecting one of the 32 channels. When HIGH, makes a0-a5 lines as well as id0-id7 lines *inputs*.

Pin number: 27
Pin name: **dac_stb**
Pin type: Digital input
Description: Data on the address pins (a0-a5) are latched into an internal address latch on the rising edge of dac_stb. When dac_stb is high, data on the ext_addr lines will alter the DAC output whose channel is select by the address stored in the internal address latch. On the falling edge the data on the address pins will be latched into the DAC register.
IMPORTANT NOTE: Data on address lines a0-a5 must be stable and valid on both rising and falling edge of "dac_stb".

Pin number: 28
Pin name: **dac_sgn**
Pin type: Digital input
Description: While the magnitude of the DAC value is placed on the bidirectional external address lines (a0-a5), the algebraic sign has a dedicated input pin

Pin number: 29
Pin name: **rst**
Pin type: Digital input
Description: Master reset. Resets all of the digital logic. All bits of the configuration register are cleared. All of the DAC registers on chip are also cleared.

Pin number: 30
Pin name: **acq_all**
Pin type: Digital input
Description: A positive-going pulse will set the "hit" register in each of the channels. This can be useful if one wants to force the acquisition of all channels on chip. AT PRESENT THERE IS NO WAY TO SET THE HIT REGISTER IN ANY ONE CHANNEL (other than by having the CFD fires). Do we need to change this?????

Pin number: 31
Pin name: **sout**
Pin type: Digital output
Description: Serial output from 48-bit configuration register.

Pin number: 32
Pin name: **sin**
Pin type: Digital input
Description: Serial clock for 48-bit configuration register. Data on "sin" pin must be valid on rising edge of "sclk".

Pin number: 33
Pin name: **sclk**
Pin type: Digital input
Description: Serial clock for 48-bit configuration register. Data on "sin" pin must be valid on rising edge sclk.

Pin number: 34
Pin name: **force_track**
Pin type: Digital input

Description: When active (HIGH) forces all peak sampling circuits into track mode even if CFDs have not fired. Force_track must be asserted 500 nsec prior to peaking of shaper circuits. Must be held active until all data has been acquired. Releasing force_track causes a reset of peak sampling circuit.

Pin number: 35
Pin name: **quiet**
Pin type: Digital input
Description: When active (HIGH) mutes analog portions of CFD circuits.

Pins 36: UNUSED

Pin number: 37
Pin name: **AVSS**
Pin type: Analog input
Description: Connect to circuit ground.

Pin number: 38
Pin name: **AVDD**
Pin type: Analog supply pin.
Description: Connect to +5VDC. Supplies power to shaper, peak sampling and full bias circuits.

Pin number: 39
Pin name: **EXT_SHAPER**
Pin type: Analog input
Description: Can be used to apply a simulated SHAPER signal to the PEAK SAMPLING circuit. For this to happen the configuration register bit 37 should be active high.

Pins 40-43: UNUSED

Pin number: 44
Pin name: **EVEN_PULSER**
Pin type: Analog input
Description: Pulser input for even channels (0.2, 4, 6, etc.)

Pin number: 45
Pin name: **ODD_PULSER**
Pin type: Analog input
Description: Pulser input for odd channels (1, 3, 5, 7, etc.)

Pin number: 46
Pin name: **PULSER_AVDD**
Pin type: Analog input
Description: Connect to +5VDC.

Pin number: 47
Pin name: **PULSER_AVSS**
Pin type: Analog input
Description: Connect to circuit ground.

Pin number: 48
Pin name: **CH_IN15**
Pin type: Analog input
Description: Channel 15 detector input

Pin number: 49
Pin name: **CH_IN14**

Pin type: Analog input
Description: Channel 14 detector input

Pin number: 50
Pin name: **CH_IN13**
Pin type: Analog input
Description: Channel 13 detector input

Pin number: 51
Pin name: **CH_IN12**
Pin type: Analog input
Description: Channel 12 detector input

Pin number: 52
Pin name: **CH_IN11**
Pin type: Analog input
Description: Channel 11 detector input

Pin number: 53
Pin name: **CH_IN10**
Pin type: Analog input
Description: Channel 10 detector input

Pin number: 54
Pin name: **CH_IN9**
Pin type: Analog input
Description: Channel 9 detector input

Pin number: 55
Pin name: **CH_IN8**
Pin type: Analog input
Description: Channel 8 detector input

Pin number: 56
Pin name: **CSA_GND**
Pin type: Analog input
Description: This is a signal ground for the CSA circuits. For negative-going pulses at output of CSA, connect to 4.0 VDC. If processing positive-going pulses, connect to 2.5 VDC.

Pin number: 57
Pin name: **CSA_AVSS**
Pin type: Analog supply pin
Description: Connect to circuit ground

Pin number: 58
Pin name: **CSA_AVDD**
Pin type: Analog supply pin
Description: Connect to +5VDC.

Pin number: 59
Pin name: **CH_IN7**
Pin type: Analog input
Description: Channel 7 detector input

Pin number: 60
Pin name: **CH_IN6**
Pin type: Analog input
Description: Channel 6 detector input

Pin number: 61
Pin name: **CH_IN5**

Pin type: Analog input
Description: Channel 5 detector input

Pin number: 62
Pin name: **CH_IN4**
Pin type: Analog input
Description: Channel 4 detector input

Pin number: 63
Pin name: **CH_IN3**
Pin type: Analog input
Description: Channel 3 detector input

Pin number: 64
Pin name: **CH_IN2**
Pin type: Analog input
Description: Channel 2 detector input

Pin number: 65
Pin name: **CH_IN1**
Pin type: Analog input
Description: Channel 1 detector input

Pin number: 66
Pin name: **CH_IN0**
Pin type: Analog input
Description: Channel 0 detector input

Pins 67-135: UNUSED

Pin number: 136
Pin name: **AVDD1**
Pin type: Analog supply pin. Supplies power for the above.
Description: Connect to +5VDC.

Pin number: 137
Pin name: **AVSS1**
Pin type: Analog supply pin. Return currents for channels 0-7 for TVC circuits
Description: Connect to circuit ground.

Pin number: 138
Pin name: **TVC_OUT**
Pin type: Analog output
Description: Analog output voltage proportional to the duration of time that has elapsed between the channel being hit (the one presently selected) and the assertion of the “common_stop” signal.

Pin number: 139
Pin name: **PEAK_OUT**
Pin type: Analog output
Description: Peak amplitude of shaper signal for the selected channel.

Pin number: 140
Pin name: **CSA_OUT**
Pin type: Analog output
Description: CSA output for the selected channel. Only available if the “test mode” bit in the configuration register is a ‘1’.

Pin number: 141

Pin name: **SHAPER_OUT**
Pin type: Analog output
Description: Shaper output for the selected channel. Only available if the “test mode” bit in the configuration register is a ‘1’.

Pin number: 142
Pin name: **DLY_VC**
Pin type: Analog input
Description: Control voltage that determines the time delay between a channel being hit and the automatic reset of the time-to-voltage converter, the peak sampling circuit, and the active and hit registers in that channel.

Pin number: 143
Pin name: **DGND**
Pin type: Digital supply pin for above.
Description: Connect to circuit ground.

Pin number: 144
Pin name: **DVDD**
Pin type: Digital supply pin for common digital circuits, CFDs, and reset logic
Description: Connect to +5VDC.

Pin number: 145
Pin name: **PEAK_TIME**
Pin type: Analog input
Description: Control voltage for shaper peaking time. Set to 2.5 VDC for a 1 •sec peaking time (approximate).

Pin number: 146
Pin name: **MULTIPLICITY**
Pin type: Analog output
Description: Analog output voltage proportional to the number of channels whose hit registers are currently set.

Pin number: 147
Pin name: **AGND**
Pin type: Analog input
Description: Analog ground (2.5 Volts)

Pin number: 148
Pin name: **TVC_CAP_GND**
Pin type: Analog input
Description: Connect to a clean circuit ground.

Pin number: 149
Pin name: **AVDD2**
Pin type: Analog supply pin. Supply for channels 8-15 TVC circuits.
Description: Connect to +5VDC.

Pin number: 150
Pin name: **AVSS2**
Pin type: Analog supply pin. Return currents for channels 8-15 TVC circuits.
Description: Connect to circuit ground.

Pin number: 151
Pin name: **SUBSTRATE**
Pin type: Analog input

Description:	Biases silicon substrate. Connect to clean circuit ground.
Pins 152-160:	UNUSED