

Design of a Restartable Clock Generator for Use in GALS SoCs

Masters Thesis Defense

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Design Team

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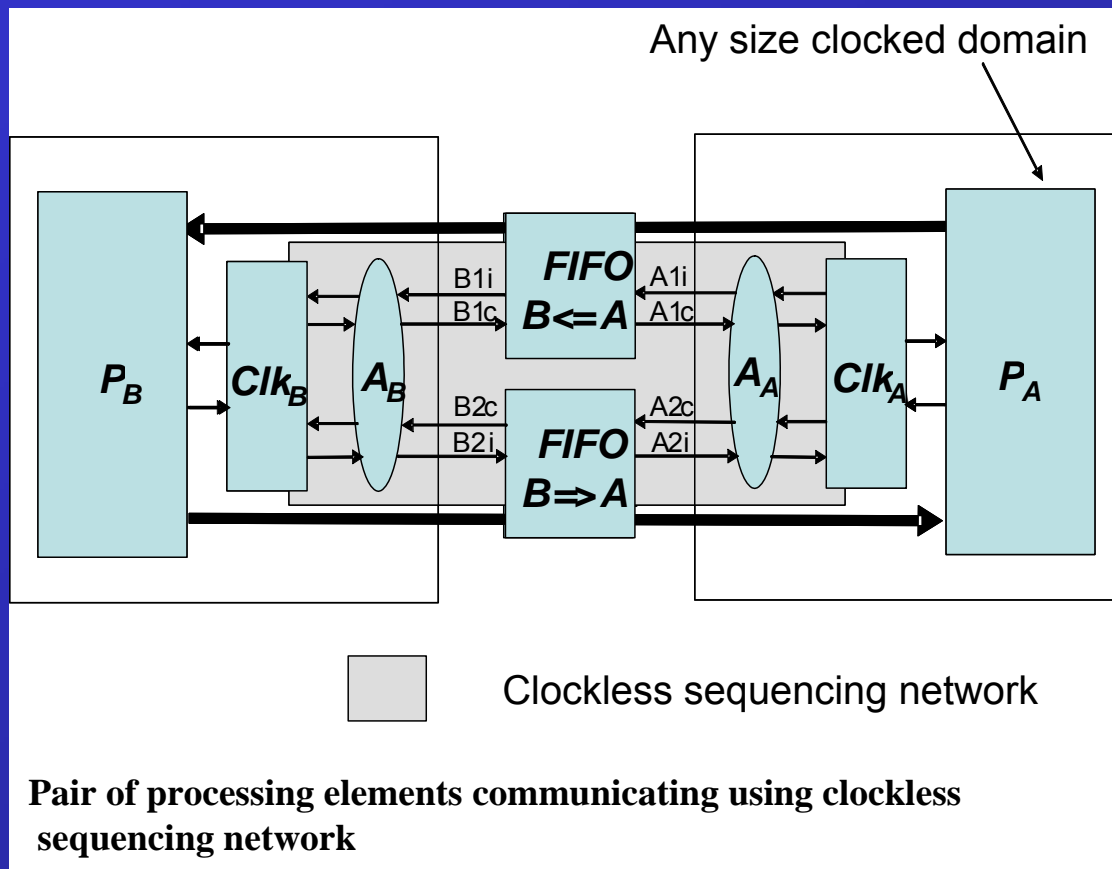
Blendics Integrated Circuit Systems, LLC

- ❑ President. Jerry Cox

Background

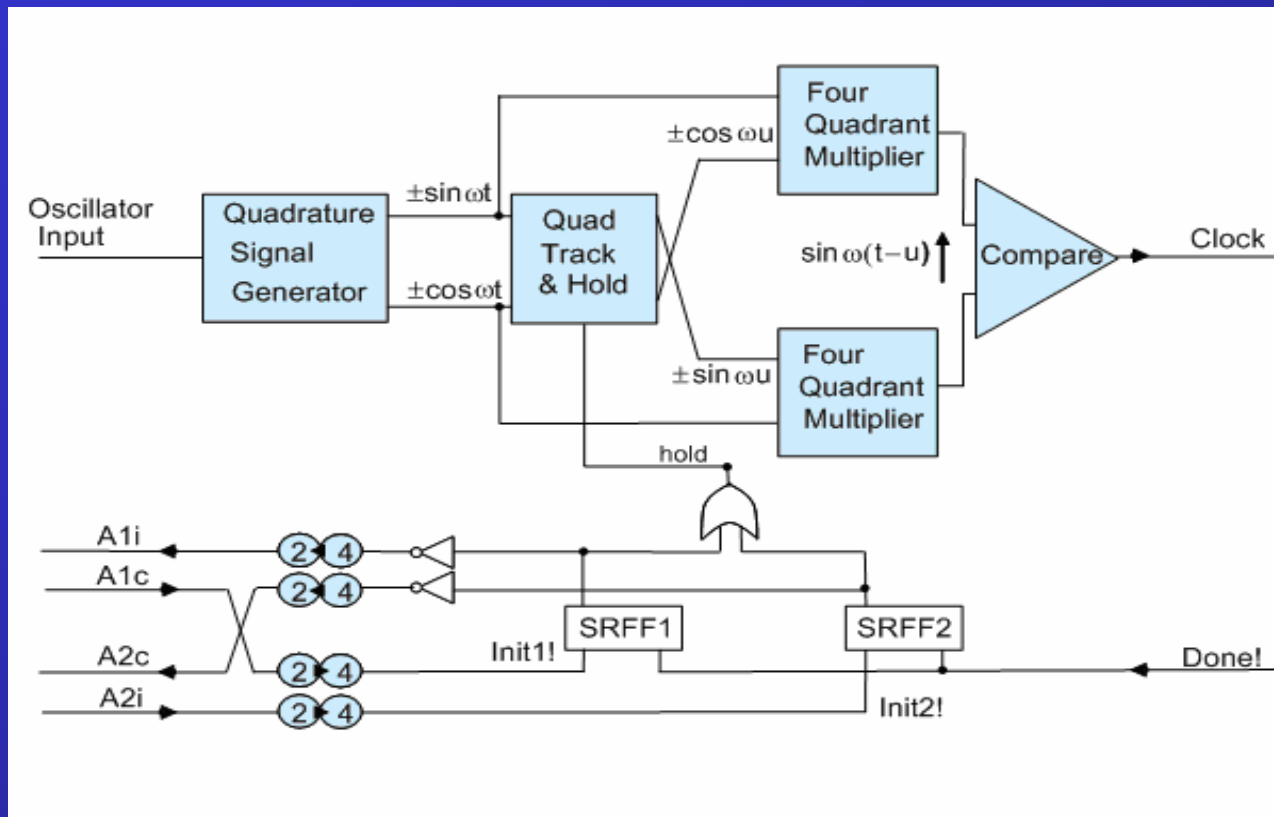
- Verification occupies 60% to 80% of the engineering hours expended on the design of complex integrated circuits (ICs).
- Module reuse along with elimination of the global verification component of chip design has the potential to cut the design time of future ICs.
- Develop a novel methodology that blends clockless and clocked systems and eliminates the need for global verification. It is a special case of the Globally Asynchronous, Locally Synchronous (GALS) design approach.

Blended Design methodology



- The clock generator serves as a local clock to the data processing subsystem.
- A clockless sequencing network between the two subsystems to initiate the operation of the data processing subsystem's local clock, and to signal an acknowledgment of the completion of that action.
- Avoids synchronizer failures by stopping the clock and then restarting it when data is valid.

Clock Generator

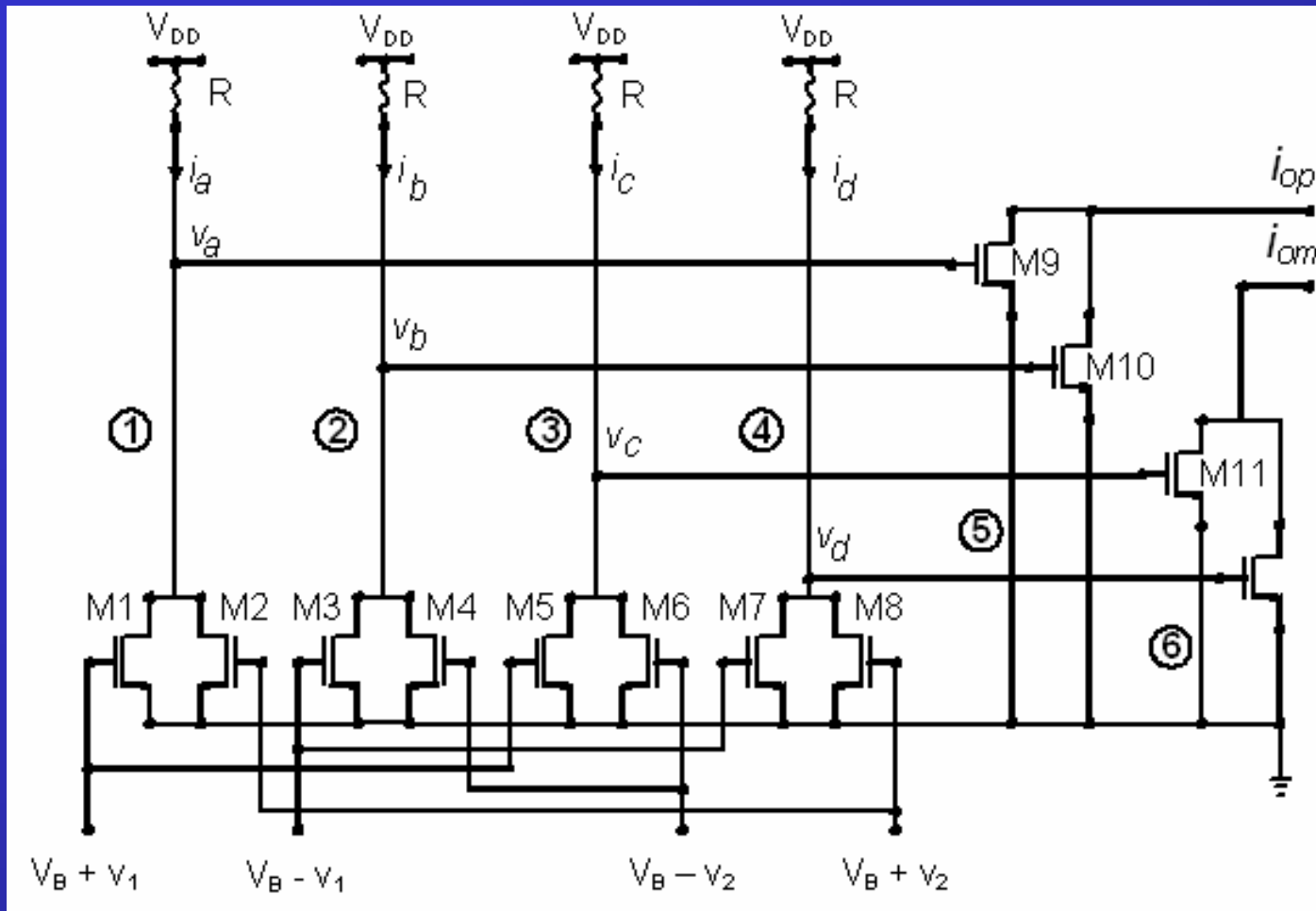


The operation of the clock generator is based on the simple trigonometric identity, $\sin \omega(t-u) = \sin \omega t \cdot \cos \omega u - \cos \omega t \cdot \sin \omega u$

Clock generator

- Constructed from a pair of fully-differential analog multipliers, a comparator, a quad track-and-hold (T/H) circuit, a pair of SR latches, and an OR gate.
- The restartable clock can be stopped and then restarted at an arbitrary phase of the source.
- Can be connected to an external crystal oscillator or a local all-silicon, MEMS-based oscillator as input sources.

Initial Analog Multiplier



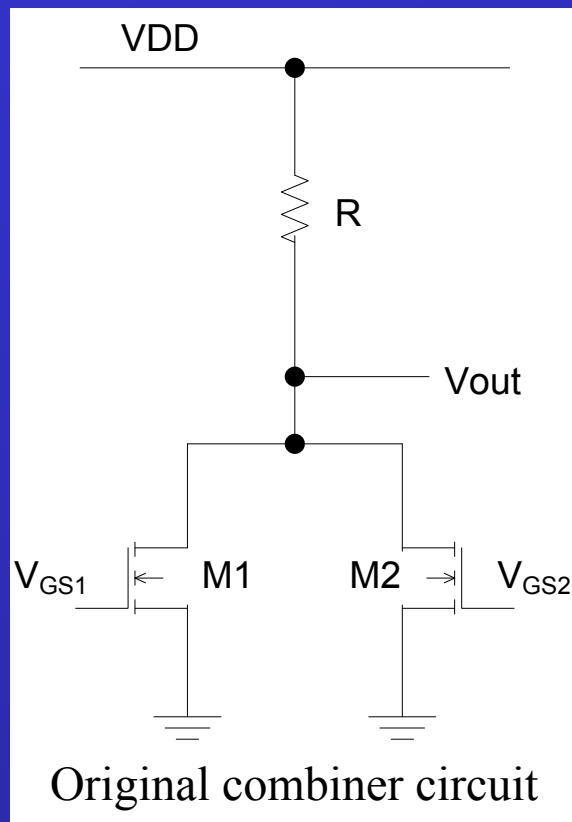
First presented by Hsiao and Wu in their paper “A parallel structure for CMOS four-quadrant analog multiplier and its application to a 2-GHz RF down-conversion mixer” in 1998.

Initial Analog Multiplier

- Consist of six combiners which has a symmetrical structures because they combine the input signals to form the output.
- V_B is the DC pedestal on which the input signals rest.
- Multiplication of two signals, v_1 and v_2 is achieved through the use of the quarter-square principle shown below

$$x \cdot y = \frac{1}{4}[(x + y)^2 - (x - y)^2]$$

Original Combiner Design



- The Square Law characteristic of a MOS transistor

$$i_{DS} = \frac{1}{2n} \cdot K_{pn} \cdot S_n \cdot (v_{GS} - V_{TN})^2$$

- One of the voltage outputs of the “first stage” combiner

$$v_{out} = \frac{-R}{2n} \cdot K_{pn} \cdot S_n (V_B + v_1 - V_{TN})^2 + \frac{-R}{2n} \cdot K_{pn} \cdot S_n (V_B + v_2 - V_{TN})^2 + V_{DD}$$

The Output Current of the Multiplier

- The output currents i_{op} and i_{om}

$$i_{op} = \frac{S_n \cdot K_{pn}}{2n} [v_a^2 + v_b^2 - 2V_{TN} \cdot (v_a + v_b) + 2V_{TN}^2]$$

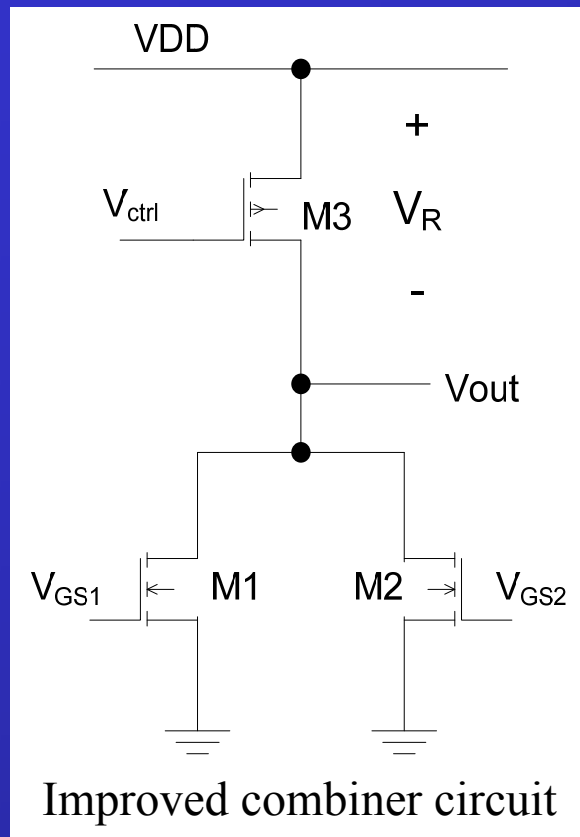
$$i_{om} = \frac{S_n \cdot K_{pn}}{2n} [v_c^2 + v_d^2 - 2V_{TN} \cdot (v_c + v_d) + 2V_{TN}^2]$$

- The differential output current of the multiplier, i_{out}

$$i_{out} = K_{mult} \cdot v_1 \cdot v_2$$

$$\text{where } K_{mult} = 4 \left[\left(\frac{S_n \cdot K_{pn}}{n} \right)^3 \cdot R^2 \cdot (V_B - V_{TN})^2 \right]$$

Improved Analog Multiplier



- The real resistor is replaced by a PFET transistor working in resistive region.

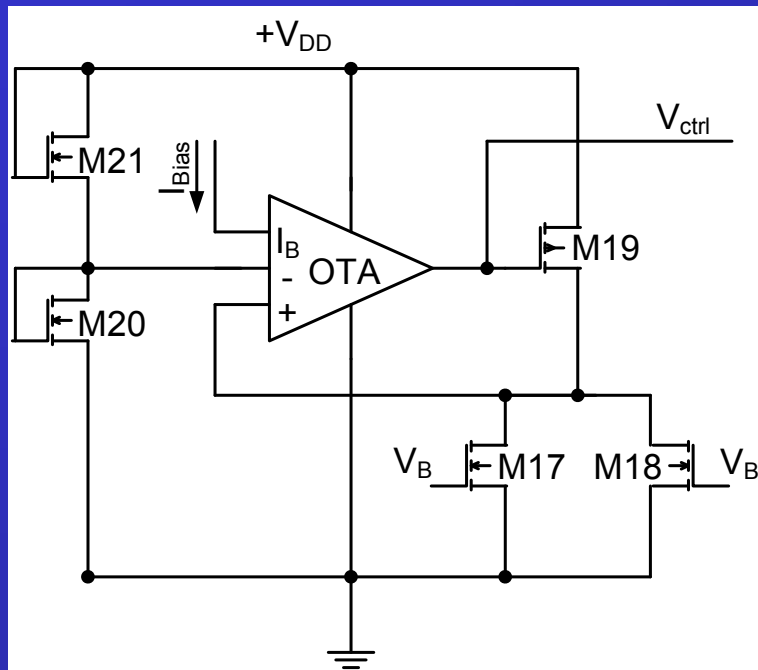
$$R_{eq} = \frac{n}{K_{pp} \cdot S_p \cdot (V_{DD} - V_{ctrl} - |V_{TP}|)}$$

- Re-written expression of K_{mult}

$$K_{mult} = \left[\frac{2V_R}{(V_B - V_{TN})} \right]^2 \left(\frac{S_n \cdot K_{pn}}{n} \right)$$

- By adjusting the control voltage, V_{ctrl} , the resistance can be altered in order that the DC voltage, V_R , across device M_3 is tuned to the desired value.

Automatic gain control circuit for resistive PFET



- Voltage divider M_{20} & M_{21}
- Symmetric Miller type – Operational Transconductance Amplifier (OTA)
- Negative feedback loop to generate the control voltage V_{ctrl}

Sensitivity Analysis

Estimated and simulated results in multipliers

Process Corners	Initial analog multiplier		Improved analog multiplier	
	$\frac{\Delta I_{out_est}}{I_{out_est}}$	$\frac{\Delta I_{out_sim}}{I_{out_sim}}$	$\frac{\Delta I_{out_est}}{I_{out_est}}$	$\frac{\Delta I_{out_sim}}{I_{out_sim}}$
Typical		0		0
Best	54%	26%	-6.5%	0.5%
Worst	-48%	-57%	17.6%	-3.1%

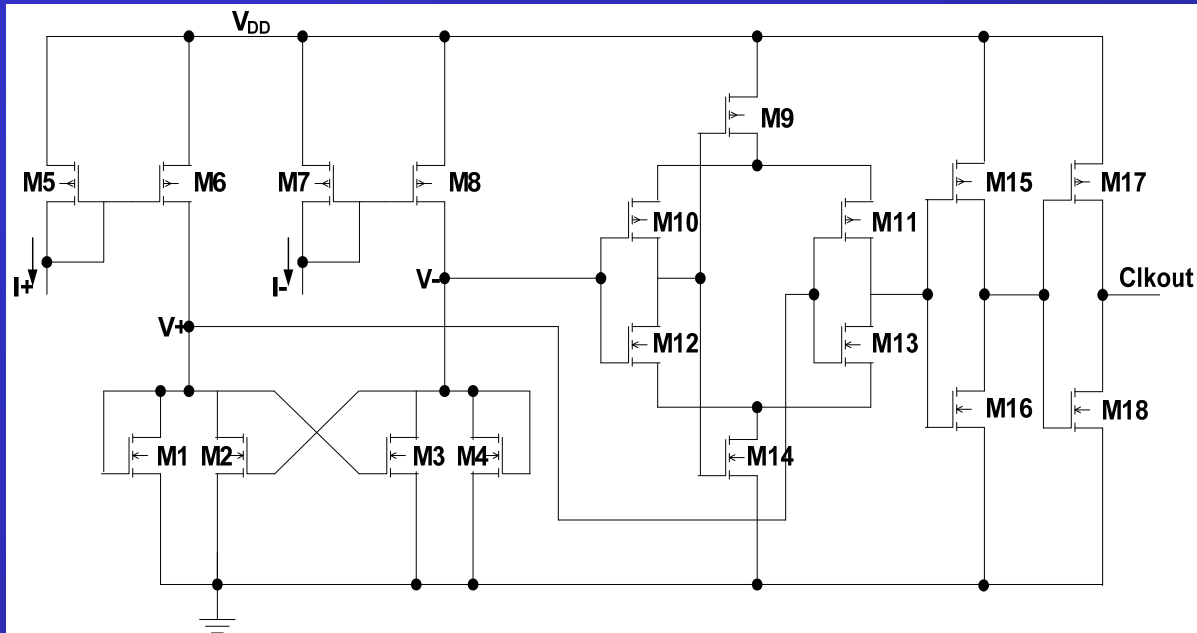
➤ For initial multiplier:

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\Delta K_{mult}}{K_{mult}} = 2 \cdot \frac{\Delta R}{R} + 3 \cdot \frac{\Delta K_{pn}}{K_{pn}} - 2 \cdot \frac{V_{TN}}{V_B - V_{TN}} \cdot \frac{\Delta V_{TN}}{V_{TN}}$$

➤ For improved multiplier:

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\Delta K_{mult}}{K_{mult}} = \frac{\Delta K_{pn}}{K_{pn}} + \frac{2 \cdot V_{TN}}{V_B - V_{TN}} \cdot \frac{\Delta V_{TN}}{V_{TN}}$$

High-Speed Comparator



- Current Mirror
- High-Speed NFET latch
- Self-biased differential amplifier
- Push-pull output drivers

Non Ideal Effects

- Channel length modulation
- Mismatch and offset analysis

Channel length Modulation

- The I - V characteristic of a FET does not fit in the ideal square law.

$$i_{DS} = \frac{1}{2n} \cdot K_{pn} \cdot S_n \cdot (v_{GS} - V_{TN})^2$$

- Factor $(1 + \lambda v_{DS})$ should be considered. λ represents the channel length modulation factor which is inversely proportional to the length of the device, L .

- The multiplier gain

$$K_{mult} = \left[\frac{2V_R}{(V_B - V_{TN})[1 + \lambda \cdot (V_{DD} - V_R)]} \right]^2 \left(\frac{S_n \cdot K_{pn}}{n} \right)$$

Comparison of simulation results

		Mathcad		Electrical Simulation
		With λ	Without λ	
Output of the multiplier's first-stage combiner	I_{Req}	680 μA	604 μA	706 μA
	V_{BO1}	0.5 V	0.5 V	0.49 V
Peak-to-peak output	I_{out}	1.49mA	1.59mA	1.53mA

Note: I_{Req} is DC drain-to-source current of PFET $M3$ in the multiplier's first-stage combiners.

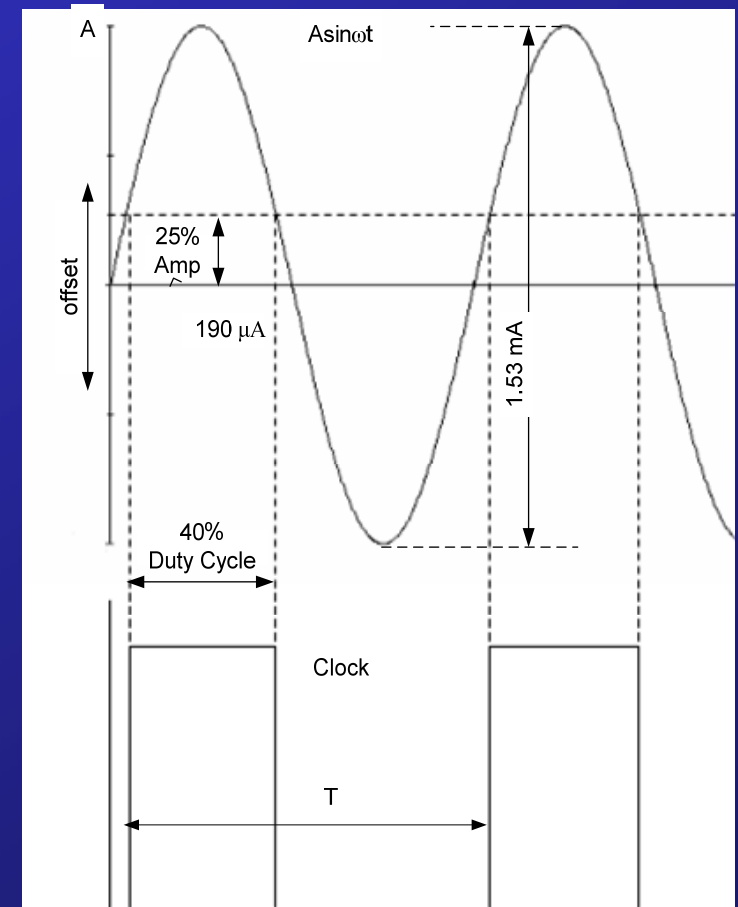
V_{BO1} is the DC output voltage for the first-stage combiners.

I_{out} is the peak-to-peak differential current transferred to the NMOS latch in the comparator

If λ is included, the analytical predictions agree closely (within 5%) with the results obtained from electrical simulations.

Mismatch and offset analysis

- Random offsets due to mismatch in transistor parameters will result in the clock's duty cycle differing from the ideal fifty percent.
- In fact, if the offset current becomes larger than the peak differential output current, the clock becomes stuck at one logic level.
- The standard deviation of the offset current was computed as $15\ \mu\text{A}$. The 6σ value, $90\ \mu\text{A}$ is well below the upper limit of $190\ \mu\text{A}$ which was needed to ensure a reasonable duty cycle for the output clock.



Variance computed at each stage

- For NFET in the “first stage” combiner

$$\sigma_{I_{DS1}}^2 = g_{m1}^2 \cdot \sigma_{V_{TN}}^2 + I_{DS1}^2 \cdot \left(\frac{\sigma_{K_{pn}}^2}{K_{pn}^2} + \frac{\sigma_{W_n}^2}{W_n^2} + \frac{\sigma_{L_n}^2}{L_n^2} \right) = (2.5\mu A)^2$$

- For the resistive PFET of the “first stage” combiner

$$\sigma_{R_{eq}}^2 = R^2 \cdot \left(\frac{\sigma_{V_{TP}}^2}{V_{SAT}^2} + \frac{\sigma_{K_{pp}}^2}{K_{pp}^2} + \frac{\sigma_{W_p}^2}{W_p^2} + \frac{\sigma_{L_p}^2}{L_p^2} \right) = (4.3\Omega)^2$$

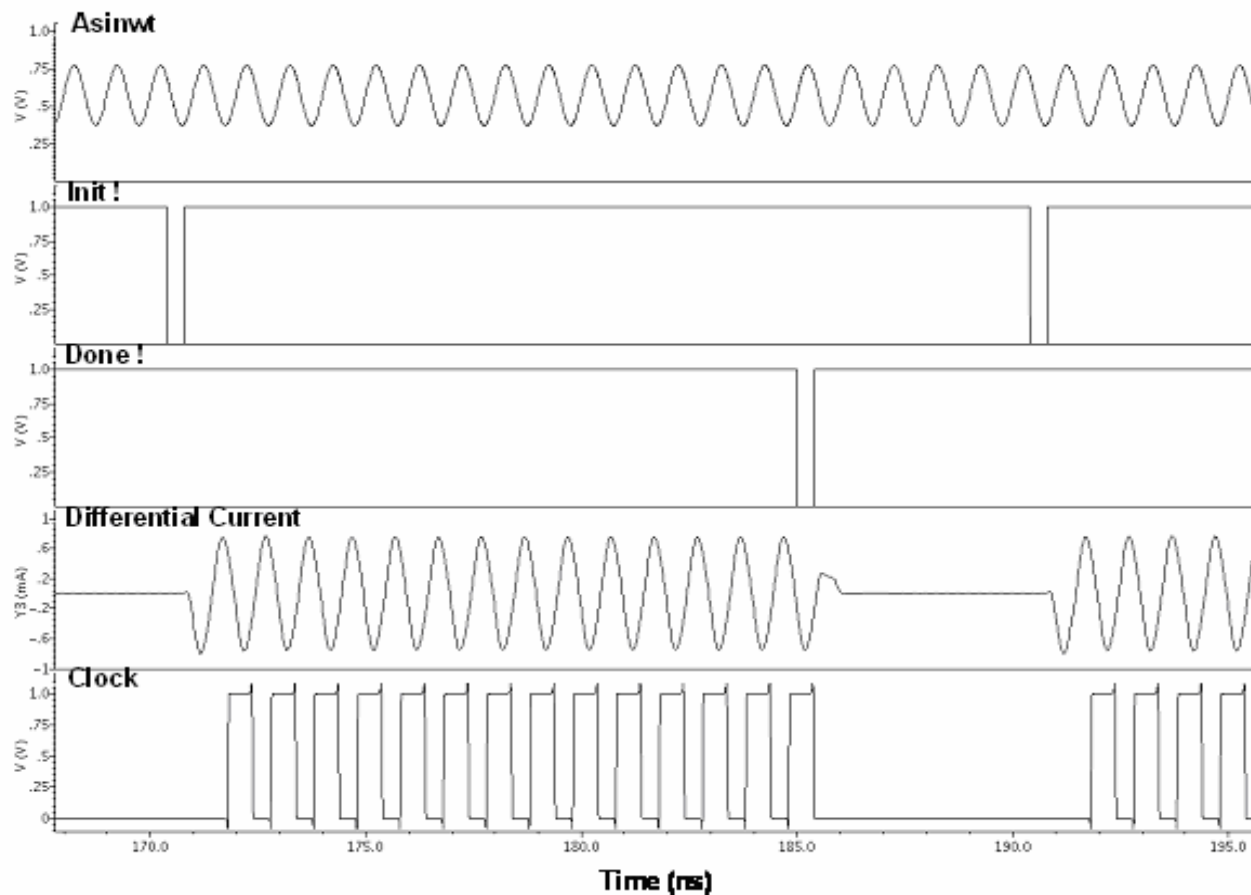
- For the output of the “first stage” combiner

$$\sigma_{V_{O1}}^2 = 2R_{eq}^2 \sigma_{I_{DS1}}^2 + (2I_{DS1})^2 \sigma_{R_{eq}}^2 = (3.8mV)^2$$

- For the differential current output delivered to the NMOS latch

$$\sigma_{I_{out}}^2 = 8 \cdot g_{m2}^2 \cdot (\sigma_{V_{TN}}^2 + \sigma_{V_{O1}}^2) + 8 \cdot I_{DS2}^2 \cdot \left(\frac{\sigma_{K_{pn}}^2}{K_{pn}^2} + \frac{\sigma_{W_n}^2}{W_n^2} + \frac{\sigma_{L_n}^2}{L_n^2} \right) = (15\mu A)^2$$

Simulation results



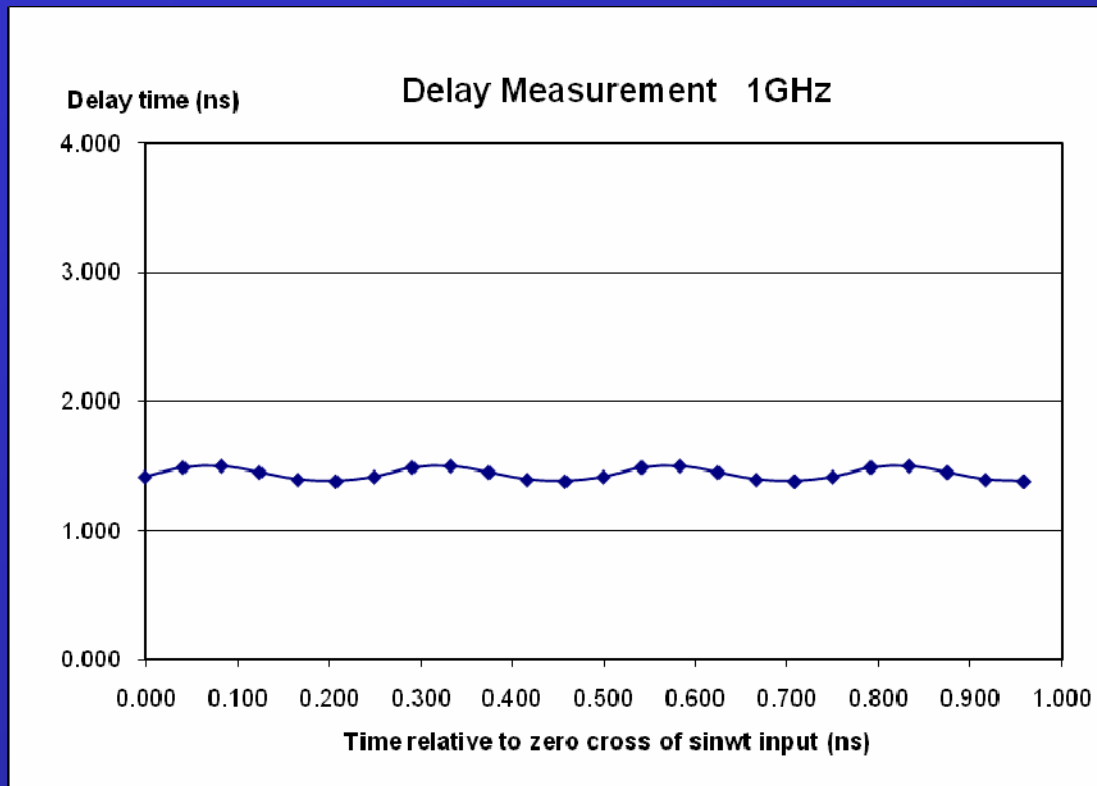
$$V_B = 570\text{mV}$$

$$\text{Amp} = 200\text{mV}$$

$$\text{Freq} = 1\text{GHz}$$

$$\text{Duty cycle} \approx 50\%$$

Simulation result (cont.)



- Delay in restarting clock is less than 1.5 ns.
- The peak-to-peak variation in the time required to restart the clock is 120 *psec*.

Summary

- The restartable clock generator is implemented in 90nm CMOS process.
- Completely transistor design without resistors existing in the circuit.
- Up to 1GHz, clock frequency can be achieved across different process corners.
- Only a single 1V supply is required with 10mW power consumption.
- The duty cycle of the clock output is near 50%.
- The delay in restarting the clock is small, less than 1.5ns.

Conclusion

- The restartable clock can be stopped and then restarted at an arbitrary phase of the source, like a delay based clock.
- Completely eliminates metastability hazards.
- Can be connected to an external crystal oscillator or a local all-silicon, MEMS-based oscillator as input sources.

Further work

- A small systematic offset should be added into the comparator to ensure that the clock always restart from low to high.
- Monte Carlo simulations to confirm the results presented in thesis predicting the likely offset current will be performed in the future.
- Efficiently generate the quadrature input signals from an external crystal oscillator or MEMS-based clock.

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Thank You !

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