

Name: _____

ID Number: _____

Contact information: _____

Indicate the two areas you select:

Subject area 1: _____

Subject area 2: _____

Exam results

Problem	Grade (0-5)	Graded by	Comments

Total score received: _____ out of 25 pts. Recommendation: PASS / FAIL (circled).

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Instructions For MS EE Final Written Examination

This exam is composed of questions in the following subject areas:

1. Communications Systems
 2. Computer Design
 3. Computer Vision and Image Processing (CVIP)
 4. Control Systems
 5. Digital Signal Processing (DSP)
 6. IC Design
 7. Power Systems
- Choose two subject areas from the list above. The choice of problems is restricted to only two areas. Clearly indicate your selected subject areas by writing them in the appropriate place on the cover sheet.
 - Solve 5 problems total. The problems must come from the two selected subject areas. Three from one area and two from the other.
 - Do **NOT** work on back of pages, use extra pages if necessary, write the subject area, problem number and your name at the top of each page. Number the pages for your answers, starting with page '1' for each problem.
 - You may use: your own textbooks, your own calculator, **NO** internet enabled calculators, **NO** interlibrary loan books, **NO** notes or other papers, **NO** cell phones,
 - The exam is **1 hour and 50 minutes**
 - After completed, **put only the cover sheet and the five problems you worked clipped together**, put any unused problems, etc, in the second stack of papers
 - Grades will be based only on written evidence in the submitted work.
 - If you work more than five problems only the first five will be graded.
 - Full credit will be given for professional work only: clear, concise, simple, and as complete as possible.
 - Always show your work. Answers without sufficient supporting work will be awarded zero score.
 - If you provide multiple answers to a problem that has a unique solution, only one of your solutions will be picked for grading: top-most or left-most, not necessarily the correct one.
 - Be sure to read the problems carefully, there will be no credit for solutions to misread problems.
 - Measurement units are considered an important part of the answer. Answers given with incorrect units or unit prefixes may be considered wrong even if the numeric part is right.
 - Every problem will be graded on a scale of 0-5 with 5 being the best. A score of 15 is needed to pass the exam.

ECE Master's Exit Exam**Communications Systems**

#2) A error-correction coding scheme uses 4 transmitted codewords S_1 , S_2 , S_3 , and S_4 as follows

S_1	00000000
S_2	10101010
S_3	11110000
S_4	00001111

(a) Find the number of errors the decoder can detect.

(b) Determine if the code is linear

ECE Master's Exit Exam**Communications Systems**

#3) (a) Find the 2nd-order extended Huffman code for two symbols A and B with the probabilities 0.8 and 0.2.

(b) Calculate the coding efficiency.

ECE Master's Exit Exam**Computer Design**

#1) A sequence of instructions is given. Show how they proceed through a typical 5-stage RISC pipeline (assuming all memory accesses are cache hits). The branch is unconditional.

	Cycle#	1	2	3	4	5	6	7	8	9	10	11	12
R3 := M(R7+3)	LD1												
M(R3+4) := R2	ST2												
R1 := R5 + R3	ADD3												
Branch to top	BR4												
R1 := R2 + R6	ADD5												

b. Identify every instance of forwarding occurring in the above sequence.

c. If the branch was conditional on R1, one more clock cycle would be required to complete the sequence. Explain when and why.

ECE Master's Exit Exam**Computer Design**

#2)) Explain what is meant by the phrase "microprogrammed control unit." Briefly explain the difference between "horizontal" and "vertical" microcode. What is a nano-memory and a nano-program, and when are their use beneficial?

ECE Master's Exit Exam**Computer Design**

#3) A finite-state machine has 2^n possible states. At each clock pulse, it reads in a k -bit symbol, emits an m -bit output symbol (including feedback bits), and switches to a new state. The symbol emitted and the new state depends on the current state and the input symbol.

a) Draw a block diagram indicating how the machine can be implemented using a ROM. Explain your diagram.

b) Determine how big the ROM must be. Explain.

c) A non-pipelined processor has a microcode-based controller implemented as a finite-state machine of the sort indicated above. Explain what the states, the k -bit input symbol, and the m -bit output symbol correspond to in this context. How is the instruction processing accomplished?

d) A given processor has an instruction set containing 16 instructions. The average CPI (clocks per instruction) when the cache hit probability is 100%, is 5. Determine the required size of the ROM. Explain how you arrived at your answer, and state any assumptions you have made.

ECE Master's Exit Exam Computer Vision & Image Processing

#1) a. A video frame is scanned at $1/30$ of a second, using interlaced scanning. If we have 720 lines of interest, and 1280 pixels per line, at what rate must we perform the analog to digital conversion? (ignore synch pulse time)

b. i) Approximately how many electrons are liberated if:

irradiation = 500,000 photon flux/nm²

quantum efficiency of device = 0.05 electron flux/photon flux

area = 100 nm²

time period = 10 milliseconds

the photon flux is bandlimited to visible wavelengths

ii) Is this a tube or solid state device? Explain.

ECE Master's Exit Exam Computer Vision & Image Processing

#2) a) Using the convention that the first number per row is a run of zeros, and horizontal RLC, find the RLC for each bit plane for the following 3 bpp image (numbers are base 10):

$$\begin{bmatrix} 7 & 7 & 7 & 7 \\ 4 & 4 & 4 & 4 \\ 4 & 3 & 4 & 3 \\ 2 & 2 & 0 & 0 \end{bmatrix}$$

b) Explain why a Gray code may improve the compression with bitplane RLC. In the image from part (a), which row will benefit the most from using a gray code? Why?

ECE Master's Exit Exam Computer Vision & Image Processing

#3). An imaging system has a lens with a diameter of 100mm and a focal length of 10mm. The system is setup so that objects at a distance of 2.0 meters are correctly focused. Assume that the imaging device is a CCD with round pixel elements that have a 0.1mm diameter. Describe how an object at a distance of 1.5 meters appears in the image. a) Provide a numeric value to describe the object, b) use words to explain how it will appear.

ECE Master's Exit Exam**Control Systems**

#1) Given the following differential equation:

$$\frac{d^2}{dt^2} y(t) + 2 \frac{d}{dt} y(t) + y(t) = u(t).$$

- a. Assume the initial conditions are zero, i.e. $y(0)=0, \dot{y}(0) = 0$, write down the transfer function $G(s)=Y(s)/U(s)$.
- b. If the input is a unit-step function, what is the output signal $y(t)$ of this system?

ECE Master's Exit Exam

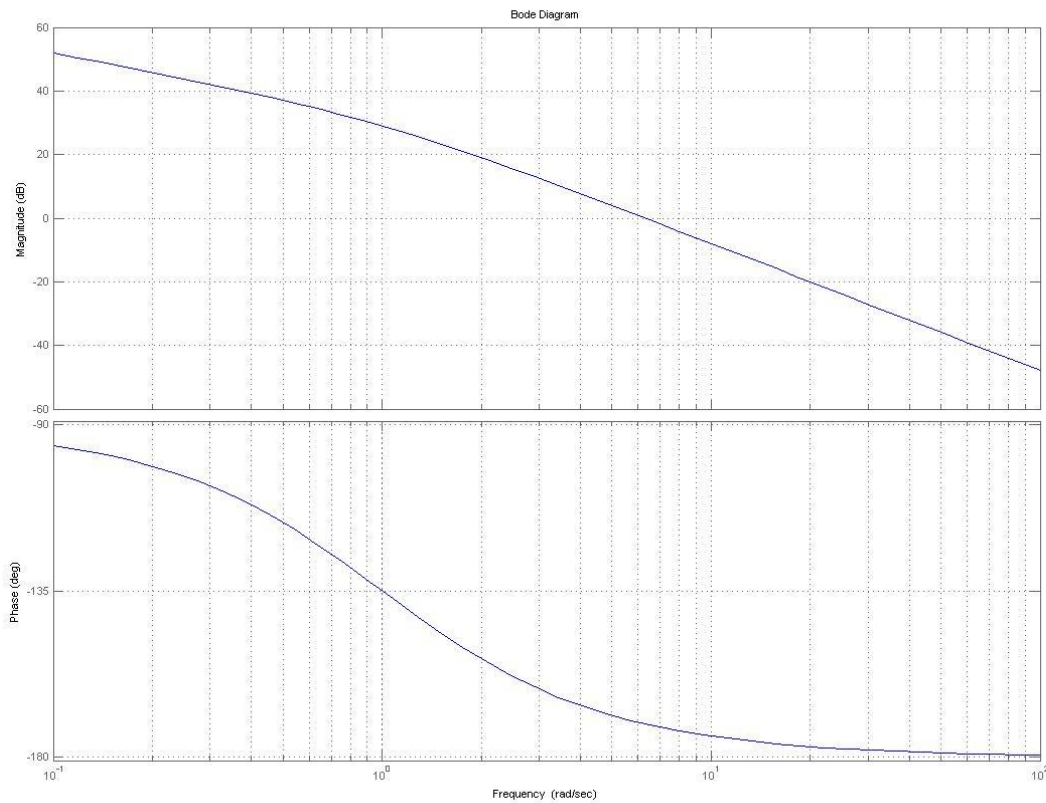
Control Systems

- #2) Given a system with the following transfer function

$$G(s) = \frac{40}{s(s+4)}$$

With the bode plot shown below.

- What are the phase margin and gain margin from the plot?
- Design a lead compensator $G_c(s) = \frac{Ts + 1}{\alpha Ts + 1}$, such that the phase margin is at least 50° .



ECE Master's Exit Exam**Control Systems**

#3) Given the open-loop transfer function for a unity-feedback system as

$$G(s) = \frac{K}{s(s+1)(s+2)}.$$

- a. Draw the root locus plot of $G(s)$.
- b. Determine the stability range for K .

ECE Master's Exit Exam**Digital Signal Processing**

#1) A causal, linear, time-invariant, discrete-time system H with input x_n and output y_n is described by the difference equation:

$$y_n = 0.9 y_{n-1} - 0.81 y_{n-2} + x_n + x_{n-2}$$

- a) Determine the transfer function $H(z)$ for this system.
- b) Sketch the pole-zero diagram for this system.
- c) Sketch the magnitude and the phase of the frequency response $H(e^{j\omega})$, for $0 < \omega < \pi$
- d) Determine the output sequence y_n for the input sequence x_n :

$$x_n = \begin{cases} 1 & \text{if } n = 2 \\ -0.9 & \text{if } n = 3 \\ 0.81 & \text{if } n = 4 \\ 0 & \text{for all other } n \text{'s} \end{cases}$$

ECE Master's Exit Exam**Digital Signal Processing**

#2) Let $\{s(nT), -\infty < n < \infty, n \text{ an integer}\}$ denote equi-spaced samples, taken once each T seconds, of an analog signal $s(t)$. This signal is not necessarily band-limited. Denote the Fourier transform of this signal by $S(f)$, where:

$$S(f) = \int_{-\infty}^{\infty} s(t) e^{-j2\pi ft} dt.$$

a) Prove that if $s(nT) = \delta(nT)$ then:

$$\frac{1}{T} \sum_{k=-\infty}^{\infty} S\left(f - \frac{k}{T}\right) = 1.$$

Carefully state any assumptions that you make, and show all the details in your proof.

b) Prove the converse to part a). That is, prove that if

$$\frac{1}{T} \sum_{k=-\infty}^{\infty} S\left(f - \frac{k}{T}\right) = 1.$$

Then $s(nT) = \delta(nT)$.

c) Give an explicit example (via either an equation or a carefully labeled graph) of a signal $s(t)$ that is not band-limited and has a Fourier transform satisfying:

$$\frac{1}{T} \sum_{k=-\infty}^{\infty} S\left(f - \frac{k}{T}\right) = 1.$$

ECE Master's Exit Exam**Digital Signal Processing**

#3) Give a clear but brief (1 to 3 sentence) answer to each of the following 10 questions.

1. What is the relationship, if any, between the discrete Fourier transform (DFT) and a fast Fourier transform (FFT)?
2. What is the relationship between a discrete-time, linear system that is causal and the unit circle in the complex z -plane associated with the z -transform of its unit-sample response?
3. Describe the region of convergence of the z -transform of the unit-sample response of a discrete-time, linear system that is stable.
4. What does it mean to design a discrete-time filter to correspond to a continuous-time filter when the principle of "impulse-invariance" is used?
5. State the Nyquist sampling theorem.
6. Describe the input-output characteristic of an ideal b -bit uniform quantizer.
7. What is Gibbs' phenomenon?
8. What is the definition of a linear system?
9. What is aliasing?
10. Comment on general characteristics of Butterworth filters.

ECE Master's Exit Exam**IC Design**

- #1) Consider a metal 1 wire which is $5\ \mu\text{m}$ wide and $250\ \mu\text{m}$ long which runs over the substrate. Assume the capacitance per unit area is $0.031\ \text{fF} / \mu\text{m}^2$ and the fringe capacitance per unit length is $0.076\ \text{fF} / \mu\text{m}$. Also, assume the sheet resistance is $0.08\ \text{ohms} / \text{square}$.
- a) What is the lumped capacitance presented by the wire?
 - b) What is the lumped resistance of the wire?

ECE Master's Exit Exam**IC Design**

#2) Realize the following function using a fully complementary CMOS complex gate:

$$F = (A \mid B) \& (C \mid D)$$

where $\&$ is the logical AND operator and \mid is the logical OR operator.

ECE Master's Exit Exam**IC Design**

#3) Determine I_{DS} for the FETs described below. Use the agreed upon process parameters.

$$V_{dd} = 2.5 \text{ Volts}$$

$V_{ds,vsat}$ = saturation voltage due to velocity saturation = 0.65 volts for NFETs and -3 volts for PFETs. (Assumes $L = 0.25 \mu\text{m}$)

Length of all FETS is $0.25 \mu\text{m}$.

Threshold voltage of NFET is +0.5 Volts.

Threshold voltage of PFET is -0.5 Volts.

Transconductance parameter of NFET, K_{PN} , is $230 \mu\text{A}/\text{V}^2$

Transconductance parameter of PFET, K_{PP} , is $50 \mu\text{A}/\text{V}^2$

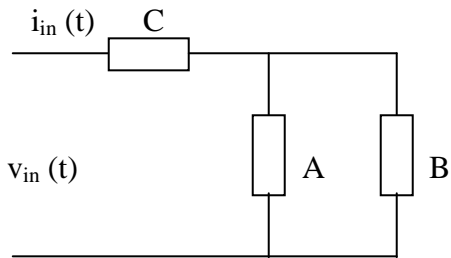
Neglect both channel length and bulk modulation effects i.e. $\gamma = 0$ and $\lambda = 0$. Assume in each case the width of the FET is $5 \mu\text{m}$.

- a) What is I_{ds} for a NFET whose gate voltage is 1.5 Volts, drain voltage is 1.5 volts, and source voltage is 0 volts?
- b) What is I_{SD} for a PFET whose gate voltage is 0 Volts, source voltage is 2.5 volts, and drain voltage is 1.5 volts?

ECE Master's Exit Exam

Power Systems

#1) For the following Y-connected three phase circuit (60 Hz)

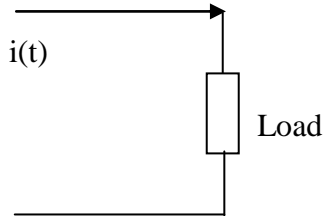


- * Load A: It consumes 90KW and -90KVAR
- * Load B: It consumes 90KVAR
- * voltage across load A and load B = 346 V_{line-to-line}
- * $C = (0.1 + j0.1) \Omega/\text{phase}$

- a) Find the current through the load A, $i_A(t)$.
- b) Find the current through the load B, $i_B(t)$
- c) Find the input current to the circuit, $i_{in}(t)$
- d) Find the input voltage, $v_{in}(t)$.
- e) Find the input power factor
- f) Find the apparent power consumed by the circuit S_{in} .

ECE Master's Exit Exam**Power Systems**

#2) A monophasic load is consuming 25 KVA at a lagging power factor of 0.8 when 200 V is applied ($f = 60\text{Hz}$).



- a) Find the current $i(t)$.
- b) Find the shunt (parallel) capacitor bank (in KVAR) to increase its power factor to 0.95 lagging.
- c) Assuming that the shunt capacitor bank is available in multiple of 1 KVAR, what is the size of shunt capacitor (in KVAR) to be installed? Also, find the new power factor after installing this capacitor bank.

ECE Master's Exit Exam**Power Systems**

#3) A single-phase, 440V/220V, 100 KVA transformer is supplying 60 Kvar to a load at a lagging power factor of 0.8. The voltage across the load is 200 V. Using a simplified equivalent circuit with $r_1 = 0.02 \Omega$, $r_2 = 0.005 \Omega$, $x_1 = 0.03 \Omega$, and $x_2 = 0.005 \Omega$,

- a) draw an equivalent circuit with all transformer parameters and find the input current to the transformer.
- b) find input voltage to the transformer.
- c) find the input apparent power and input power factor.
- d) find the efficiency and regulation of the transformer.