Instructor: Dr. George L. Engel

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Lecture: T, R: 12:30 pm – 1:45 pm (EB 3009)

Office Hours: See Dr. Engel’s website.

Course Description:

Fundamental circuit techniques and design issues for mixed-signal integrated circuits. Topics include: switched-capacitor techniques and circuits, analog-to-digital and digital-to-analog conversion including oversampled coders, along with both system-level and circuit level modeling using VerilogA.

Prerequisites:

ECE326 or equivalent, ECE483 or equivalent, or permission of instructor
Objectives:

1. To provide graduate students with the ability to design and analyze mixed-signal integrated circuits.

2. To learn how to analyze and design switched-capacitor circuits.

3. To learn how to model analog and mixed-signal components using Verilog and VerilogA.

4. To learn how to design digital-to-analog and analog-to-digital converter circuits.

Computer Tools:

Cadence Virtuoso Schematic Editor, Cadence VerilogAMS

Course Text:


References:


Grading Policy:

Exam #1 20%
Exam #2 20%
Final Exam 20%
Midterm Project 20%
Final Project 20%
Lectures

T Aug 21  Chapter 13: Discrete Time Signals
           13.1 Overview of Some Signal Spectra
           13.2 Laplace Transform

R Aug 23  13.3 Z-Transform
           13.4 Downsampling and Upsampling

T Aug 29  13.5 Discrete-Time Filters
           13.6 Sample and Hold Response

R Aug 31  Chapter 14: Switched-Capacitor Circuits
           14.1 Basic Building Blocks

T Sep 05  14.2 Basic Operation and Analysis

R Sep 07  14.2 Basic Operation and Analysis

T Sep 12  14.4 First Order Filters

R Sep 14  14.5 Biquad Filters

T Sep 19  14.5 Biquad Filters
           14.6 Charge Injection

R Sep 21  14.7 Switched-Capacitor Gain Circuits
           14.8 Correlated Double Sampling

T Sep 26  Review of Verilog
           Cadence EDA Tools

R Sep 28  **** EXAM #1 ****

T Oct 03  Introduction to VerilogA

R Oct 05  VerilogA (Conservative system descriptions)

T Oct 10  VerilogA (Conservative system descriptions)
           VerilogA (Signal flow graph descriptions)

R Oct 12  VerilogA (Event processing)
T Oct 17  VerilogA (Signal generation)
R Oct 19  VerilogA (Data recording)
T Oct 24  Verilog AMS tutorial
R Oct 26  Chapter 15: Data Converter Fundamentals
          15.1  Ideal D/A Converter
          15.2  Ideal A/D Converter
T Oct 31  *** EXAM #2 ***
R Nov 02  15.3  Quantization Noise
          15.4  Signed Codes
          15.5  Performance Limitations
T Nov 07  Chapter 16: Nyquist Rate D/A Converters
          16.1  Decoder-Based Converters
          16.2  Binary-Scaled Converters
R Nov 09  16.3  Thermometer-Code Converters
T Nov 14  16.4  Hybrid Converters
R Nov 16  Chapter 17: Nyquist Rate A/D Converters
T Nov 21  ********** THANKSGIVING (NO CLASSES) **********
R Nov 23  ********** THANKSGIVING (NO CLASSES) **********
T Nov 28  17.1  Integrating Converter
R Nov 30  17.2  Successive Approximation Converters
T Dec 05  17.2  Successive Approximation Converters
R Dec 07  17.5  Flash Converters
Class Attendance Policy:

Based on University Class Attendance Policy 119: It is the responsibility of students to ascertain the policies of instructors with regard to absence from class, and to make arrangements satisfactory to instructors with regard to missed course work. Failure to attend the first session of a course may result in the student’s place in class being assigned to another student.

Class Policies:

If you have a documented disability that requires academic accommodations, please go to Disability Support Services for coordination of your academic accommodations. DSS is located in the Student Success Center, Room 1270; you may contact them to make an appointment by calling (618) 650-3726 or sending an email to disabilitysupport@siue.edu. Please visit the DSS website located online at www.siue.edu/dss for more information.

Students are expected to be familiar with and follow the Student Academic Code. It is included in the SIUE Policies and Procedures under Section 3C2.2.