ECE585-001  
Mixed-Signal Design and Modeling

Course Syllabus  
Fall 2014

Instructor: Dr. George L. Engel  
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http://www.siue.edu/~gengel  
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Lecture: M, W: 10:00 am – 11:15 am (EB 3008)

Office Hours: See Dr. Engel’s website.

Course Description:

Fundamental circuit techniques and design issues for mixed-signal integrated circuits. Topics include: switched-capacitor techniques and circuits, analog-to-digital and digital-to-analog conversion including oversampled coders, along with both system-level and circuit level modeling using VerilogA.

Prerequisites:

ECE476 or equivalent, ECE483 or equivalent, or permission of instructor
Objectives:

1. To provide graduate students with the ability to design and analyze mixed-signal integrated circuits.
2. To learn how to analyze and design switched-capacitor circuits.
3. To learn how to model analog and mixed-signal components using Verilog and VerilogA.
4. To learn how to design digital-to-analog and analog-to-digital converter circuits.

Computer Tools:

Cadence Virtuoso Schematic Editor, Cadence VerilogAMS

Course Text:


References:

- P. Allen and D. Holberg, “CMOS Analog Circuit design: Third edition,” Oxford Press, 2012. (This is the same textbook used in ECE584.) If you have the Second Edition that is fine!!!!

Grading Policy:

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**Lectures**

M Aug 18  
**Chapter 13: Discrete Time Signals**  
13.1 Overview of Some Signal Spectra  
13.2 Laplace Transform  
13.3 Z-Transform

W Aug 20  
13.4 Downsampling and Upsampling  
13.5 Discrete-Time Filters

M Aug 25  
13.6 Sample and Hold Response

W Aug 27  
**Chapter 14: Switched-Capacitor Circuits**  
14.1 Basic Building Blocks

M Sep 01  
*** LABOR DAY – -> NO CLASSES ***

W Sep 03  
14.2 Basic Operation and Analysis

M Sep 08  
14.2 Basic Operation and Analysis

W Sep 10  
14.7 Switched-Capacitor Gain Circuits  
14.8 Correlated Double Sampling

M Sep 15  
14.4 First Order Filters

W Sep 17  
14.5 Biquad Filters

M Sep 22  
14.3 Noise in SC Circuits  
14.6 Charge Injection

W Sep 24  
Introduction to VerilogA  
ASSIGN PROJECT

M Sep 29  
Exam #1 (Chapter 13 and Chapter 14)

W Oct 01  
VerilogA (Conservative system descriptions)

M Oct 06  
VerilogA (Signal flow graph descriptions)

W Oct 08  
VerilogA (Event processing)

M Oct 13  
VerilogA (Signal generation)
Chapter 15: Data Converter Fundamentals

15.1 Ideal D/A Converter
15.2 Ideal A/D Converter

Chapter 16: Nyquist Rate D/A Converters

16.1 Decoder-based Converters
16.2 Binary-Scaled Converters

M Nov 03
16.3 Thermometer-Code Converters

W Nov 05
16.4 Hybrid Converters

M Nov 10
Chapter 17: Nyquist Rate A/D Converters
17.1 Integrating Converters

W Nov 12
17.2 Successive Approximation Converters

M Nov 17
17.2 Successive Approximation Converters

W Nov 19
17.5 Flash Converters

PROJECT DUE

M Nov 24
*** THANKSGIVING BREAK ***

W Nov 26
*** THANKSGIVING BREAK ***

M Dec 01
Chapter 18: Oversampling Converters
18.1: Oversampling without Noise Shaping
18.2: Oversampling with Noise Shaping
18.3: System Architectures

W Dec 03
Exam #3 (Chapter 16 and Chapter 17)
Please notify me no later than the end of the first week of class concerning any academic accommodations that you will need. You must have a documented disability and an ID CARD from Disability Support Services.

If you need accommodations not indicated on the Disability Support Services ID CARD, such as special equipment for clinical experiments or for outside classroom settings, please contact me or the Disability Support Services office as soon as possible so arrangements can be made for the additional equipment or accommodations.