II. Bias circuit

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Introduction

Active devices (transistors) have to be properly biased to process the signal

In an analog signal processing circuit there are two fundamental parts:

Processing part
- Bias circuit
  - The processing part is devoted to elaborate the signal
    - Dynamic requirement
  - The bias circuit is devoted to supply currents and/or voltages to the processing one in order to allow it to properly operate
    - Static requirement (Low-frequency, immunity to $V_{DD}$ noise, temperature, and technology spread)

CMOS current mirrors

Definitions

A current mirror reads a current entering in a read-node and mirror this current (with a suitable gain factor) to an output node (nodes)

\[ I_{out} = k \cdot I_{Ref} \]

$k$ current gain

Current mirror non-idealities
- Current gain error
- Output impedance ($r_{out}$) => reduces the output current $I_{out}$
  \[ I_{out} = k \cdot I_{Ref} \cdot \frac{R_{L}}{R_{L} + r_{out}} \]
- Saturation voltage ($V_{CM}$)
  => for $V_{DD} < V_{CM}$ the current mirror doesn't operate correctly
  => reduces the output voltage dynamic range

Basic trade-off: dynamic range $\leftrightarrow$ precision

Frequency behaviour

Applications

Bias

- Circuit no. 1
- Circuit no. 2

Signal path

- Differential-to-Single Ended transformation
- Frequency behaviour
### Simple Current Mirror

#### Current gain

- **NMOS**
  - M1 operates in saturation
  \[ I_{\text{Ref}} = I_1 = \frac{k}{2} \left( \frac{W}{L_1} \right) (V_{GS1} - V_{TH})^2 \left( 1 + \lambda V_{DS1} \right) \]
  \[ V_{DS1} = V_{GS1} = V_{GS2} \]

- **PMOS**
  - If M2 operates in saturation
  \[ I_{out} = I_2 = \frac{k}{2} \left( \frac{W}{L_2} \right) (V_{GS2} - V_{TH})^2 \left( 1 + \lambda V_{DS2} \right) \]
  \[ I_{out} = I_{\text{Ref}} \left( \frac{W}{W_1} \right) \left( 1 + \lambda V_{DS1} \right) \]

#### Output impedance \((r_{out})\)

- Insert \( V_{\text{test}} \)
- Evaluate \( I_{\text{test}} \)
- Calculate \( r_{out} = \frac{V_{\text{test}}}{I_{\text{test}}} \)

- Use of long device (large \( L \)) to increase \( r_{out} \)
- Use of large \( (V_{GS} - V_{TH}) \) for good matching (small importance of \( V_{TH} \) mismatch)

#### Frequency behaviour

- Small signal equivalent circuit

\[
\begin{align*}
\frac{i_{\text{out}}}{i_{\text{in}}} & = \frac{g_{m2}/g_{m1}}{1+s(C_{gs1}+C_{gs2})/g_{m1}} \\
k & = g_{m0}/g_{m1} = C_{gs2}/C_{gs1} \\
\frac{i_{\text{out}}}{i_{\text{in}}} & = \frac{k}{1+s(1+k)C_{gs1}/g_{m1}} \\
f_T & = g_{m1}/C_{gs1} \\
pole & = (g_{m1}/C_{gs1})/(1+k) = f_T/(1+k)
\end{align*}
\]

#### Output swing

- The output swing in the Simple current mirror is limited to
\[ V_{out,\text{min}} = V_{DSSat.2} \]
Simple Current Mirror

Factors affecting the mirror accuracy

- Channel length modulation ($\lambda$)
- Threshold offset
- Parasitic resistances
- Imperfect geometrical matching and current mobility variation

\[
\frac{I_{\text{out}}}{I_{\text{ref}}} = \frac{W_1}{W_2} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}
\]

It can be improved by increasing the output resistance.
- use of large $L$ (typically current mirrors are not realized with the minimum technological $L$. This can result in a large capacitance at the output node)

• Threshold offset
Threshold of MOS transistors in close proximity can differ by 4 mV. For transistors hundred of $\mu$m apart, the threshold difference $\Delta V_{TH}$ can be 40 mV

\[
I'_{\text{out}} = I_{\text{out}} \left[ 1 + 2 \frac{\Delta V_{TH}}{V_{GS} - V_{TH}} \right]
\]

Use large ($V_{GS} - V_{TH}$) to improve matching

• Parasitic resistances
A parasitic resistance in series with the source determines a voltage drop

The metal resistance is of the order of 20-50 $\mu\Omega$/sq, with 10 squares it results 0.2-0.5 $\Omega$. If the current is 10 mA it results an equivalent offset of 2-5 mV.

• Imperfect geometrical matching and current mobility variation

\[
\frac{\delta I}{I} = \frac{\delta k'}{k'} + \frac{\delta C_{ox}}{C_{ox}} + \frac{\delta W}{W} + \frac{\delta L}{L}
\]

$\delta k'$ and $\delta C_{ox}$ are minimized with closed and centroid common structures

$\frac{\delta W}{W} + \frac{\delta L}{L}$ depends on the lithographic process

For large $W$ a good strategy is to have $W$ not much larger than $L$ and to put equal transistors in parallel

\[
\frac{\delta I}{I} = \ldots + \frac{1}{n} \left( \frac{\delta W'}{W'} + \frac{\delta L'}{L'} \right)
\]
Simple Current Mirror

Factors affecting the mirror accuracy

- Imperfect geometrical matching and current mobility variation

Example:

Circuit scheme

\[ I_{\text{ref}} \]

\[ M_1 \quad M_2 \]

\[ I_{\text{out}} \]

Layout solution

\[ I_{\text{ref}} \]

\[ M_1 \quad M_2 \quad M_1 \]

\[ M_1 \quad M_2 \quad M_1 \]

\[ \text{GND} \]

\[ I_{\text{out}} \]

Simple Current Mirror

Design example

With the following technological parameter design a simple current mirror in order that it drives to the output node 1mA and it requires 400mV

\[ L_{\text{min}} = 0.5\mu m; \quad \mu_n \cdot C_{\text{ox}} = 60\mu A/V^2; \quad \mu_p \cdot C_{\text{ox}} = 30\mu A/V^2; \]

\[ \lambda_n = 0.1 V^{-1}; \quad \lambda_p = 0.2 V^{-1}; \quad \gamma = 0; \quad V_{\text{THN}} = -V_{\text{THN}} = 0.7V \]

Which is the expected output impedance?

Wilson current mirror

Increases the output resistance

\[ V_{\text{GS1}} = V_{\text{GS2}} \]

\[ I_1 = I_2 \]

\[ I_{\text{out}} = \frac{W}{L_1} \cdot \frac{1 + \lambda \cdot V_{\text{DS2}}}{1 + \lambda \cdot V_{\text{DS1}}} \]

\[ I_{\text{ref}} = \frac{W}{L_2} \]

\[ V_{\text{DSat,3}} \]

\[ V_{\text{GS2}} \]

Output swing

- The output swing in the Wilson current mirror is limited to

\[ V_{\text{out},\text{min}} = V_{\text{GS2}} + V_{\text{DSat,3}} > V_{\text{Th}} + 2 \cdot V_{\text{DSat}} \]

- There is a systematic error since \( V_{\text{DS1}} = V_{\text{DS2}} + V_{\text{GS3}} \)
Wilson current mirror

Output impedance

Small signal equivalent circuit

Improved Wilson current mirror

Current gain

Small signal equivalent circuit

Same equations with:

\[ V_{g3} = - \frac{g_{m1} V_{g2}}{g_m} \]

\[ r_f = \frac{R_L}{1 + g_m} \]

\[ r_{out} = \frac{g_m}{g_m} \frac{g_{m1}}{g_{m2}} \frac{g_{m3}}{g_{m4}} \]

• The output swing in the Wilson and improved Wilson schemes is limited to

\[ V_{out,min} = V_{GS2} + V_{DSat,3} > V_{TH} + 2V_{DSat} \]

Improved Wilson current mirror

Current gain

Cascode Current Mirror

Current gain

same equations with:

\[ V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4} \]

\[ V_{DS1} = V_{DS2} \quad \text{if} \quad V_{GS3} = V_{GS4} \]

\[ I_{out} = \frac{1}{r_f} \left( \frac{W}{L} \right) \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \]

• Higher voltage for the sensing branch (M1-M4)

• No systematic error in the current gain

• The current gain is accurate

• For large current (i.e. with \((W/L)_{M2}\) large) it allows to decrease the output capacitance using \((W/L)_{M3}\) small.
**Cascode Current Mirror**

**Output swing**

\[ I_{\text{out}} = I_{\text{ref}} \]

\[ V_{\text{GS3}} = V_{\text{GS4}} \]

- The output swing is limited to:
  \[ V_{\text{out,min}} = V_{\text{GS1}} + V_{\text{GS4}} - V_{\text{GS3}} + V_{\text{DSsat,3}} \]
  \[ V_{\text{out,min}} = V_{\text{GS2}} + V_{\text{DSsat,3}} > V_{\text{TH}} + 2V_{\text{DSsat}} \]

**Multiple-Cascode Current Mirror**

- More cascode stage can be stacked to increase output impedance.
- For n stages
  - Output impedance
    \[ r_{\text{out}} \approx (r_{\text{ds}} \cdot g_{m})^{n-1} \cdot r_{\text{ds}} \]
  - BUT:
    - The saturation voltage increases to:
      \[ V_{\text{out,min}} = (n-1)V_{\text{TH}} + nV_{\text{DSsat}} \]
    - The current gain is accurate \( V_{\text{DS1}} = V_{\text{DS2}} \)

**Modified Cascode Current Mirror**

- Increase the output swing with the cascode output impedance
  - M4 shifts the voltage \( V_{\text{DS1}} \) of the amount enough to bias the gate of M3 without operating M2 out of saturation.

**Cascode Current Mirror**

**Output impedance**

- The output resistance is increased without feedback.

Small signal equivalent circuit

\[ i_{x} = g_{m3} V_{\text{GS3}} + (V_{x} - V_{S3})/r_{\text{ds3}} \]
\[ i_{x} = V_{S3}/r_{\text{ds2}} \]
Modified Cascode Current Mirror
Possible implementation

- M4 is matched with M3 to get $V_{DS1} = V_{DS2}$ (at the cost of the output swing limitation).
- The output swing is improved by the use of a level shift $V_{Sat}$:
  \[
  \Delta V = V_{GS4} - V_{GS5} = \sqrt{\frac{2}{K}I_{LS4}} - \sqrt{\frac{2}{K}I_{LS5}} I_5 = \left(\sqrt{\frac{L}{W_4}} - \frac{L}{W_5} \frac{L}{L_4} \frac{L}{L_1}\right)
  \]
- $\Delta V$ is fixed by the geometrical dimensions of $M_1, M_6, M_4, M_5$ and by $V_{ov4}$.
- The output swing is:
  \[
  V_{out,min} = V_{DS2} + V_{DS3} = 2 \cdot V_{DSat}
  \]
- Systematic error in the current gain ($V_{DS1} \neq V_{DS2}$)

High-compliance current mirrors
(I)

All transistors operate in saturation

\[
I = I_1 = I_2 = I_3 = I_4 \quad \text{(current scaling is possible)}
\]

\[
\beta_1 = \beta_2 = \beta_3 = \beta_4 \quad \Rightarrow \quad V_{ov1} = V_{ov2} = V_{ov3} = V_{ov} \quad , \quad I_4 = \beta_4 \cdot (V_{ov})^2, \quad I_2 = \beta_2 \cdot (V_{ov})^2, \quad I_3 = \beta_3 \cdot (V_{ov})^2
\]

\[
V_{ov} = \Delta V \quad \Rightarrow \quad V_{ov} = \sqrt{\frac{1}{\beta_4}} \quad , \quad V_{ov4} = 2 \cdot V_{ov}
\]

\[
\beta = 4 \cdot \beta_4 \quad \Rightarrow \quad \sqrt{\frac{1}{\beta_4}} = 2 \cdot \sqrt{1 \beta}
\]

\[
\left(\frac{W}{L}\right)_{M_1} = \left(\frac{W}{L}\right)_{M_2} = \left(\frac{W}{L}\right)_{M_3} = 4 \cdot \left(\frac{W}{L}\right)_{M_4}
\]

- Current gain
  - Systematic error due to $V_{DS1} \neq V_{DS2}$
  - Systematic error due to body effect on $M_3$

- Output swing
  \[
  V_{out,min} = 2 \cdot V_{DSat}
  \]

- Output impedance
  \[
  r_{out} = R_{ds4} \cdot g_{m2} \cdot R_{ds2}
  \]

- The scheme can be stacked for multiple cascode
High-compliance current mirrors (II)

- It is also possible to enter at the drain of M1

\[ I_{\text{out}} = I_{\text{Bias2}} + I_{\text{Ref}} \]

Regulated-cascode current mirror

- Output impedance
  \[ r_{\text{out}} = (g_{m3} \cdot r_{o3}) \cdot (g_{mA} \cdot r_{oA}) \]

- Possible implementation

Output swing for different current mirrors

Comparison

- The slope (1, 2, or 3) indicates the output impedance \( r_{\text{out}} \)

Low-voltage current mirror

For low-voltage application the dc voltage drops must be minimized in order to:
- give the maximum room for the signal swing
- not to limit the supply minimization with bias circuits

This valid both for the input stage (reading the current) and for the output stage (sinking the current)

For the simple current mirror

\[ V_{\text{out, min}} = V_{\text{DSsat}} + V_{\text{ov}} + V(I_{\text{Ref}}) \]

- The output stage (M2) requires
  \[ V_{\text{out, min}} = V_{\text{DSsat}} \]

- This is minimum, thus stacked-device topologies are avoided
- Output impedance is increased with large L
- The input stage (M1) requires
  \[ V_{\text{out, min}} = V_{\text{TH}} + V_{\text{ov}} + V(I_{\text{Ref}}) \]

This value can be reduced
Low-voltage current mirror

The input stage voltage requirement can be reduced by using the low-voltage current mirror

\[ I_{\text{out}} = I_{M3} + I_{\text{ref}} \]

- The drain of M1 is fixed to be \( V_{DD} - V_{GS3} \)
- This is fixed to be equal to \( V_{DSSat} \)
- The current mirror requires one \( V_{DSSat} \) to operate.

Low-voltage current mirror

Application

- Operational amplifier

CMOS current mirrors

Comparison Table

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Current gain</th>
<th>Output swing</th>
<th>( r_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>( 1 + \lambda \cdot V_{DS2} )</td>
<td>( V_{DSSat} )</td>
<td>( r_{ds} )</td>
</tr>
<tr>
<td>Wilson</td>
<td>( 1 + \lambda \cdot V_{DS2} )</td>
<td>( V_{TH} + 2 \cdot V_{DSSat} )</td>
<td>( g_m \cdot r_{ds}^2 )</td>
</tr>
<tr>
<td>Improved Wilson</td>
<td>1</td>
<td>( V_{TH} + 2 \cdot V_{DSSat} )</td>
<td>( g_m \cdot r_{ds}^2 )</td>
</tr>
<tr>
<td>Cascode</td>
<td>1</td>
<td>( V_{TH} + 2 \cdot V_{DSSat} )</td>
<td>( g_m \cdot r_{ds}^2 )</td>
</tr>
<tr>
<td>Triple Cascode I</td>
<td>1</td>
<td>( 2 \cdot V_{TH} + 3 \cdot V_{DSSat} )</td>
<td>( g_m^2 \cdot r_{ds}^3 )</td>
</tr>
<tr>
<td>Triple Cascode II</td>
<td>1</td>
<td>( 2 \cdot V_{TH} + 3 \cdot V_{DSSat} )</td>
<td>( g_m^2 \cdot r_{ds}^3 )</td>
</tr>
<tr>
<td>High-compliance I</td>
<td>( 1 + \lambda \cdot V_{DS2} )</td>
<td>( 2 \cdot V_{DSSat} )</td>
<td>( g_m \cdot r_{ds}^2 )</td>
</tr>
<tr>
<td>High-compliance II</td>
<td>1</td>
<td>( 2 \cdot V_{DSSat} )</td>
<td>( g_m \cdot r_{ds}^2 )</td>
</tr>
<tr>
<td>Regulated-cascode</td>
<td>( 1 + \lambda \cdot V_{DS2} )</td>
<td>( V_{TH} + 2 \cdot V_{DSSat} )</td>
<td>( g_m^2 \cdot r_{ds}^3 )</td>
</tr>
</tbody>
</table>

Exercise

1. DC analysis of Simple CM
2. AC analysis of Simple CM
   - Transfer function
   - Output impedance (for different \( L \), with same \( W/L \))
3. Check the systematic error in Wilson CM (different \( V_{DS} \))
   - Improve by using large \( L \) (with same \( W/L \))
   - Check the signal swing (DC sim.)
4. Cascode CM
   - Evaluate the output impedance (AC)
   - Evaluate the signal swing (DC)
5. Multiple Cascode CM
   - Evaluate the output impedance (AC)
   - Evaluate the signal swing (DC)
6. Large dynamic Cascode CM
   - Evaluate the output impedance (AC)
   - Evaluate the signal swing (DC)
7. Low-voltage CM operation
Current references

Introduction

- It allows to generate on-chip (no external components) a current reference
- Necessary for biasing analog subcircuits.
- The generated current reference is mirrored where required, with a suitable scaling factor.

Typically the reference current in the reference current generator is much smaller than the current level in the main circuit (i.e. the scale factor is larger than one) in order to reduce power consumption in the current reference generator.

Possible current reference generators
- Simple current reference (supply dependent)
- Current references based on a built-in voltage (supply independent)
- Current references based on a reference voltage (supply independent)

Features for a reference current
- Supply dependence
- Temperature dependence
- Technology dependence

Simple current reference (supply dependent)

- Voltage Vb is used to bias a current mirror
- For the NMOS case:
  \[ I_{REF} = \frac{V_{DD} - V_{DS1}}{R_L} \]
  \[ |V_{ov1}| = \sqrt{\frac{2}{R} \cdot \frac{R_{L}}{W/L}} \cdot I_{REF} \]
  \[ I_{REF} = \frac{V_{DD} - |V_{TH1}| - |V_{ov1}|}{R_L} \]
  \[ V_{DD} - |V_{TH1}| - \sqrt{\frac{2}{R} \cdot \frac{R_{L}}{W/L}} \cdot I_{REF} \]

Supply dependence
- \( I_{REF} \) depends on supply voltage \( V_{DD} \)

Temperature dependence
- \( R_1 \): positive temperature coefficient (TC)
- \( |V_{TH1}| \): negative temperature coefficient
- \( |V_{ov1}| \): positive temperature coefficient

Typically the sum \( (V_{GS1} = |V_{TH1}| + |V_{ov1}|) \) has a negative TC

Current references based on a built-in voltage

Basic principle

- The current is obtained by "extracting" a built-in voltage \( (V_{bi}) \) to be applied to a given resistor

\[ I_{REF} = \frac{V_{bi}}{R_1} \]

- The dependence of the built-in voltage on temperature and other parameters will affect the generated reference current.
- The generated current is substantially independent from supply voltage.
- Micropower current reference based on this principle are also available.
Self-biased current reference
\((V_{TH} + V_{OV})\)-based

- Built-in voltage:
  \[ V_{bi} = V_{GS1} = V_{TH} + V_{OV} \]

\[ W_3/L_3 = W_4/L_4 \] (i.e. current mirror)
\[ I_1 = I_2 = k' \frac{W_1}{L_1} (V_{GS1} - V_{TH})^2 \]
\[ R \cdot I_2 = R_{1} \cdot I_{GS1} = \sqrt{\frac{2 I_2}{k'} \frac{L}{W_1} + V_{TH}} \]

- Typically, \( V_{OV} \) is designed to be much smaller than \( V_{TH} \) in order to have:
  \[ I_1 \approx \frac{V_{TH}}{R_{1}} \]

- Low currents can be generated using large resistor \((V_{TH} + V_{OV})\) in the range of 1 V

Temperature dependence
- \( R_1 \): positive TC
- \( V_{TH} \): negative TC
- \( V_{OV} \): positive TC
  \(|(V_{TH}) + |V_{OV}|\): negative TC

- Complementary structure is always possible

Possible start-up circuit solution

- At start-up, MS is turned on, thus forcing M4 in the saturation region. Then it is definitively turned off.

Self-biased low-current reference generator
\(\Delta V_{OV}\)-based

Built-in voltage: \( \Delta V_{OV} = V_{OV1} - V_{OV2} \)

\[ \frac{L_3}{W_3} = \frac{L_4}{W_4} \rightleftharpoons \frac{L_1}{W_1} = m \cdot \frac{L_2}{W_2}; \quad m > 1 \]

- M3-M4 is an ideal current mirror \( \Rightarrow I_3 = I_4 = I_1 = I_2 = I_{REF} \)
- \( V_{TH1} = V_{TH2} \)

\[ \sqrt{\frac{2 I_{REF}}{k'} \frac{L}{W_1}} = \sqrt{\frac{2 I_{REF}}{k'} \frac{L}{W_2} + R \cdot I_{REF}} \]

\[ \sqrt{I_{REF}} = \frac{1}{R_{1}} \sqrt{\frac{2}{k'} \left[ \frac{1}{W_1 L_1} \left( 1 - \frac{1}{\sqrt{m}} \right) \right]} \]

- \( \Delta V_{OV} \) generally ranges from tens to hundreds mV
- Small currents can be obtained with not very large R
- For \( m=10, \quad V_{R} = 60 \text{ mV} \) if it is required \( I = 1 \mu A \)
  \( \Rightarrow R = 60k\Omega \)

Temperature dependence:
- \( R_1 \): positive TC
- \( \Delta V_{OV} \): positive TC.

- Also for this circuit a start-up circuit is necessary

Complementary structure also available:
- M3, M4 n-channel transistors (source connected to \( V_{SS} \))
- M1, M2 p-channel transistors (source of M1 connected to \( V_{DD} \))
- R1 connected between source of M2 and \( V_{DD} \)
- in n-well processes, M1 and M2 in the same well.
### VBE-based current reference

![Circuit Diagram]

- Q1 is a substrate BJT
- M1 to M4 operate in saturation region (improved Wilson current mirror)
- \( I_1 = I_2 = I_{\text{REF}} = I \)
- \( V_{GS1} = V_{GS2} \Rightarrow V_{S1} = V_{S2} \Rightarrow V_{\text{REF}} = V_{EB} \)
- \( I = \frac{V_{EB}}{R_1} \)

- To generate low currents, a large \( R_1 \) is needed (\( V_{EB} \) in the range of 0.6 V)
- Start-up circuitry is needed
- Use the complementary structure for p-well processes

**Temperature dependence:**
- \( R_1 \): positive TC
- \( V_{EB} \): negative TC

### VT-based current reference

![Circuit Diagram]

**Built-in voltage:**
\[
\Delta V_{EB} = V_{EB1} - V_{EB2} = V_T \ln(n)
\]

- \( Q_1, Q_2 \): substrate BJT with different emitter areas:
  \[ A_{Q2} = n A_{Q1} \quad n > 1 \]
- \[
[I_1 = I_2 = I_{\text{REF}} \Rightarrow V_A = V_B]
\]

- \( R_1 \cdot I_{\text{REF}} = V_{EB1} - V_{EB2} = V_T \cdot R_1 \cdot \ln(n) \)

**Temperature dependence:**
- \( R_1 \): positive TC
- \( V_T \): positive TC
- Start-up circuitry is needed
- Complementary structure available only in a p-well processes

### Current references based on a reference voltage

![Circuit Diagram]

- Useful when a reference voltage is available.
- This circuit has to operate at low-frequency (dc). The opamp gain can be extremely large.
- \( I_{\text{REF}} = \frac{V_{\text{REF}}}{R_1} \)

- M1 in saturation region, for current mirror

**Temperature dependence:**
- \( R_1 \): positive TC
- \( V_{\text{REF}} \): depends on the kind of voltage reference used

- It is difficult to obtain a stable \( V_{\text{REF}} \) with a small value.

**Voltage references**

**Introduction**

- Voltage references are required in a number of analog applications (e.g. signal processing, A/D converters, D/A converters, ...).
- Different voltage references
  - Supply voltage dividers
  - Voltage references based on a built-in voltage
  - Voltage references based on the band-gap voltage
  - Voltage references based on MOS threshold voltage difference

  (the last two types are actually special kinds of voltage references based on a built-in voltage).

- In the following, all voltages will be referred to GND
- Features for a reference current
  - Supply dependence
  - Temperature dependence
  - Technology dependence
Supply voltage divider

Resistive dividers

- Analog circuits normally have only two dc voltage supplies (Vdd and ground).
- In order to obtain dc-bias voltages, voltage dividers can be used.

\[
V_{\text{REF}} = \frac{R_2}{R_1 + R_2} \cdot V_{\text{DD}} = \alpha \cdot V_{\text{DD}}
\]

with \( \alpha < 1 \)

- Large power dissipation (small resistors) or large silicon area occupation (large resistors).
- \( V_{\text{REF}} \) depends on supply voltage.
- To obtain good matching, \( R_1 \) and/or \( R_2 \) are realized by means of a suitable number of unity resistors.

Supply voltage divider

Diode-connected PMOS transistors

- Body of M2 connected to source of M2 to avoid threshold voltage mismatches due to body effect.

Assuming \( V_{\text{TH1}} = V_{\text{TH2}} = V_{\text{TH}} \)

\[
V_{\text{REF}} = V_{DS2} = \frac{\alpha}{1 + \alpha} \cdot V_{DD} + \frac{1 - \alpha}{1 + \alpha} |V_{\text{TH}}|
\]

- Several diode-connected transistors can be connected in series, if allowed by the supply voltage ("diode chain") to reduce current level for a given \( V_{\text{TH}} \)

Supply voltage divider

Diode-connected NMOS transistors

- Resistive or capacitive dividers are complex or silicon area consuming.
- MOS in the diode configuration (i.e., operating in saturation region) can be used.

\[
\begin{align*}
|V_{\text{DS1}} - V_{\text{TH1}}|^2 &= \frac{k'}{2} |V_{\text{DS2}} - V_{\text{TH2}}|^2 \\
V_{DS1} + V_{DS2} &= V_{\text{DD}} \\
V_1 &= V_{DS1} = \frac{\alpha_2}{\alpha_1 + \alpha_2} \cdot V_{\text{DD}} + \frac{\alpha_1 \cdot V_{\text{TH1}} - \alpha_2 \cdot V_{\text{TH2}}}{\alpha_1 + \alpha_2}
\end{align*}
\]

\[
\alpha_1 = \sqrt{\frac{W_1}{L_1}}; \quad \alpha_2 = \sqrt{\frac{W_2}{L_2}}
\]

It results a voltage division of \( V_{\text{DD}} \) plus an offset.

Body effect on M2 can affect the operation (\( V_{\text{TH1}} \neq V_{\text{TH2}} \))

Supply voltage divider

MOS Supply voltage divider

Disturbs on the supply

If a signal \( v_{dd} \) (usually undesired and so a disturb) is superposed to \( V_{\text{DD}} \), the small signal equivalent circuit must be considered.

\[
\begin{align*}
C_2 &= C_{gs2} \\
C_1 &= C_{gs1} + C_{ds1} + C_{sb2} \\
f_p &= \frac{1}{2 \pi \left( g_m1 + g_m2 \right) C_1 + C_2} \\
f_z &= \frac{1}{2 \pi \left( g_m2 \right) C_2}
\end{align*}
\]

At low frequency (assuming \( g_m2 \gg g_{ds2} \) and \( g_m1 \gg g_{ds1} \)) there is a resistive partition (no capacitance effect):

\[
V_{1\text{f}} = V_{dd} \cdot \frac{g_m1 + g_m2}{1/g_m1 + 1/g_m2 + g_{mb}(g_m1 + g_m2)}
\]

At high frequency there is a capacitive partition (no resistance effect)

\[
V_{1\text{f}} = V_{dd} \cdot \frac{C_2}{C_1 + C_2}
\]

One of the two lines is valid depending if

\[
V_{1\text{f}} > V_{1\text{f}} \quad \text{(line I)} \quad \text{or} \quad V_{1\text{f}} < V_{1\text{f}} \quad \text{(line II)}
\]

It results a noise injection from the power supply (Vdd)
### Voltage references based on a built-in voltage

**Basic principle**
- Extraction of the chosen built-in voltage $V_{bi}$
- Generation of a current $I_{R1} = V_{bi}/R_1$
- Generation of a mirrored current $I_{R2} = k I_{R1}$
- Generation of the reference voltage $V_{REF}$ forcing $I_{R2}$ across a resistor $R_2$, matched with $R_1$

\[
V_{REF} = R_2 \cdot I_{R2} = R_2 \cdot k \cdot I_{R1} = k \cdot \frac{R_2}{R_1} \cdot V_{bi}
\]

- Temperature dependence of $V_{REF}$: it is a function of the temperature dependence of $V_{bi}$

### (Vth+Vov)-based voltage reference

- Built-in voltage: $V_{th} + V_{ov}$
- M1 to M5 in saturation region

\[
V_{REF} = k \cdot \frac{R_2}{R_1} \cdot V_{R1} = k \cdot \frac{R_2}{R_1} \cdot (V_{th} + V_{ov})
\]

- Generally $V_{ov}$ is made much smaller than $V_{th}$

**Temperature dependence:**
- $V_{th}$: negative TC
- $V_{ov}$: positive TC ($|V_{th}| + |V_{ov}|$: negative TC)

Start-up circuitry needed.
Complementary structure available

### VBE-based voltage reference

**Built-in voltage: $V_{BE}$**

M1 to M5 in saturation region

\[
(W/L)_3 = (W/L)_4 \Rightarrow I_3 = I_4 = I_{R1}
\]
\[
(W/L)_1 = (W/L)_2 \Rightarrow V_{R1} = V_{EB}
\]
\[
(W/L)_5 = k \cdot (W/L)_4 \Rightarrow I_{R2} = k \cdot I_{R1}
\]
\[
V_{REF} = k \cdot \frac{R_2}{R_1} \cdot V_{R1} = k \cdot \frac{R_2}{R_1} \cdot V_{EB}
\]

**Temperature dependence:**
- $V_{BE}$: negative TC.

- Start-up circuitry needed.
- Complementary structure for p-well processes.

### Voltage references based on the band-gap voltage

**Basic principle**

\[
V_{REF} = V_{BE} + m \cdot V_T
\]

where $V_T = kT/q$ is the thermal voltage.

- Suitable choice of $m$ to have zero TC at the desired operating temperature.
- At room temperature ($T = 300$ K):
  - $V_{BE}$: temperature dependence $\approx -2.2$ mV/°C
  - $V_T$: temperature dependence $\approx +0.086$ mV/°C.

- If $m \approx 25.6$ we have zero TC for $V_{REF}$
- At $T = 300$ K we have:

\[
V_{REF} = V_{BE} + 25.6 V_T \approx 1.26 \text{ V (silicon band-gap)}
\]
**Band-gap voltage reference**

- Q1, Q2: substrate BJT with different emitter areas
  \[ A_{Q2} = n \cdot A_{Q1} \]
  \[ n > 1 \]

\[ V_A = V_B \]
\[ R_2 = R_3 \Rightarrow I_{R2} = I_{R3} = I = I_{Q1} = I_{Q2} \]
\[ V_{R1} = V_{EB1} - V_{EB2} = V_T \cdot \ln(n) \]
\[ I = \frac{V_{R1}}{R_1} = V_T \cdot \ln(n) \]
\[ V_{REF} = V_{EB1} + R_2 \cdot V_T \cdot \ln(n) \]

where
\[ m = \frac{R_2}{R_1} \cdot \ln(n) = \frac{R_2}{R_1} \cdot \ln \left( \frac{A_{Q2}}{A_{Q1}} \right) \]

For ambient temperature:
\[ m = \approx 25.6. \]

Example:
\[ n = 8 \Rightarrow A_{Q2} = 8A_{Q1} \text{ (easy to obtain in layout)} \]
\[ R_2 = R_3 = \approx 12.3 \, R_1 \]

**Band-gap voltage multiplier**

- To be used when \( V_{REF} > 1.26 \, V \) is required

\[ V_{REF} = V_{BG} \left( 1 + \frac{R_A}{R_B} \right) \]

where \( V_{BG} \) is the band-gap voltage.
- The multiplier can be included in the feedback loop.

\[ V_{DD} \]
\[ V_{REF} \]
\[ R_A \]
\[ R_B \]

\[ V_{DD} \]
\[ V_{REF} \]
\[ R_A \]
\[ R_B \]

- For p-well processes.

\[ V_{REF} = V_{BG} \left( 1 + \frac{R_A}{R_B} \right) \]

**Voltage references based on MOS threshold voltage difference**

- M1 and M2: transistors with equal k’ and different threshold voltages, e.g.:
  - both enhancement transistors with different VTH
  - one enhancement and the other depletion transistor

\[ V_D3 = V_D4 \quad (W/L)_3 = (W/L)_4 \quad k_3 = k_4 \]

It follows that:
\[ I_3 = I_4 = I_1 = I_2 = I \]
\[ (W/L)_1 = (W/L)_2 \quad \rightarrow \quad V_{ov1} = V_{ov2} \]
\[ V_{REF} = -V_{GS2} + V_{GS1} = -V_{TH2} - V_{ov2} + V_{TH1} + V_{ov1} \]
\[ V_{REF} = V_{TH1} - V_{TH2} = \Delta V_{TH} \]

- \( \Delta V_{TH} \) is generally small. A voltage multiplier is required.
- Spread in threshold voltages, hence in \( \Delta V_{TH} \)
- Offset of the operational amplifier affects \( V_{REF} \)