Development of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Important

NEED FOR INTEGRATED CIRCUIT

The need for high density analog signal processing in the low and intermediate energy nuclear physics community is widespread. No commercial microchip is currently available with the following requested features:

1) Particle identification (α particle, γ-ray, *etc.*) capability using PSD technique
2) Ability to support multiple (*i.e.* initially eight but eventually sixteen) radiation detectors
3) Three separate integration regions with independent control of charging rate in each region which can be used for high-quality pulse shape discrimination (PSD).
4) Built-in high-quality timing circuitry
5) Multiple (currently, three) triggering modes
6) Analog multiplicity output indicating number of detectors impacted by radiation
7) Can be used with wide variety of detectors (CsI, photodiode, liquid scintillator)
8) Provides data sparsification

INTENDED APPLICATIONS

The integrated circuit (IC) will be suitable for use in recently planned nuclear physics experiments. One has already been approved by the National Superconducting Cyclotron Laboratory (NSCL). The experiment is to be performed in Fall of 2007. The microchip currently under design uses a technique known as pulse shape discrimination (PSD) to classify the radiation type (*i.e.* α particle, γ-ray, *etc.*).

While circuits capable of particle identification *are available* in discrete analog form (bulky!) and in digital form (power-hungry!), none are available in a low-power, small, integrated form. As a result, mass production of PSD technology (at a reasonable cost) is currently unavailable, but is actively being sought by our government's Department of Homeland Security. Our research has the potential to **greatly reduced false positives** from detectors sensitive to different types of radiation. **Thus, our IC may someday play an important role in the detection of nuclear attacks launched by terrorists against our nation!**
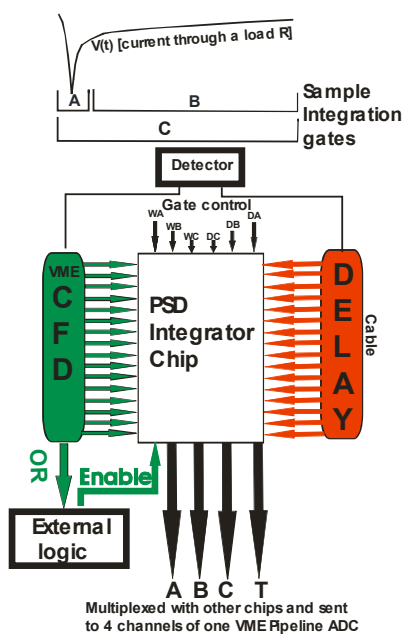
GENERAL DESCRIPTION

Our research group is currently developing a micro-chip we call PSD8C. The research is funded by a two-year, $200,000 grant from NSF (National Science Foundation). PSD8C (Pulse Shape Discrimination, 8 Channel) is an 8 channel integrated circuit (IC) for use in experiments in low- and intermediate-energy nuclear physics where particle identification (α particle, γ-ray, *etc.*) is important. The IC will be fabricated (August 2007) in the AMIS 0.5 μm, N-well, double-poly, triple-metal, high-resistance C5N process available through MOSIS. Below is a brief description of how it all works.

Detector outputs will be split for logic and linear branches. Timing signals would be generated by leading-edge or constant-fraction-discriminators. The individual timing signals and delayed linear signals would be sent to the chip. The pulse-shape discrimination scheme with a 16-channel chip is illustrated below (see System Overview). The individual CFD logic signals ANDed with a global enable signal provide channel enables. For each linear signal (accompanied by its logic), three different integrations (called **A, B** and **C**) would be performed with start times referenced to the individual discriminators. In addition, an amplitude **T** will be produced proportional to the difference between the individual discriminator and an external common stop reference.

The delays in the integrators starting times (D_A, D_B, D_C) and the widths (W_A, W_B, W_C) of the integration windows are controlled by the user on a chip-by-chip basis. In the figure, the delays D_A, D_B, D_C are voltages that are converted to times on-chip as are the widths W_A, W_B, W_C. Each channel (see Typical Channel) in the multi-channel IC is composed of three sub-channels and a time-to-voltage converter (TVC). The sub-channels produce the three different integrations (**A, B** and **C**), and the TVC (Time-to-Voltage Converter) will produce the amplitude **T** that will be proportional to the difference in time between the channel's discriminator firing and an external common stop reference. Aside from the user controlled delay and widow widths, the feature that allows this chip to be used with detectors as diverse as liquid scintillators (fast) and CsI (slow) is a bank of eight resistors (for each sub-channel) which determine the charging rates of the integrating capacitors. The architecture of a typical sub-channel is also depicted below.

A *common* channel provides biasing for the 8 (eventually 16) processing channels and contains readout electronics. A 48-bit configuration register allows the user to selectively disable CFD outputs on a channel-by-channel basis, select test modes, select charging rates of integrator capacitance, select voltage-to-time conversion characteristics, select TVC measurement range, and assign an 8-bit ID to the chip. One of three triggering modes can also be selected. The chip only responds when an externally applied chip address matches the ID stored in the chip's
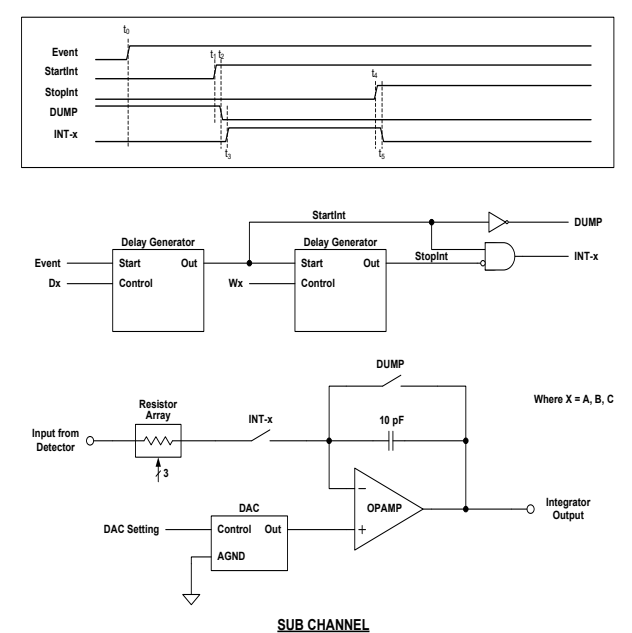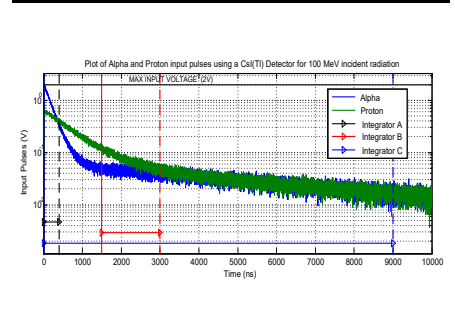
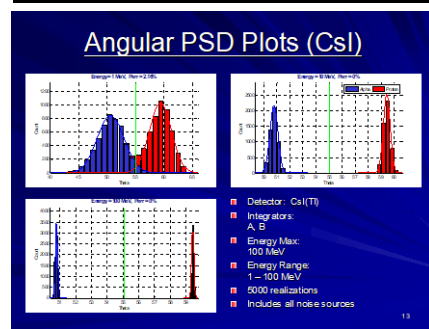### System Overview

Typical Channel

FULL CHANNEL
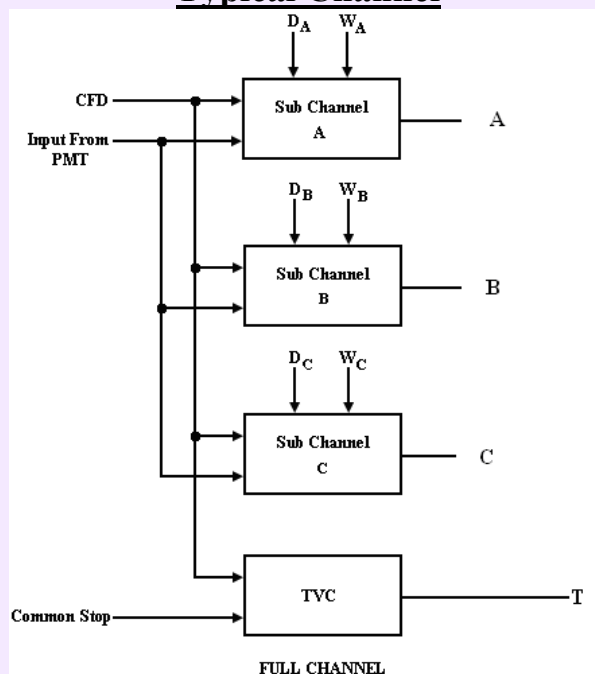
Sub-Channel

SUB CHANNEL

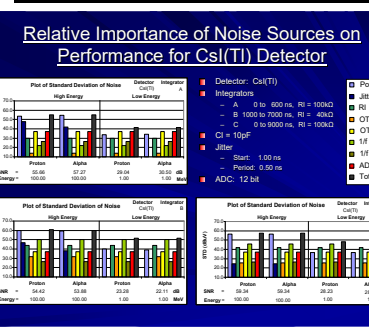## SIMULATED PERFORMANCE

REPRESENTATIVE PULSE SHAPES

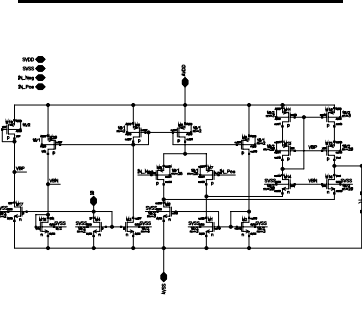### PULSE SHAPE DISCRIMINATION

CAREFUL NOISE ANALYSIS

INTEGRATOR AMPLIFIER

REFERENCES

Detailed electrical descriptions and updates:

http://www.ee.siue.edu/~gengel/PSD.htm

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