

# Enhanced Pulse Shape Discrimination (PSD) System For Nuclear Physics Applications

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Design Status

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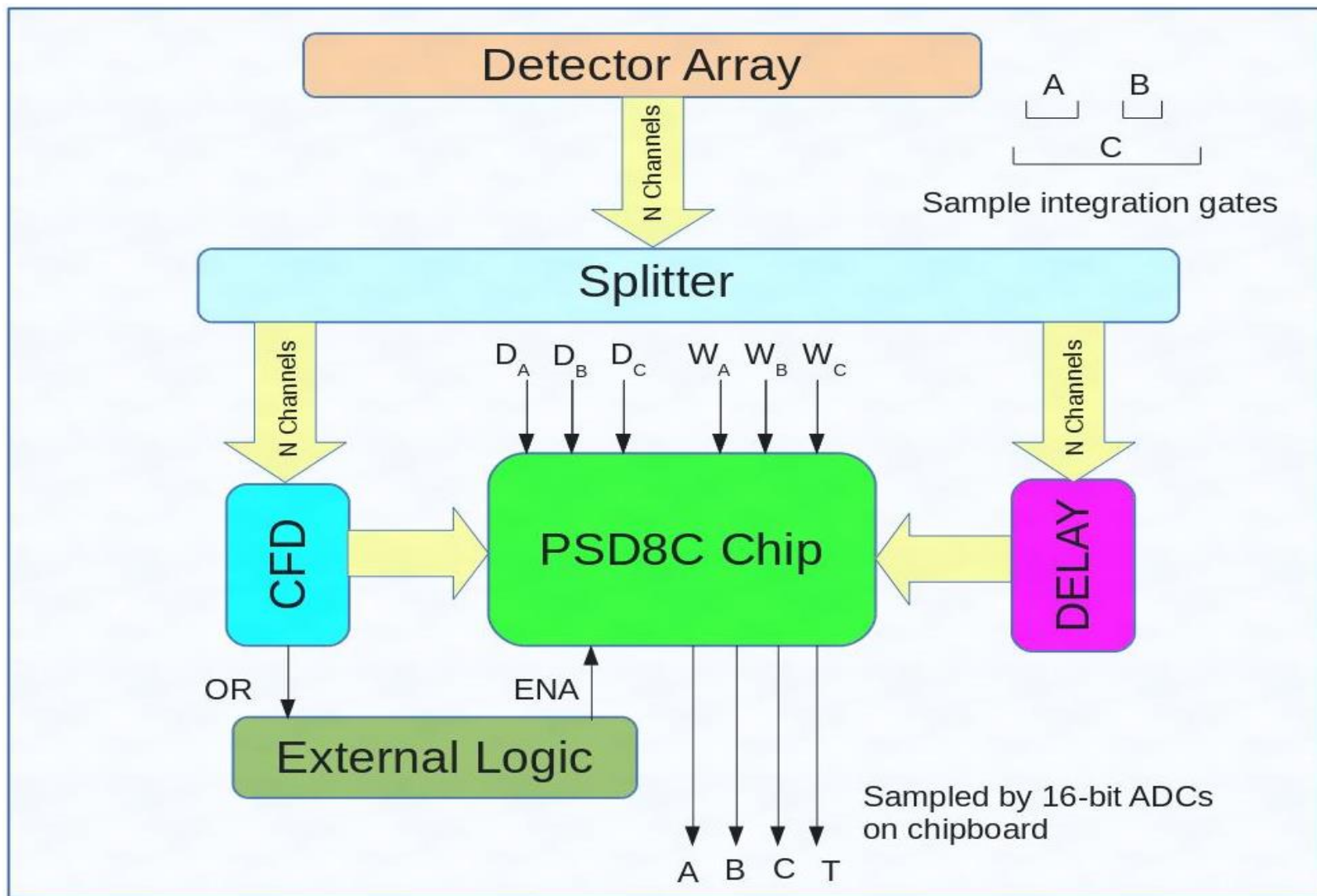
# Presentation Outline

- PSD Chip and System Overview
- PSD3 Shortcomings
- PSD4 (Enter our 4<sup>th</sup> Generation IC!!!!)
- **Scheduled for fabrication ... Dec. 4, 2017**
- Summary

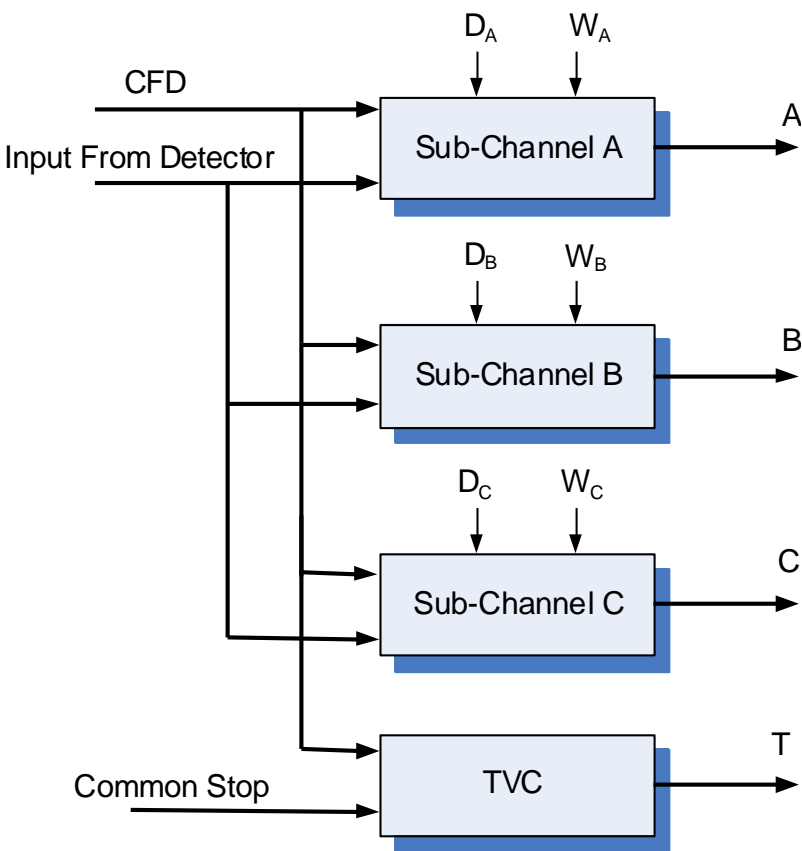
# Our PSD Chip

- PSD3 (3<sup>rd</sup> Generation IC) is our current mass integrator chip (8 channels) capable of yielding particle identification from scintillators with pulse-shape discrimination.
- Nine years ago we fielded an ASIC (PSD1 i.e. 1<sup>st</sup> Generation), which when used in conjunction with external discrimination, can be used to generate the integrals from three user selected regions of the light pulse from a scintillator .
- Our chip greatly simplifies the task of creating a large array of scintillators that contain particle identification information in the pulse shape.

# PSD System

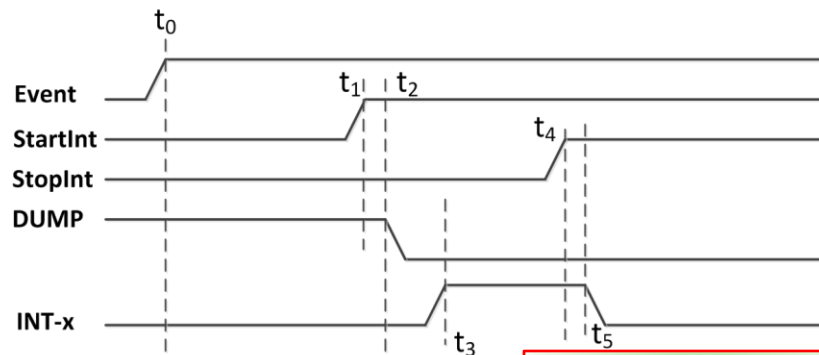


# PSD Chip Overview

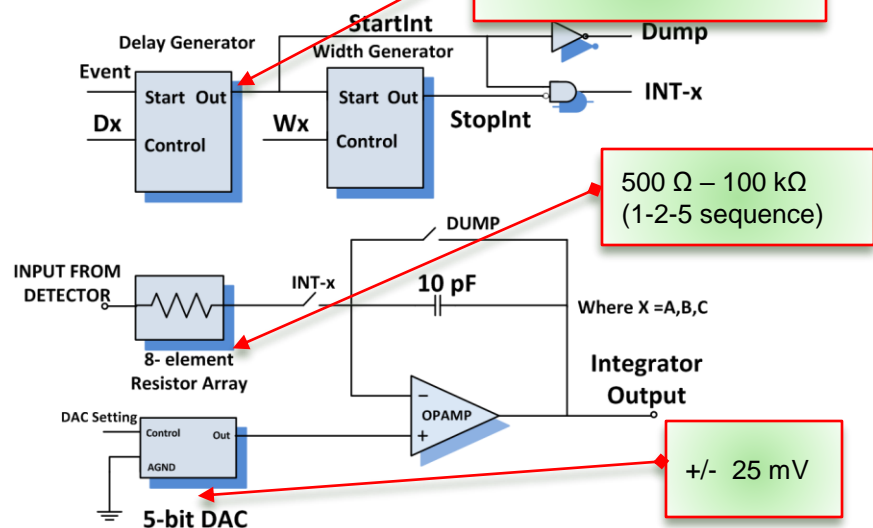


PSD3 TVC ranges (500 ns, 2  $\mu$ s)  
PSD4 TVC ranges (250 ns, 2  $\mu$ s).

PSD8C Channel



20 ns – 70 ns, 50 ns – 300 ns  
200 ns – 1.5  $\mu$ s, 1  $\mu$ s – 10  $\mu$ s



500  $\Omega$  – 100 k $\Omega$   
(1-2-5 sequence)

+/- 25 mV

PSD8C Sub-Channel

## PSD3 Works Well ... But ! (Part I)

- PSD3 operates from a single 5 Volt supply. The use of 5 Volts helps ensure a large dynamic range but the FPGA which directly interfaces to the IC operates at 3.3 Volts, cluttering the chip-board with a large number of level translators.
- Analog signals (A, B, and C integrator outputs) from PSD3 come off chip differentially and are digitized by off-chip ADCs. Since the IC supports both negative and positive polarity inputs, it is necessary for the off-chip ADC to “swap” the differential input lines when processing negative polarity inputs. The only 16-bit ADC currently available to do this “swap” is the Linear Technology’s LTC1865.

## PSD3 Works Well ... But ! (Part II)

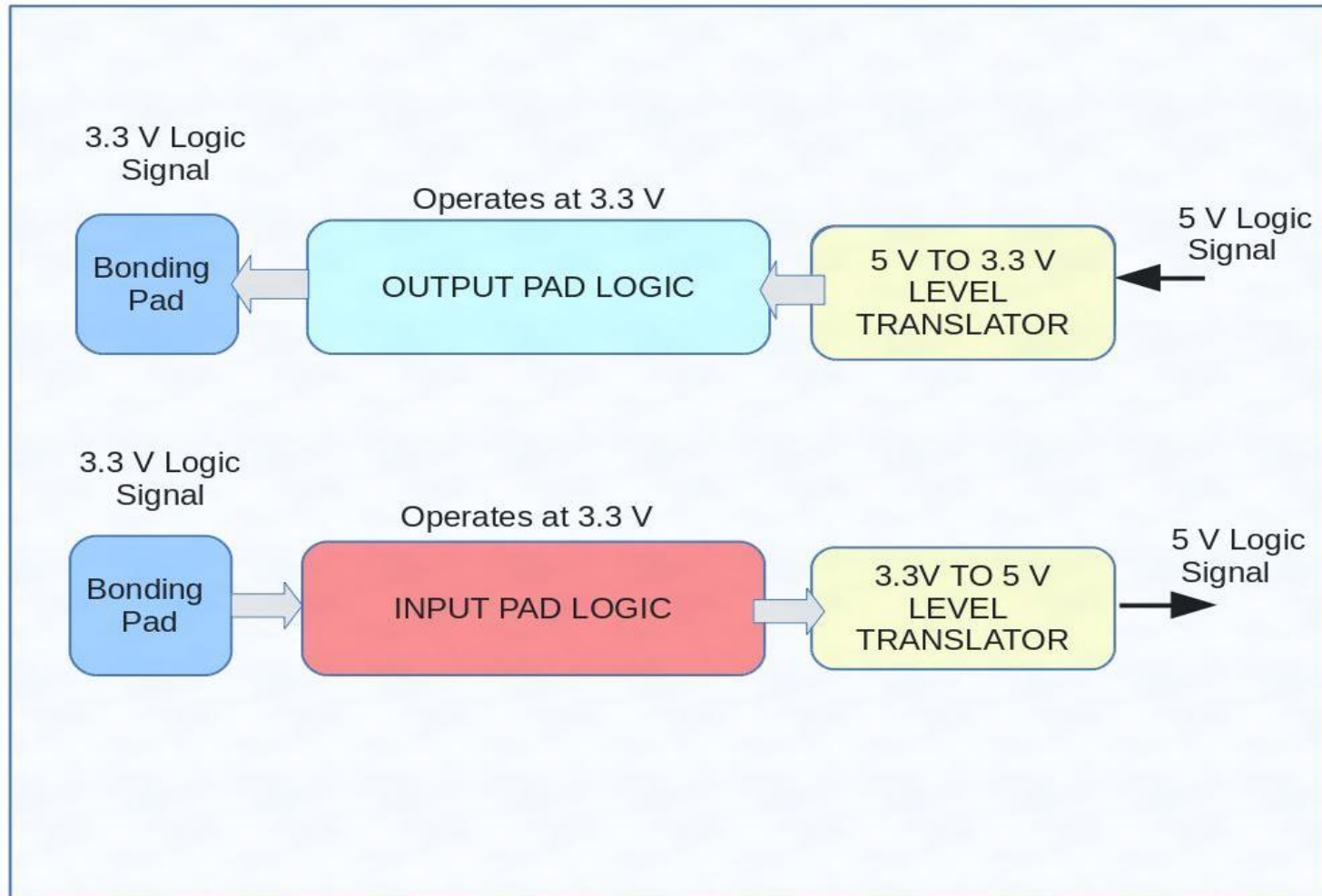
- The on-board time-to-voltage converters (TVCs) suffer from a logic bug (which has a work around, thankfully!)
- While the TVC timing resolution is acceptable for most applications, some potential applications would benefit from improved resolution.

## Enter PSD4 (our 4<sup>th</sup> Generation IC)!!!

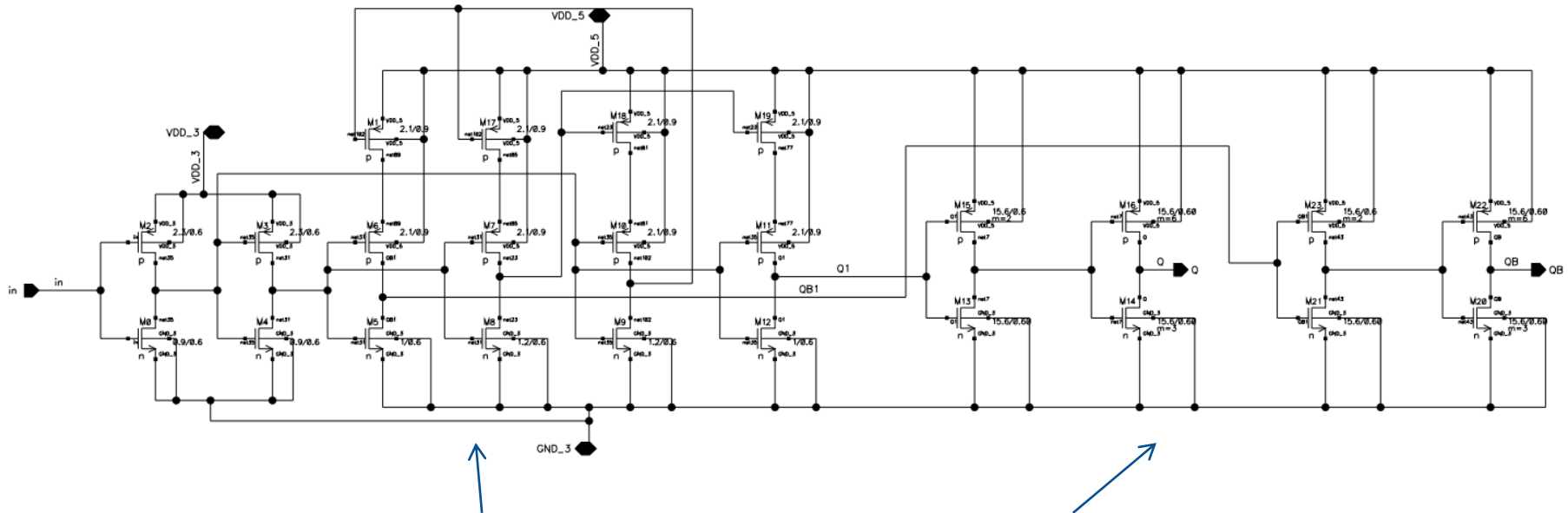
- Let's walk through the enhancements one-by-one!!!
- We'll look at schematic-level changes, modified layout, and simulation results.



# Addition of Level Translators



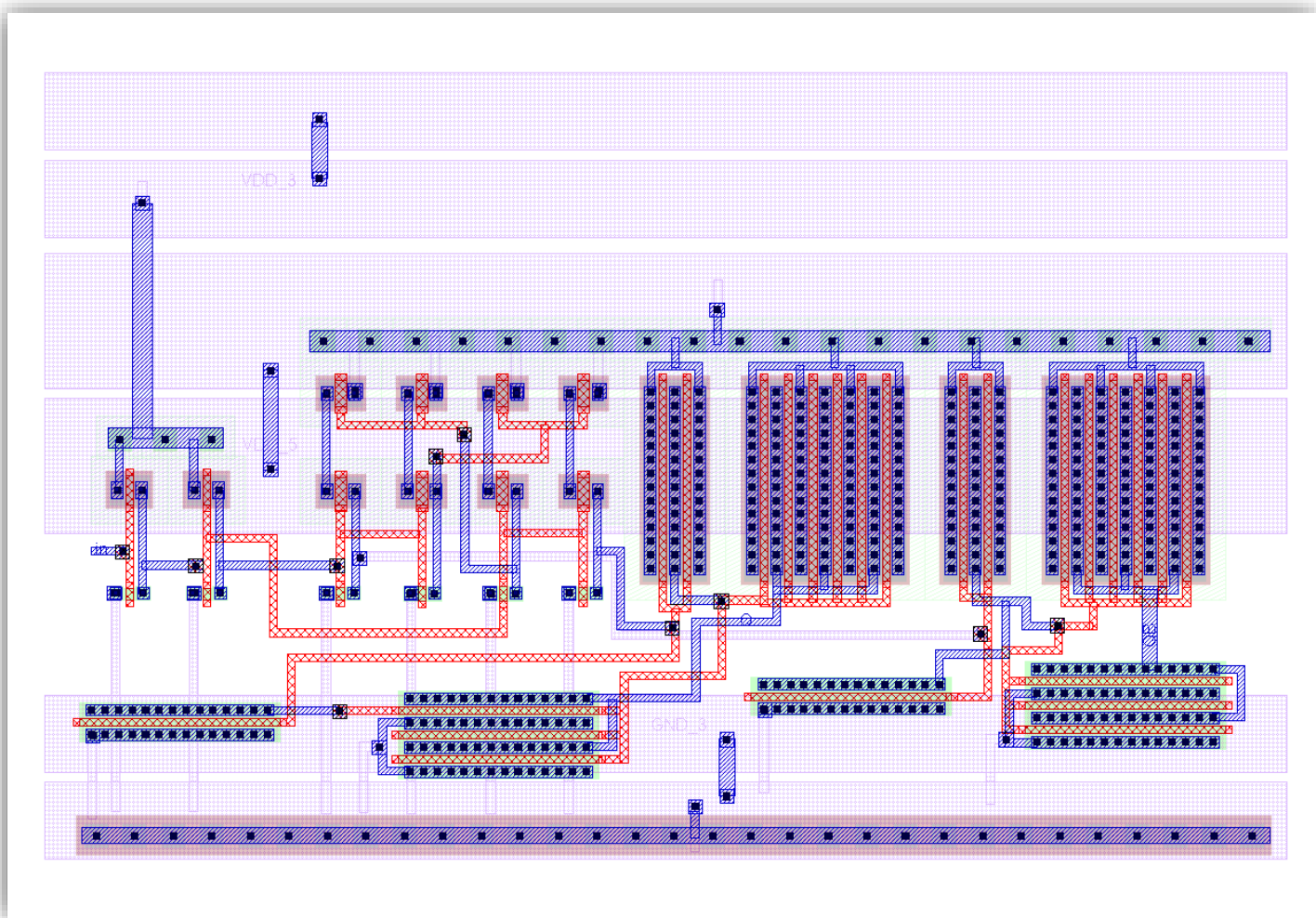
# Level Translator Schematic



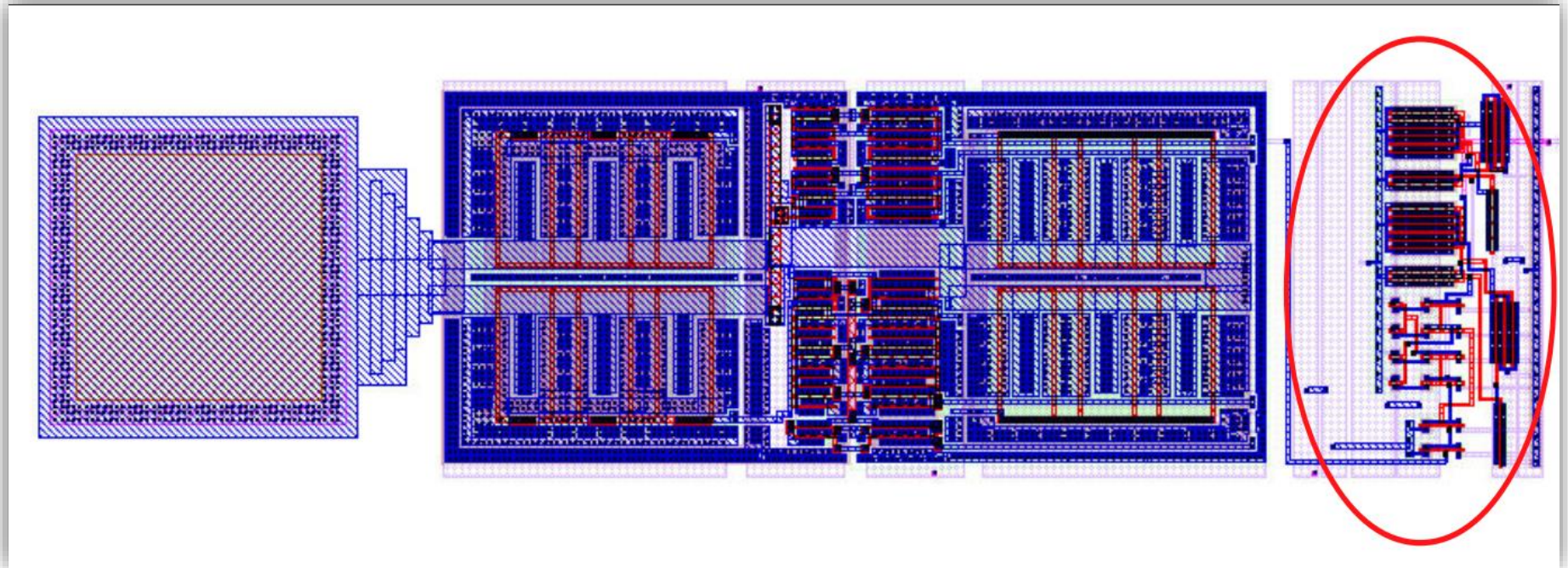
Level shifters.

Buffers similar to those in original pad.

# Level Translator Layout

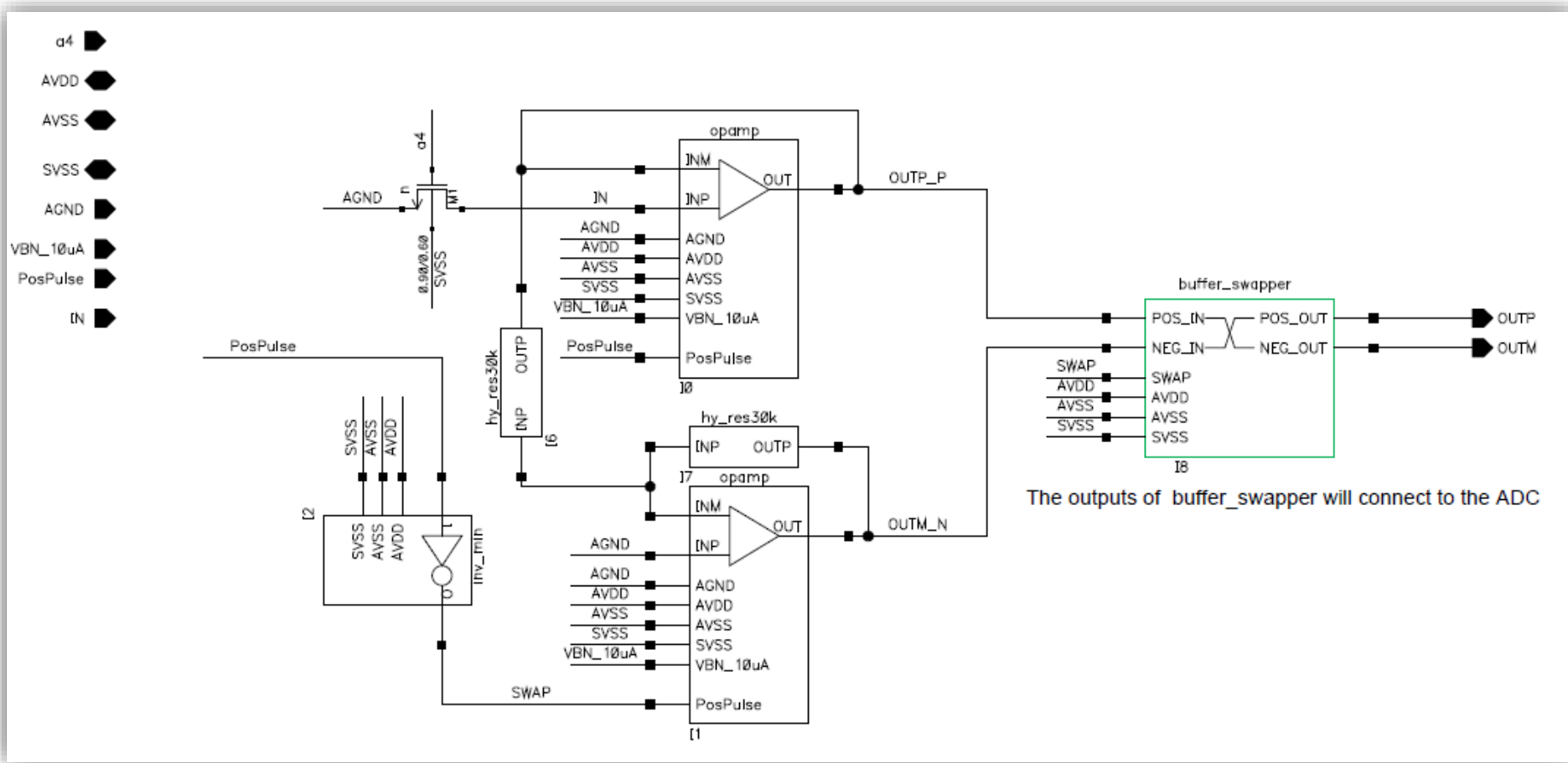


# Digital I/O Pad With Level Translation!



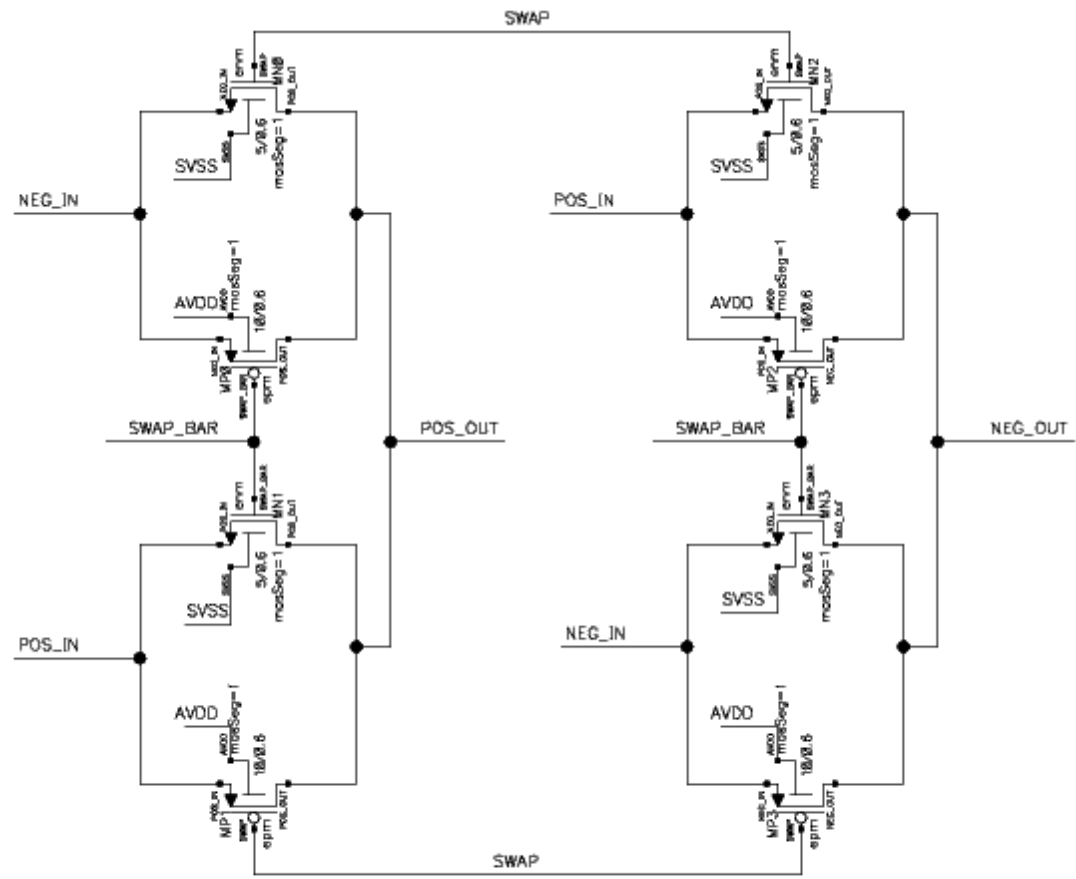
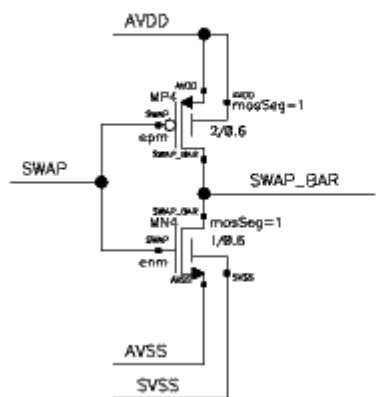
Internal pull-down resistors ( $10\text{ K}\Omega$ ) were also added to the bi-directional pins used by the chip ID bus.

# “Swapper” Function Added to PSD4

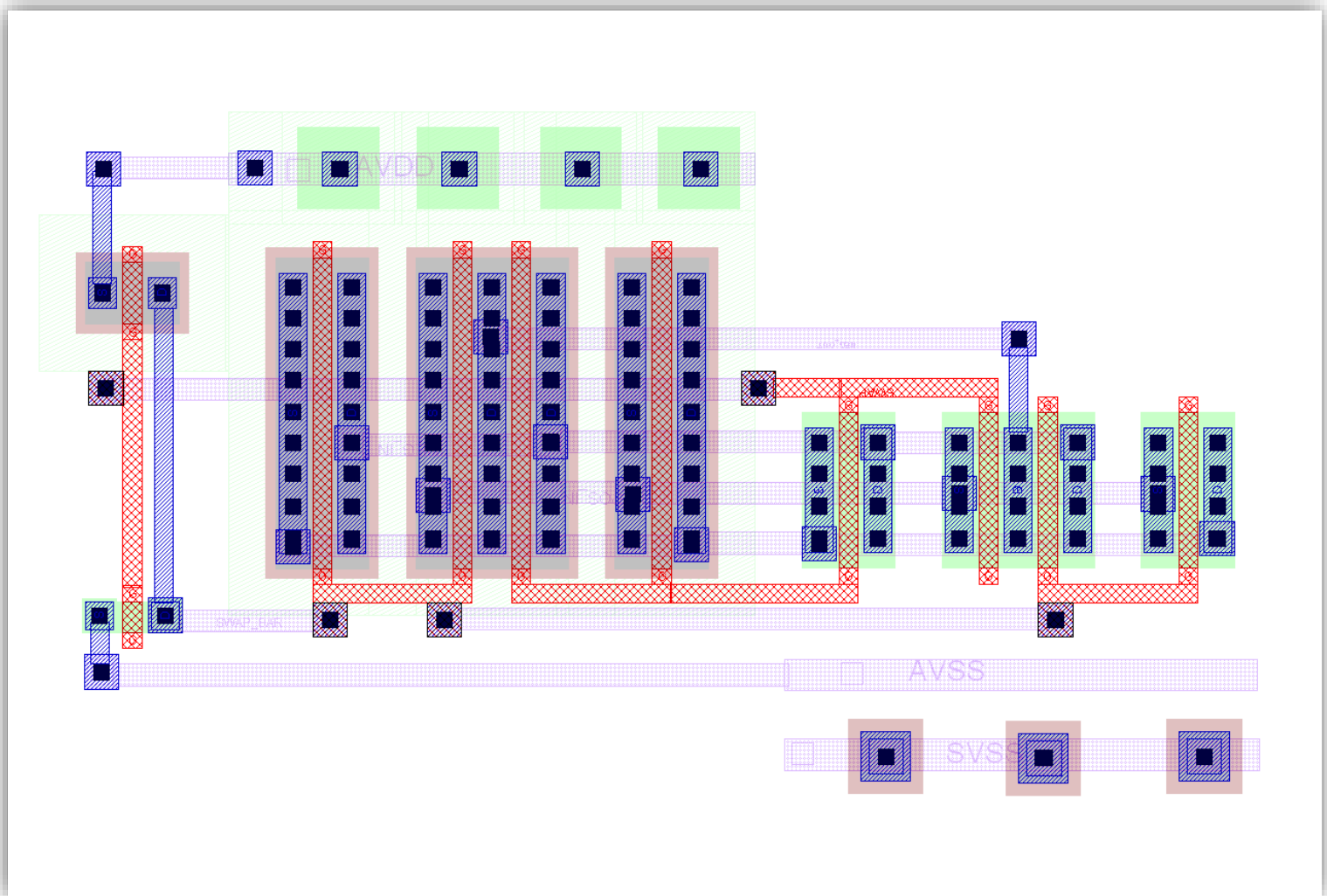


# “Swapping” Outputs is Easy!

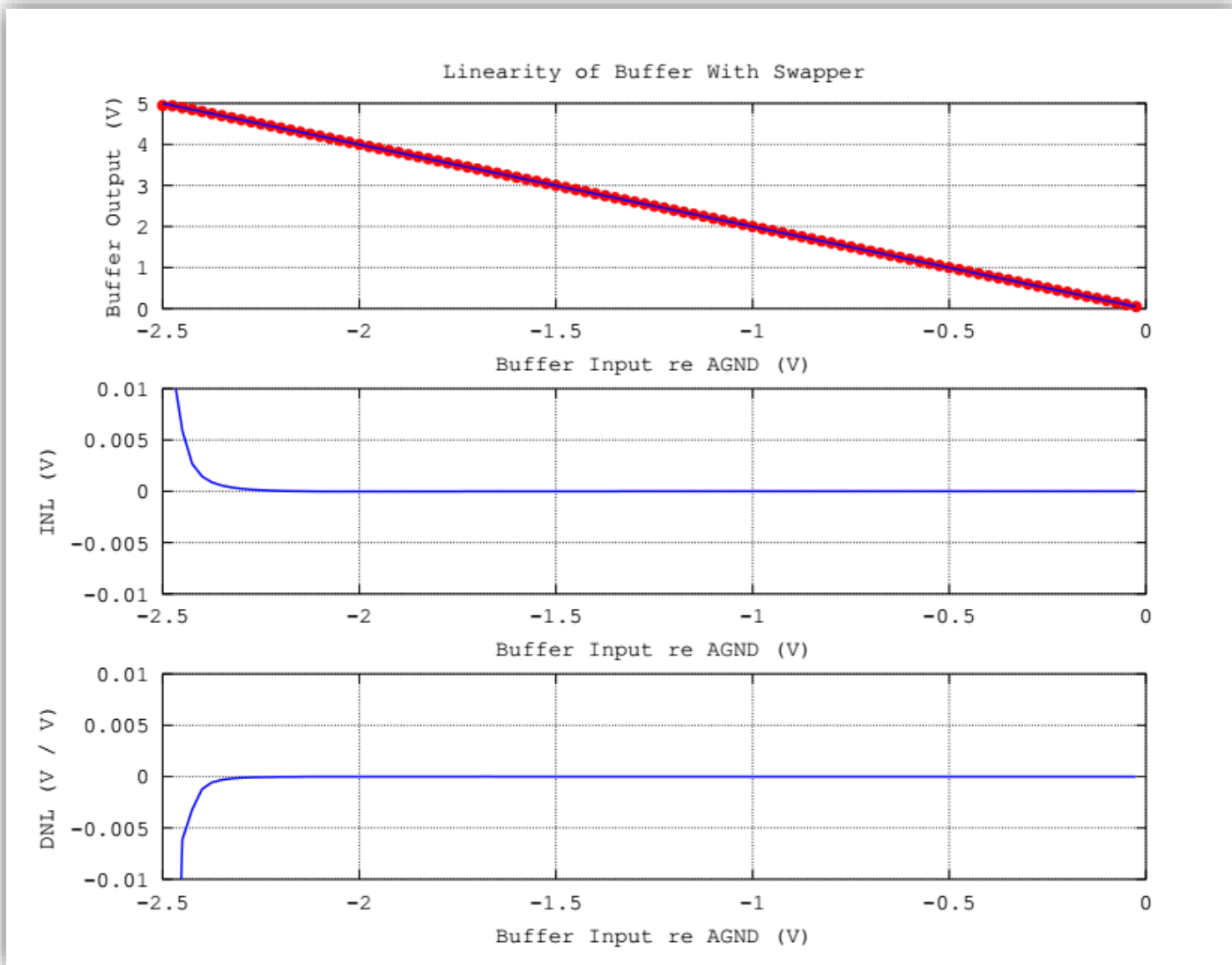
- SWAP
- AVSS
- AVDD
- SVSS
- NEG\_IN
- POS\_IN
- POS\_OUT
- NEG\_OUT



# “Swapper” Layout

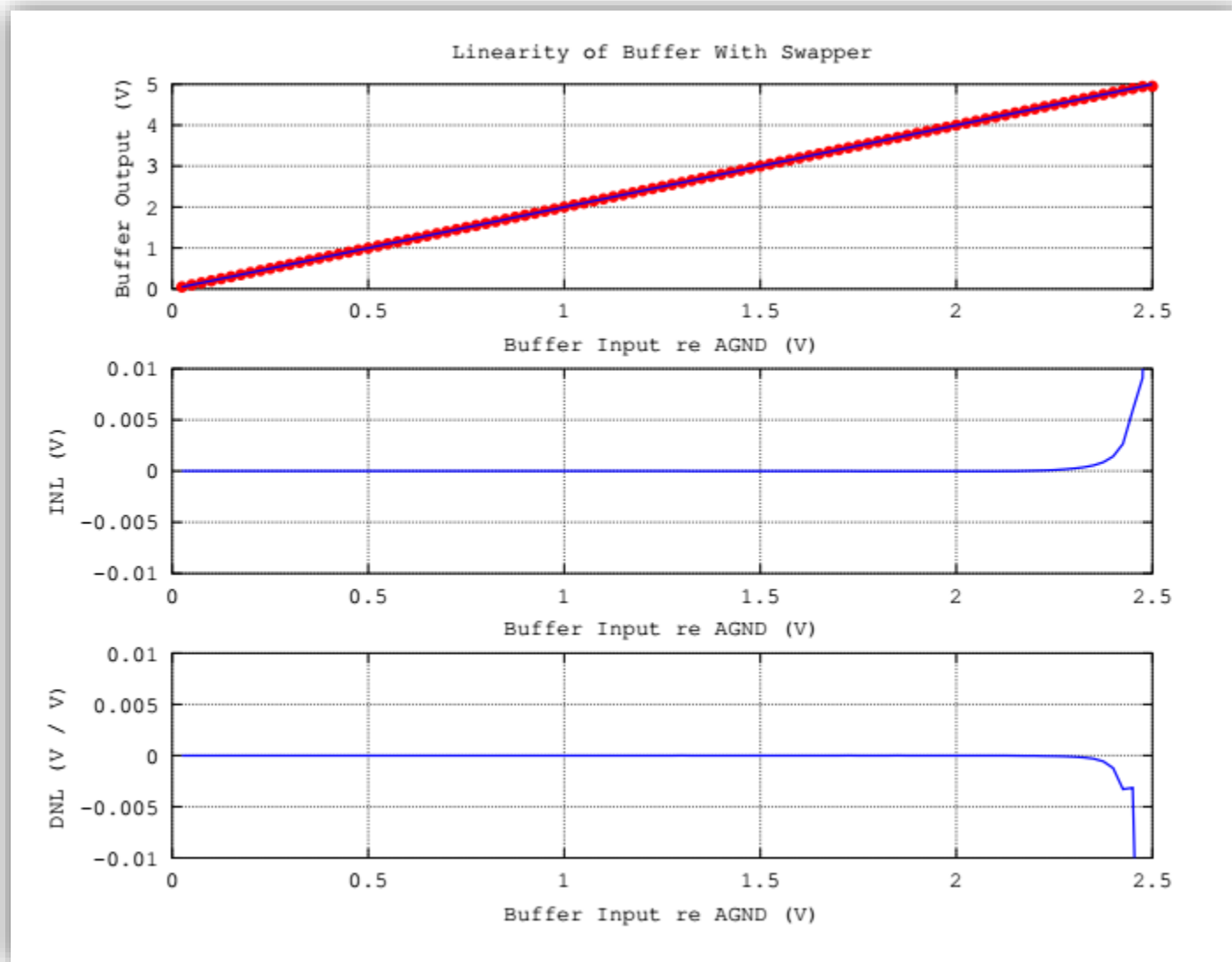


# Linearity of Buffer with “Swapper”

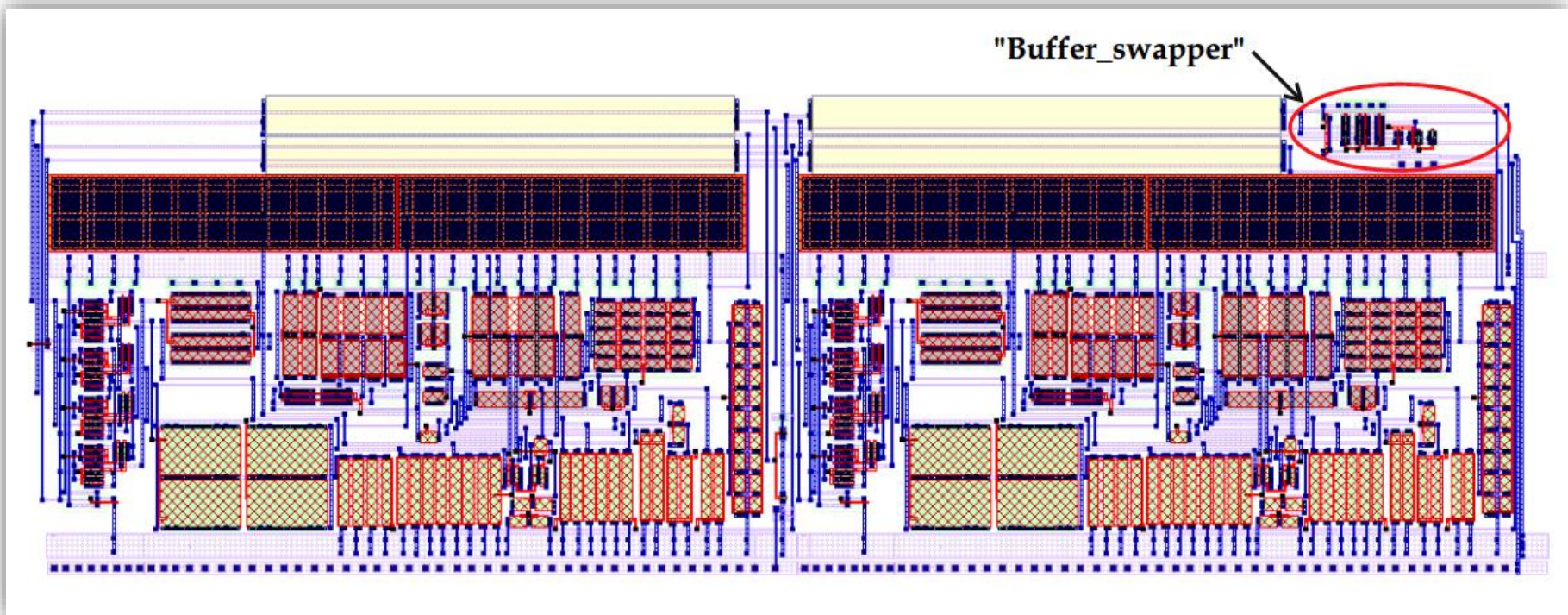




# Linearity of Buffer with “No Swapper”

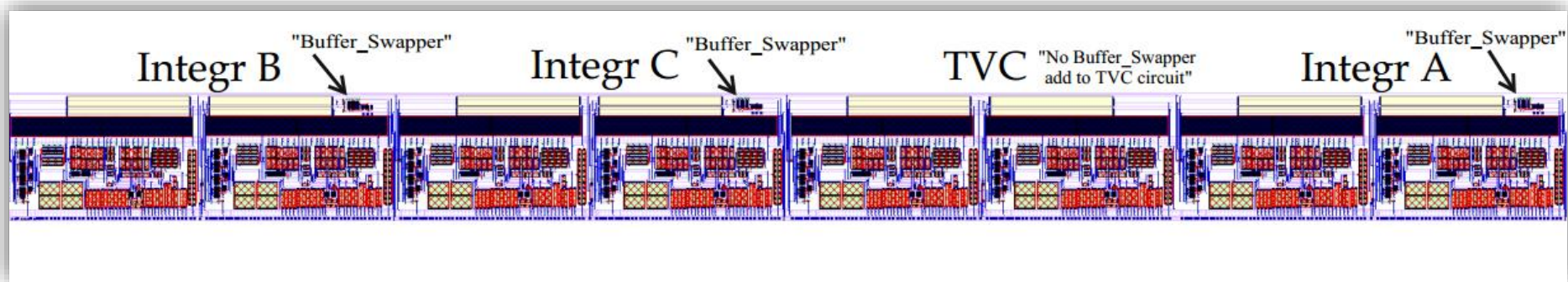


There was just a enough room ... Whew!!!!



# Changes to the Off-Chip Driver Block

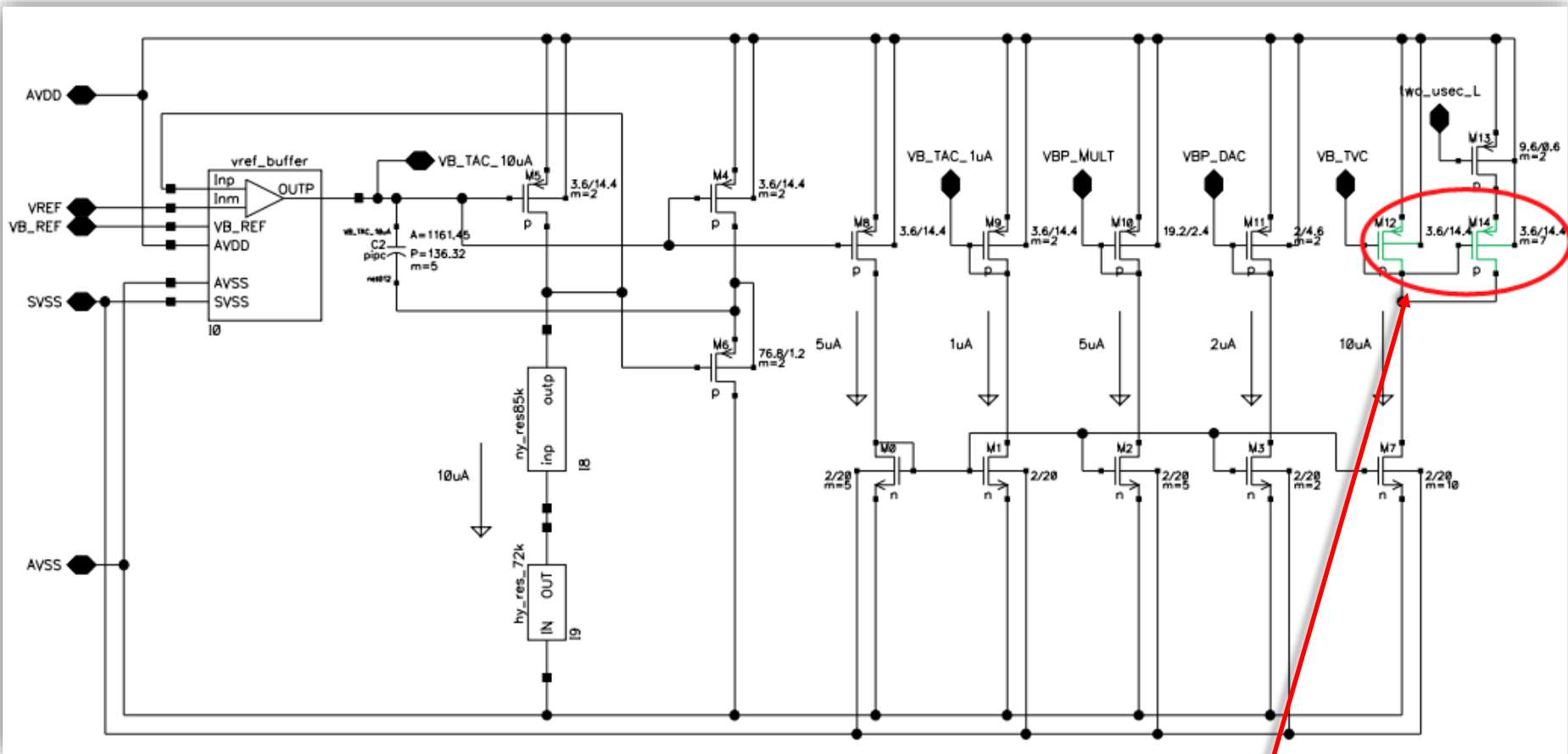
The “Swapper” circuit was only added to the integrator A, B, and C output buffers. The TVC output is always of one polarity!



# Change 500 ns TVC range to 250 ns

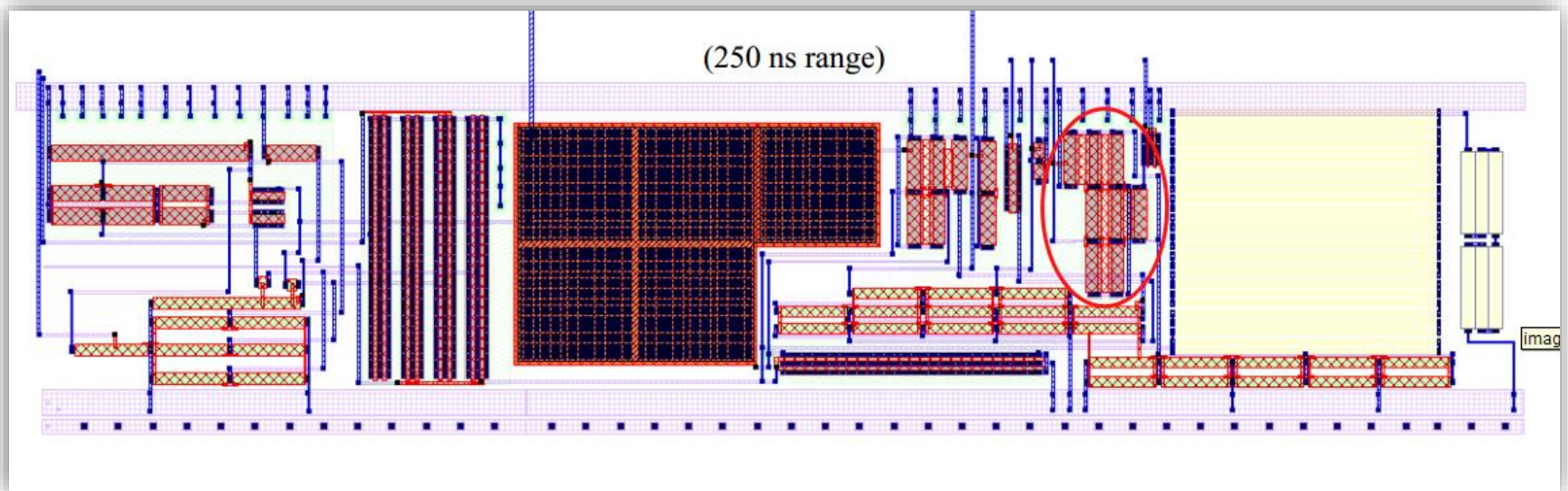
- This change will improve the timing resolution but range is so short that it would be almost unusable unless we delay the start of the TVC.
- We decided for PSD4, rather than start the TVC on the **rising** edge of the CFD pulse, we would start the TVC on the **falling** edge of its CFD input. Width of CFD pulse implements the delay that we need! This implies that **both** edges of the CFD pulse must possess very low jitter. Integrator delays are still relative to the rising edge of the CFD pulse, just as in PSD3.
- *A common stop* signal stops the TVCs in all channels.

# Double Current for 250ns Mode



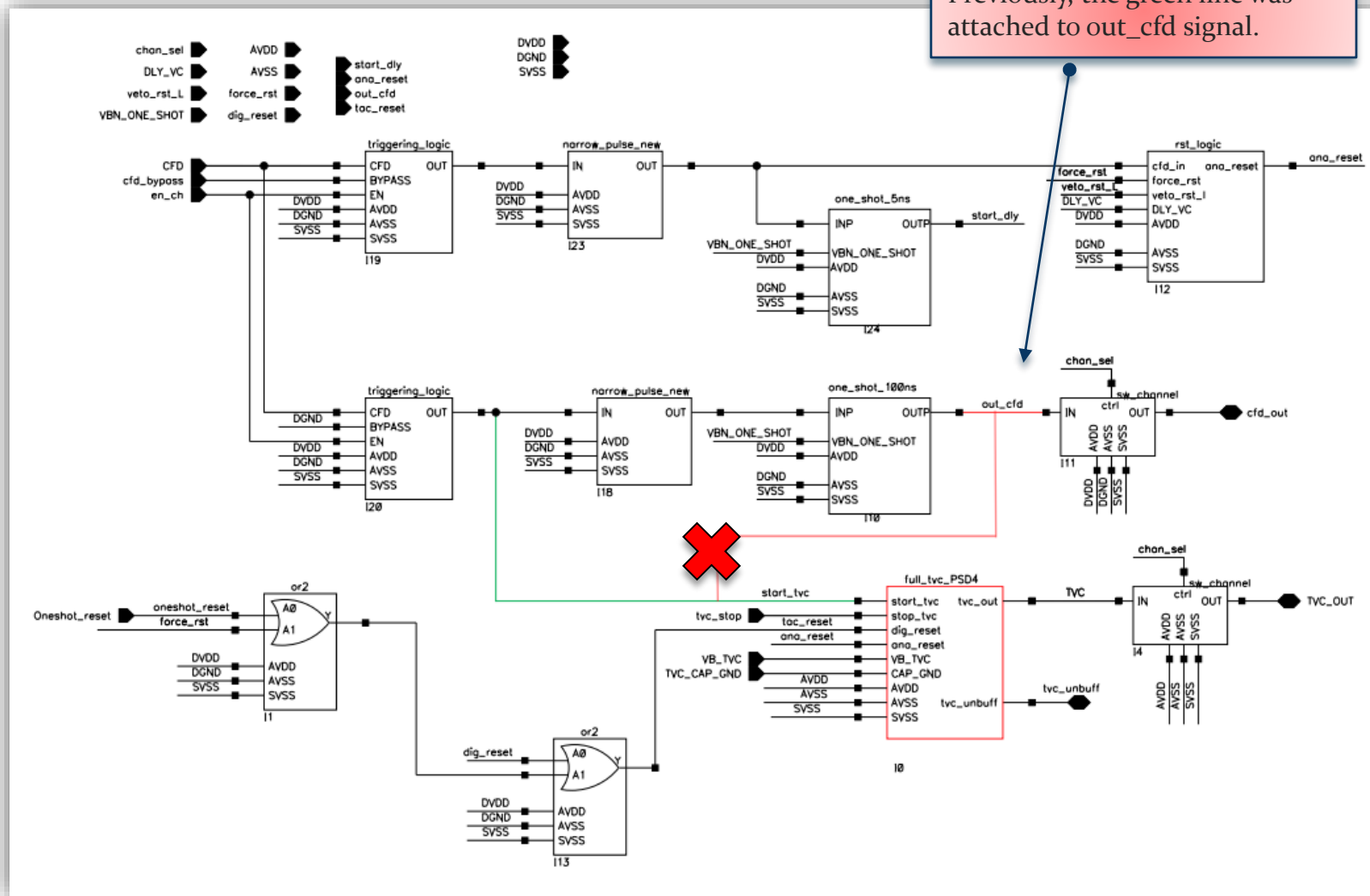
We Changed the size of M12 (m=2) and M14 (m=6) to M12 (m=1) and M14 (m=7)

# Small Layout Change in Constant Current Source Cell



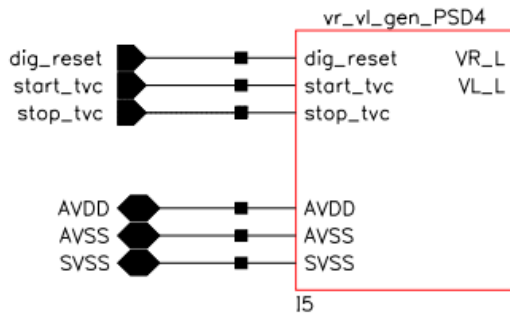
# TVC Needs to See Original CFD Signal

Previously, the green line was attached to out\_cfd signal.



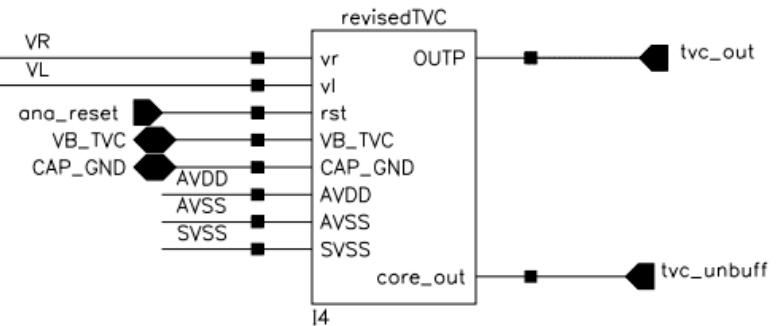
# TVC Circuit Modifications

## Digital (Changed)



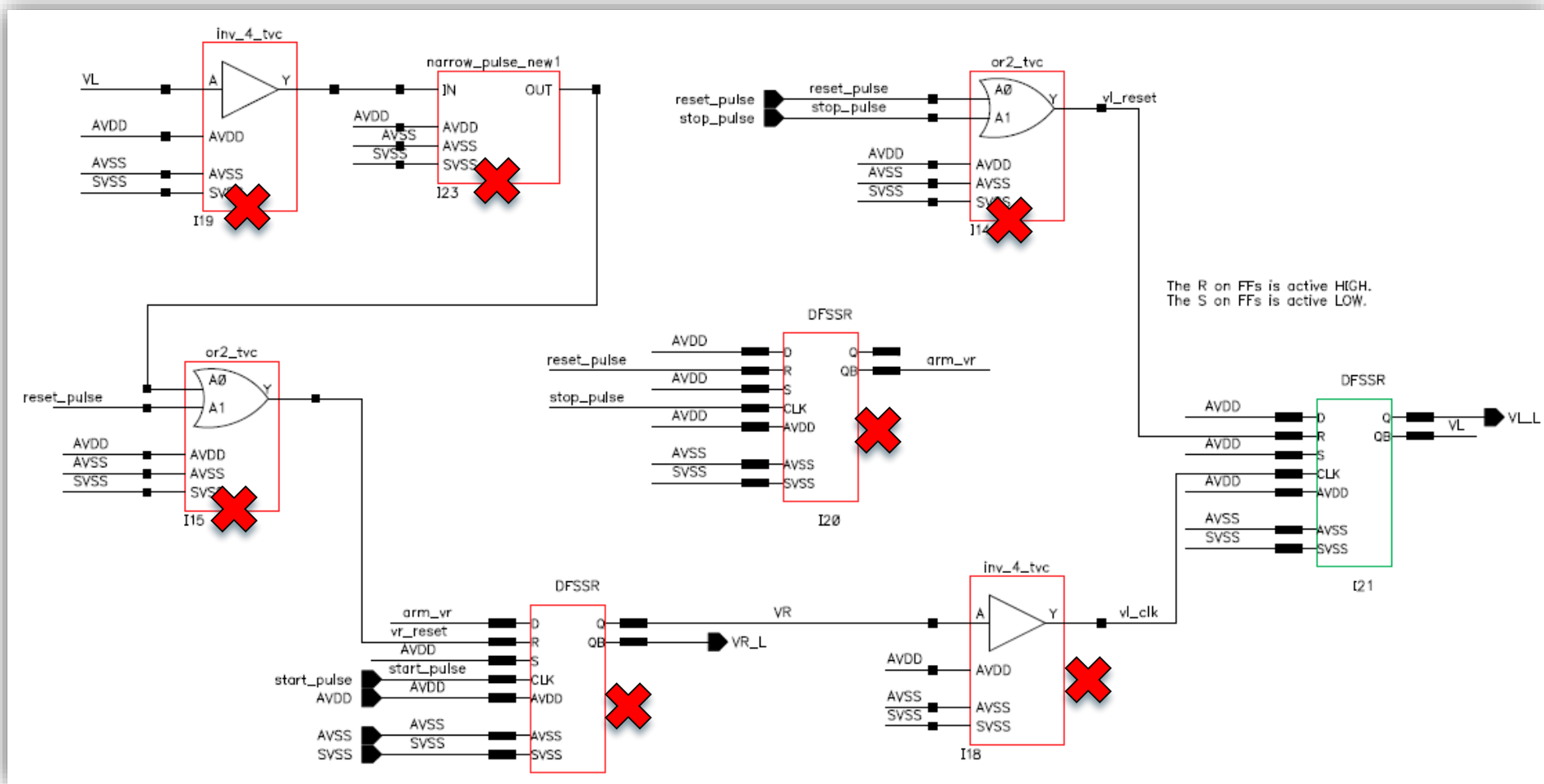
VR and VL are active low signals.  
They drive the gates of PFETs.

## Analog (Not Changed)



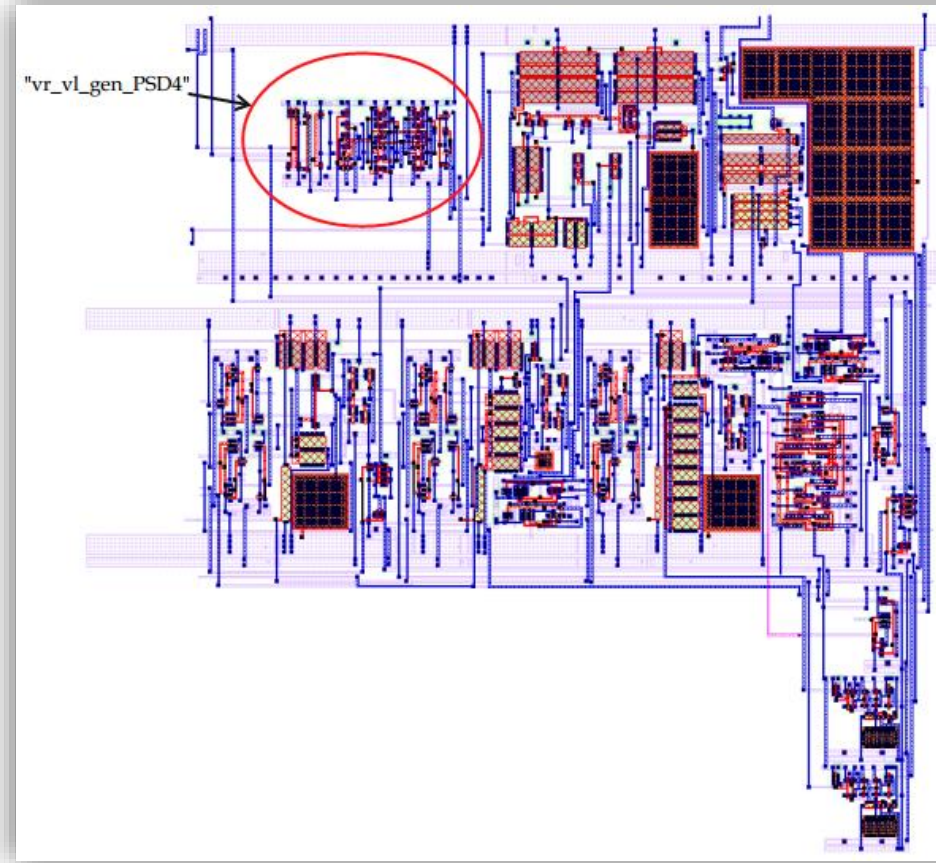
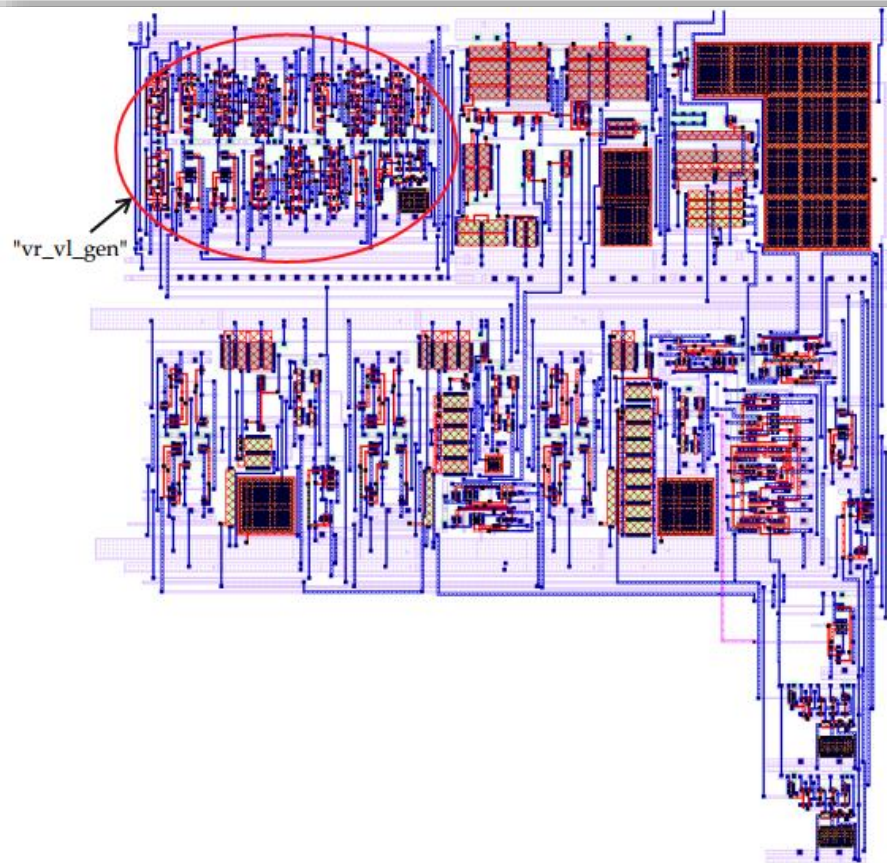


# Digital Control Simplified

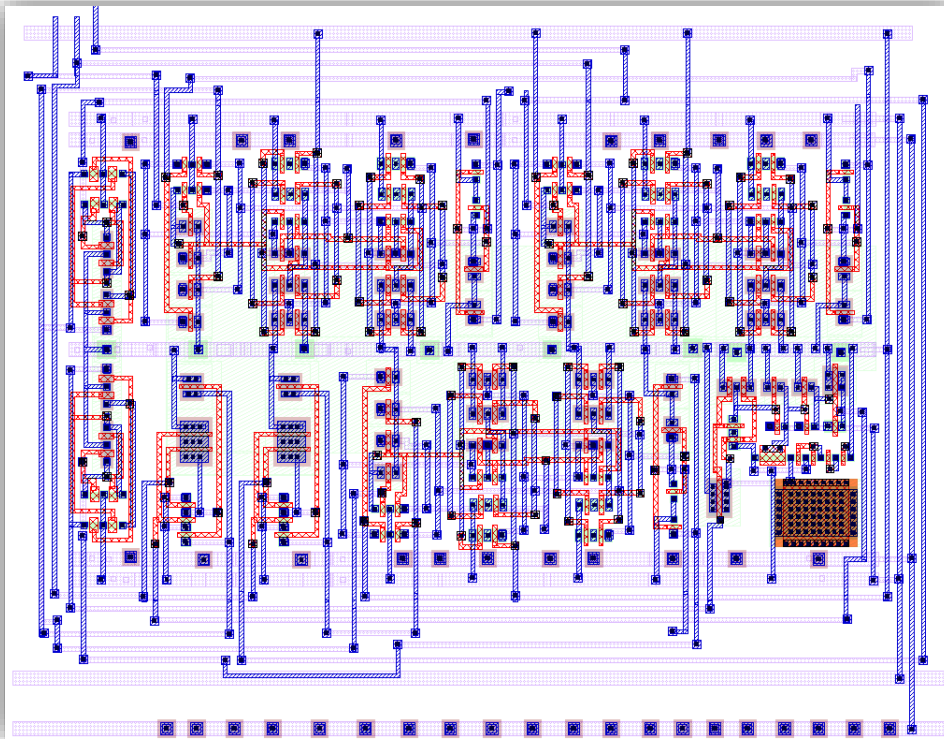




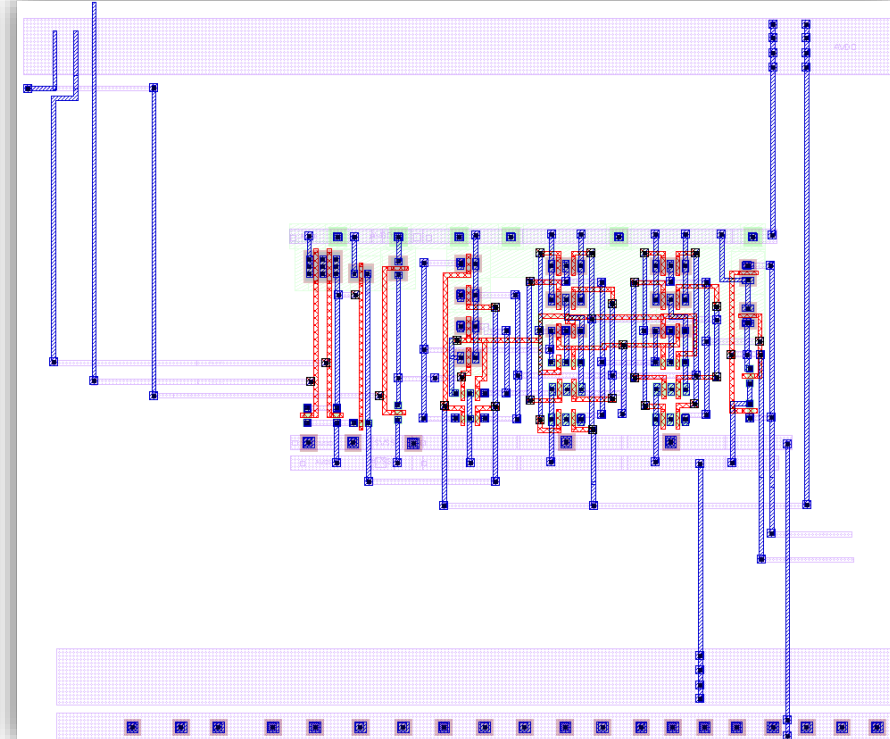
# TVC Layout (before and after!)



# Let's Go in For a Better View!

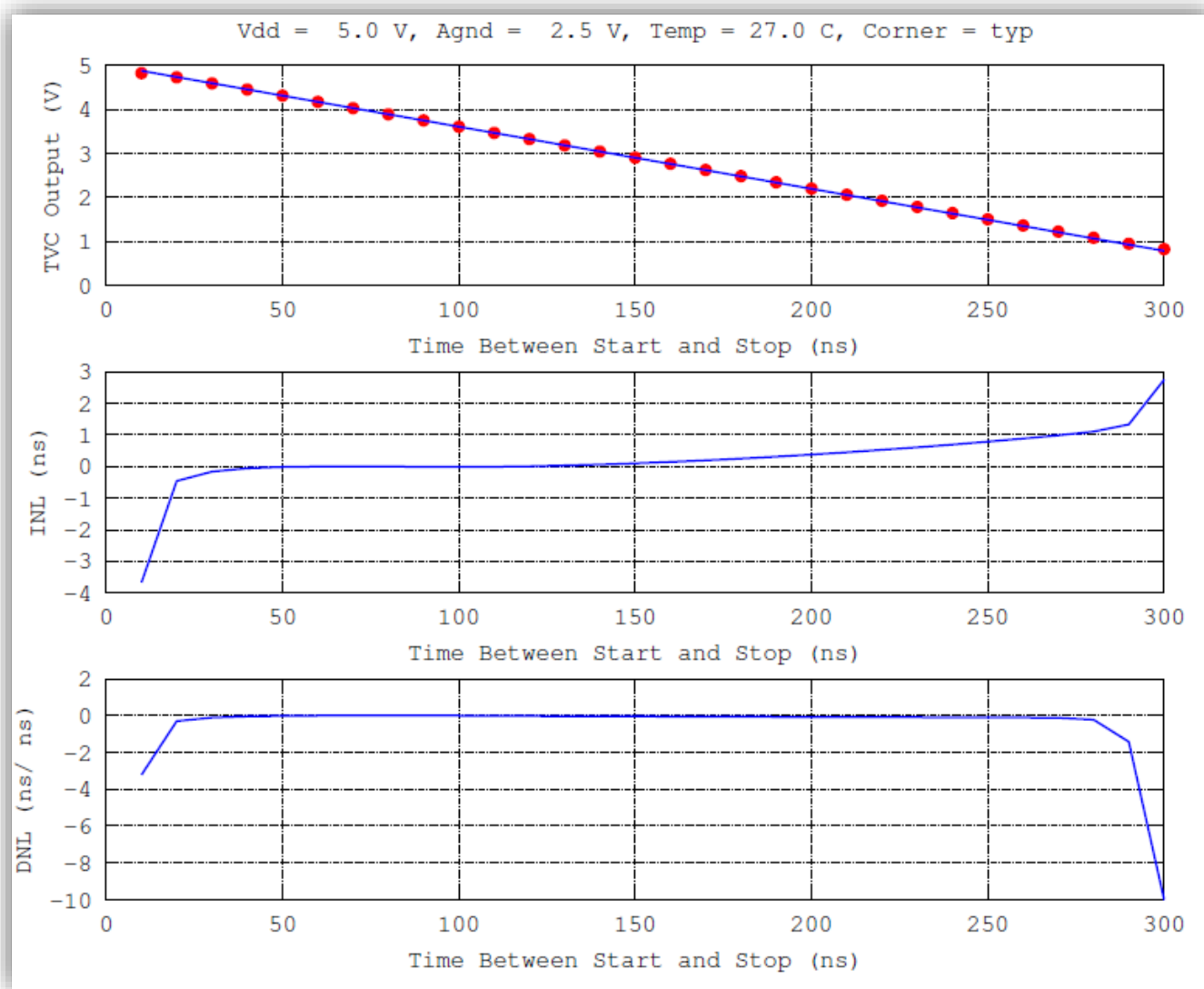


BEFORE



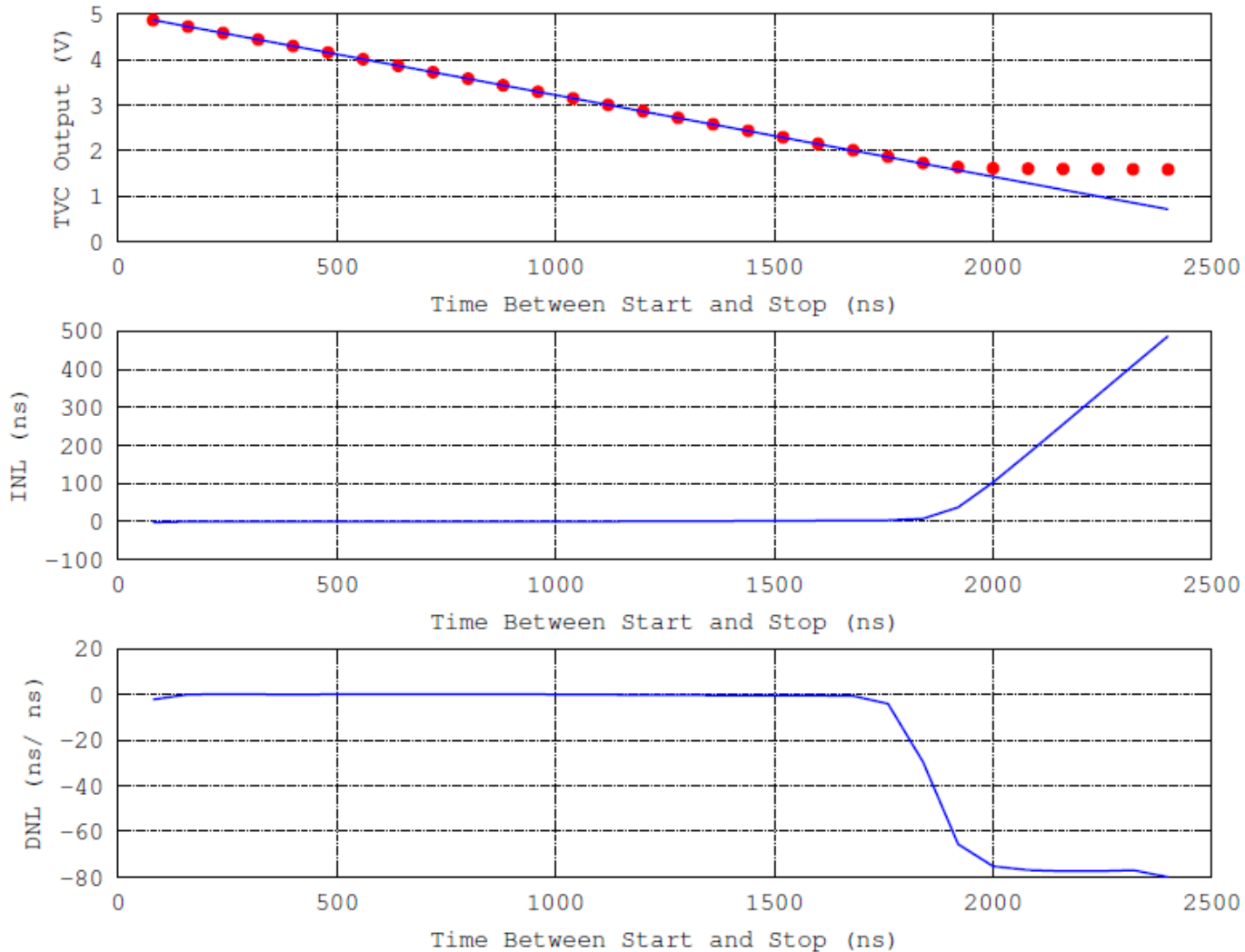
AFTER

# TVC Linearity (Typical, 250 ns Range)



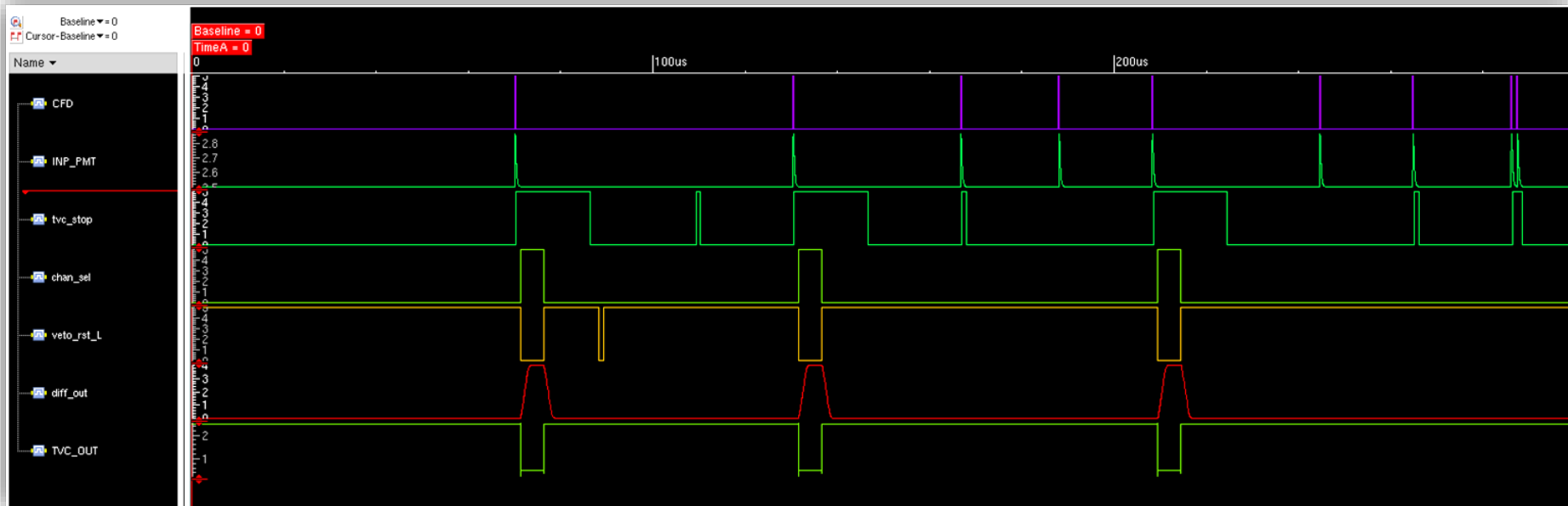
# TVC Linearity (Typical, 2000 ns Range)

Vdd = 5.0 V, Agnd = 2.5 V, Temp = 27.0 C, Corner = typ



# Functional Test on Single Channel

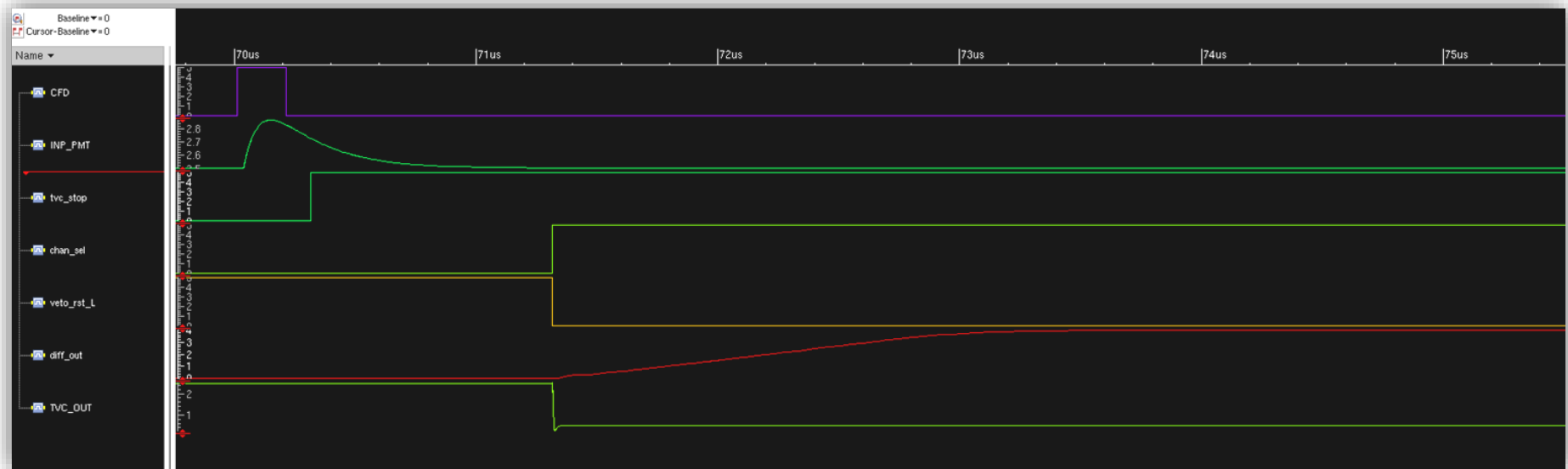
Simulation demonstrates that revised TVC functions correctly!



# Settling Time Behavior of Buffer

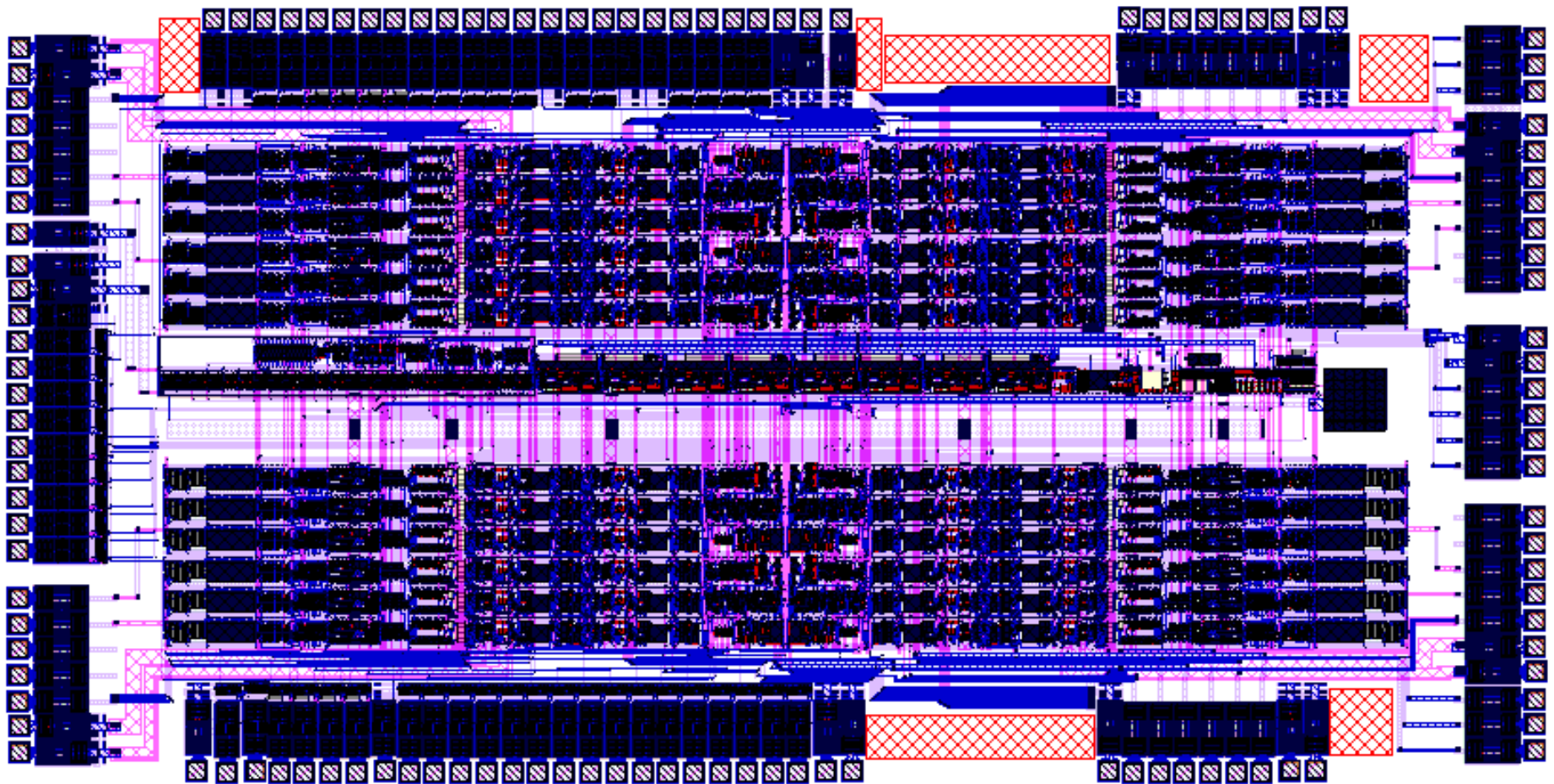
TVC starts on falling edge of CFD signal stops on rising edge of TVC\_STOP signal.

Observe that takes differential signal from output buffer about 4 usec to settle.

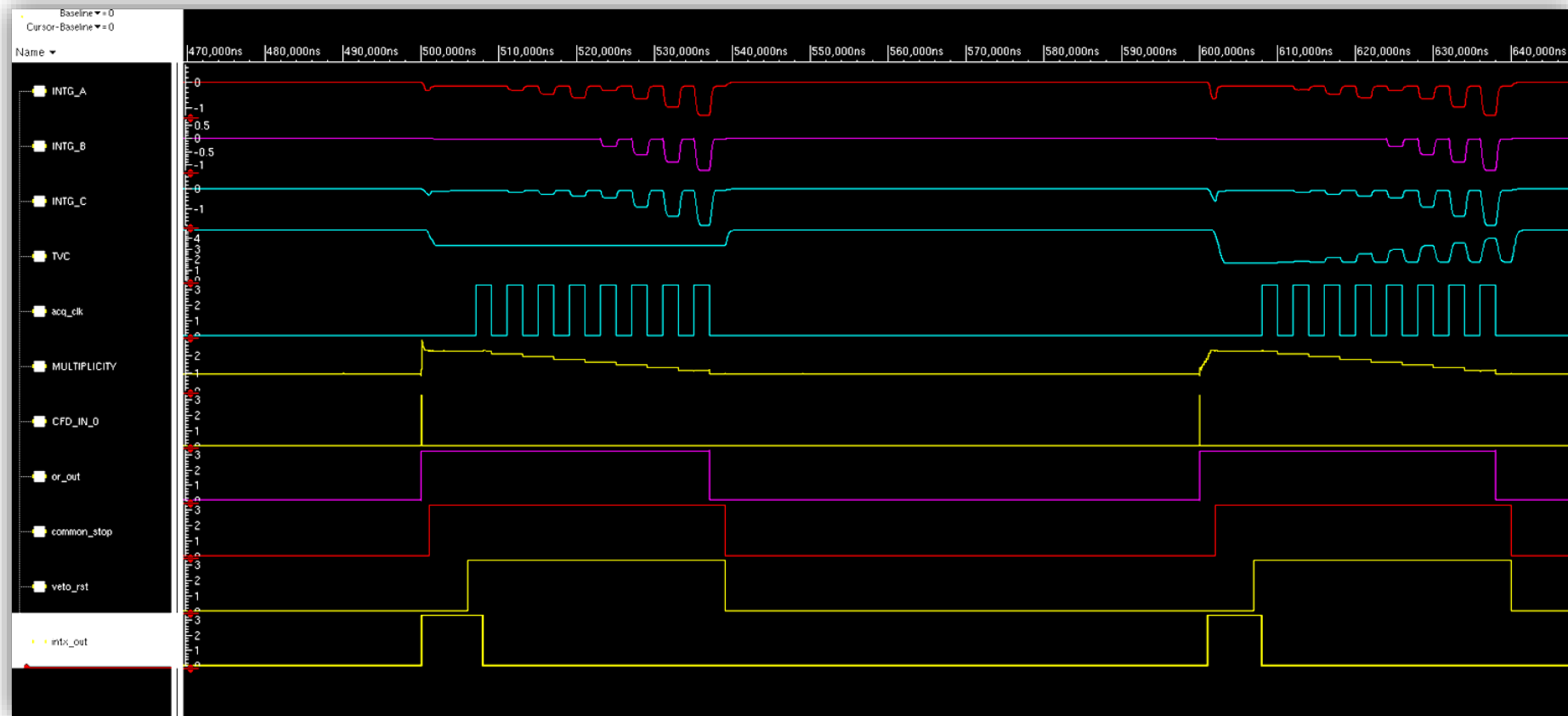




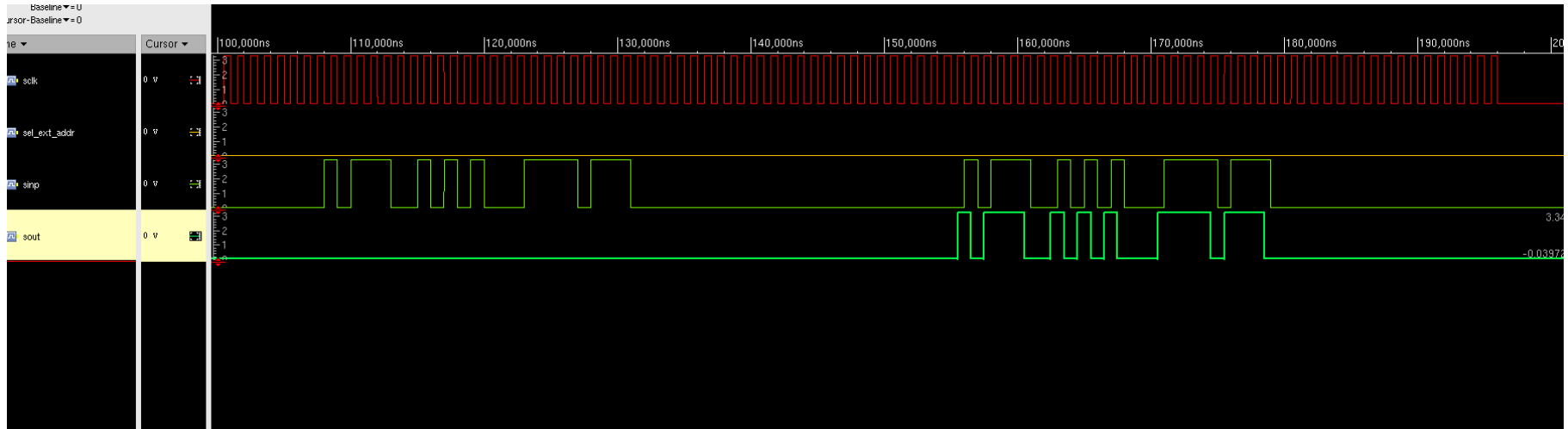
# PSD4 Final Layout (5.7 mm x 2.9 mm)



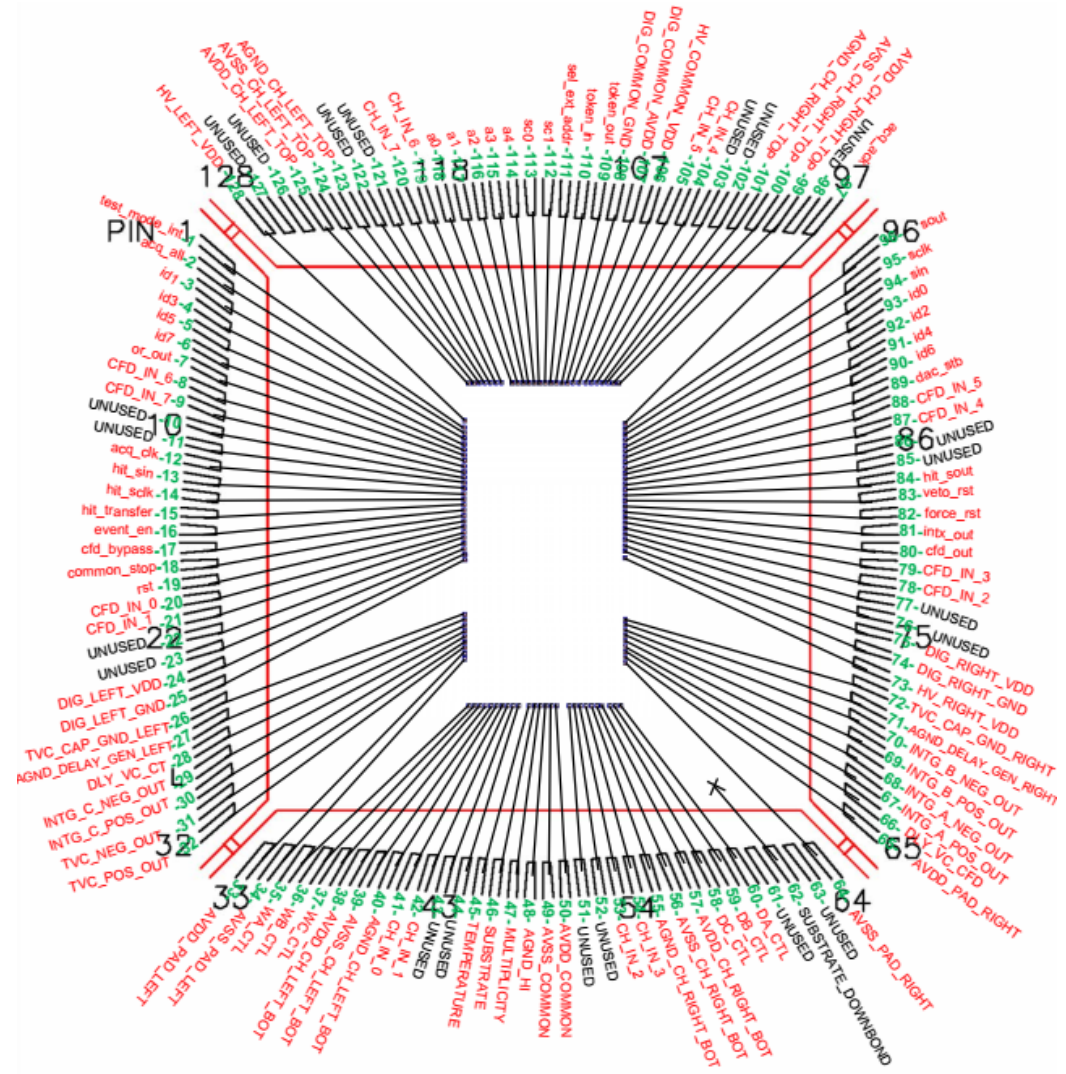
# Simulation With Extracted Netlist of Full Chip!!!



# Configuration Register Successfully Loaded!!!



# Bonding Diagram



# Summary

- PSD4 addresses issues with current PSD3
- Changes, while not trivial, are “safe”
- Scheduled for fabrication on Dec. 4, 2017
- Current plan is to purchase 160 packaged parts at a total cost of \$42,900!