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Preview of Award 1625499 - Annual Project Report

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Federal Agency and Organization Element to Which Report is Submitted:	4900
Federal Grant or Other Identifying Number Assigned by Agency:	1625499
Project Title:	MRI: Development of ASIC's Suite for Analog Processing of Signals from Large Arrays of Silicon-Strip Detectors and PSD-Capable Scintillators
PD/PI Name:	George L Engel, Principal Investigator
Recipient Organization:	Southern Illinois University at Edwardsville
Project/Grant Period:	02/01/2017 - 01/31/2020
Reporting Period:	02/01/2018 - 01/31/2019
Submitting Official (if other than PD\PI):	N/A
Submission Date:	N/A
Signature of Submitting Official (signature shall be submitted in accordance with agency specific instructions)	N/A

Accomplishments

*** What are the major goals of the project?**

The major goals of the project are to develop two multi-channel integrated circuits (ICs) for use in nuclear physics experiments. The two ICs are called PSD8C (Pulse Shape Discrimination - 8 Channel) and HINP16C (Heavy Ion Nuclear Physics - 16 Channel). The PSD8C chip provides particle identification and is generally used with scintillators while the HINP16C chip will have excellent energy resolution and high dynamic range. The chip will be used with silicon strip detectors.

The PSD8C is an improved version of an IC which was initially developed as part of an NSF-MRI about 10 years ago. The HINP16C is also an improved version (better performance and additional features) of an IC whose development dates back to around 2003. Existing versions of both ICs have been used successfully in numerous experiments to date. The improvements for both ICs are described in detail in the NSF-MRI proposal.

Another important, but perhaps not "major" goal, of the project is to design a third IC (christened CFD - **C**onstant **F**raction **D**iscriminator) which can be used as a companion chip to PSD8C and would make the PSD8C IC much easier to use. This third IC would replace a rather large board of electronics which is generally required when PSD8C is used. The purpose of the CFD chip is to create digital pulses which mark the arrival of the analog pulses at the input pins to the PSD chip. These CFD output signals serve as digital inputs to the PSD chip and are used to start the TVC circuits along with the integrator delay (delay before start of integration) circuits residing on the PSD chip.

It should be noted that the CFD chip circuits are **needed** by the HINP chip and therefore **must be developed before the HINP chip can be fabricated**. Therefore, while the CFD chip can be used in conjunction with the PSD chip to reduce PSD system complexity, it is foremost a *test* chip which allows us to validate the timing circuits which ultimately need be integrated onto the HINP chip. One of our **major** objectives of the MRI was to improve the CFD circuits on the HINP IC. Creation of the CFD chip is a major stepping stone along the road to improving the HINP chip!

*** What was accomplished under these goals (you must provide information for at least one of the 4 categories below)?**

Major Activities: In the first year of the project, my group worked on the PSD chip. During the past year, we turned our attentions to the design of the CFD and HINP chips. The CFD chip was developed first because its circuits are needed on the larger and more complex HINP chip. As stated above while the CFD chip has use as a companion chip to the PSD chip, the primary reason for fabricating the CFD chip is to test out the critical timing circuits that must be integrated onto the larger, more complex, and more expensive HINP chip. Our plan is to test the CFD chip before submitting the HINP chip so that any necessary changes can be made to the CFD circuits before they are fabricated as part of the HINP chip.

Specific Objectives: Our specific objectives during the past year were to

1.) Test the PSD chip which went in for fabrication in Dec 2017 and came back from fabrication in May 2018.

2.) Design the CFD (Constrant Fraction Discriminator) circuitry which is a major block in the design of the HINP chip. The CFD circuitry is responsible for producing a digital output pulse that marks the onset of an analog input signal. The digital output pulse must occur at he same time regardless of the amplitude of the analog input pulse. Moreover, the digital timing pulse must possess excellent walk and jitter characteristics. These circuits must eventually be integrated onto the HINP chip.

3.) Develop the other circuits (linear branch) which are integral to HINP chip operation.

4.) Assemble the CFD circuits into a stand-alone chip. The stand-alone chip's primary purpose is to test the performance of the critical circuits which constitute the timing branch of the HINP chip. However, if completely successful, this CFD test chip could be used in conjunction with the PSD chip, thereby simplifying our existing PSD systems.

5.) Submit the CFD chip for fabrication. If the CFD chip is completely successful then it will be used in conjunction with the PSD chip to reduce system size and complexity. Regardless, the CFD chip will be used to validate the timing circuitry which ultimately must reside on the HINP chip. Once again, the CFD chip should be viewed as a chip which foremost tests critical HINP circuits before integrating them into the overall HINP design. The circuits on the CFD chip comprise approximately one-half of the silicon area of the HINP chip. It is literally a "cut and paste" operation. Being able to verify these critical circuits before having to use them in the HINP design will greatly improve the odds of a fully functional HINP chip coming back from the fabrication facility later this year!

Significant Results: The PSD chip was successfully modified and submitted for fabrication in December 2017. The chips arrived at our lab in May 2018 and were then delivered to the Nuclear Reactions Group at Washington University led by Dr. Lee Sobotka. The chips were tested and were determined to work correctly!

The CFD chip was designed, simulated, and physically layed out. The chip was submitted for fabrication on December 10, 2018. We are hopeful that it will come back from fabrication sometime in May of 2019. The CFD chip will then be tested. Based on the results of testing, we will make any necessary modifications to the CFD circuits before submitting the HINP chip for fabrication.

Much of the electrical design of the HINP chip has been completed. There is still a lot of physical layout and verification which must be completed before the IC can be submitted for fabrication.

Key outcomes or Other achievements:

*** What opportunities for training and professional development has the project provided?**

The MRI has provided many opportunities for training several graduate students. Seven students worked on the project during year one of the grant and additional students were involved in the design process during this past year. The students who worked on the project during year two of the grant were Pratharna Jani (MSEE May 2018), Sneha Edula (MSEE May 2018), Bryan Orabutt (MSEE August 2018), Monjur Rafi (MSEE December 2018), Sai Geetha Allipuram (MSEE expected May 2019), Lakshmi Teja Vipparla (MSEE expected May 2019), Anil Korkmaz (MSEE expected May 2019), and Jayasurya Burla (MSEEE expected August 2019).

Orabutt (Aug. 2018), Korkmaz (May 2019), Allipuram (May 2019), and Burla (Aug. 2018) are all writing Master's Theses which describe different aspects of the IC development funded by this NSF-MRI grant.

These graduate students performed a wide variety of tasks which are part of the development cycle of a mixed-signal ASIC (Application Specific Integrated Circuit). These tasks include

1.) System-level design

2.) Circuit-level design

3.) Electrical simulation

4.) Physical layout

5.) Physical verification (LVS i.e. Layout Versus Schematic and DRC i.e. Design Rule Checks)

6.) Parasitic extraction (PEX)

7.) Testbench creation using SystemVerilog and VerilogA

8.) Verification/interpretation of simulations results using MATLAB

The opportunity to work on an IC as a graduate student greatly improves a student's skill set and provides that student with a deeper understanding of the design flow required to produce a complex micro-chip. Pratharna Jani now works for Bausch and Lomb. Bryan Orabutt begins working (January 2019) on a doctoral degree in Computer Engineering at Washington University and will continue to be involved in the MRI project as a doctoral student.

The MRI has indirectly helped several other graduate students who did not directly work on the project since I routinely use circuits from the ICs described in this report in the graduate level IC courses that I teach here in the Electrical and Computer Engineering Department.

*** How have the results been disseminated to communities of interest?**

A poster is in prepartion as well as a paper. The poster wil be presented at a conference in February. We are also posting information about the ICs to our website.

*** What do you plan to do during the next reporting period to accomplish the goals?**

We plan to test the CFD chip when it comes back from fabrication. We also plan to complete the development of the HINP chip and submit it for fabrication before the end of 2019. Most of the design needed in the HINP IC is complete but much

more simulation and physical layout and verification is required before the HINP chip can be submitted for fabrication. Testing of the CFD chip may dictate that changes be made to the HINP design before submitting it for fabrication.

Supporting Files

Filename	Description	Uploaded By	Uploaded On
borabut_defense.pdf	PDF which describes the CFD chip. Based on powepoint presentation used at Bryan Orabutt's Masters Defense.	George Engel	01/12/2019

Products

Books

Book Chapters

Inventions

Journals or Juried Conference Papers

Licenses

Other Conference Presentations / Papers

Other Products

Other Publications

Patents

Technologies or Techniques

Thesis/Dissertations

Bryan Orabutt. *Design and Analysis of a Multi-Channel Discriminator Integrated Circuit for Use in Nuclear Physics Experiments*. (2018). Southern Illinois University Edwardsville. Acknowledgement of Federal Support = Yes

Websites

Development of ASICs for Radiation Detection and Monitoring
http://www.siue.edu/~gengel/NSF-MRI.htm

Website devoted to posting material related to the work funded by this NSF-MRI.

Supporting Files

Filename	Description	Uploaded By	Uploaded On
Orabutt_Thesis.pdf	Bryan Orabutt Masters Thesis describing CFD circuits.	George Engel	01/16/2019

Participants/Organizations

What individuals have worked on the project?

Name	Most Senior Project Role	Nearest Person Month Worked
Engel, George	PD/PI	3

Name	Most Senior Project Role	Nearest Person Month Worked
Allipuram, Sai Geetha	Graduate Student (research assistant)	3
Burla, Jayasurya	Graduate Student (research assistant)	1
Edula, Sneha	Graduate Student (research assistant)	1
Jani, Prarthana	Graduate Student (research assistant)	1
Korkmaz, Anil	Graduate Student (research assistant)	6
Orabutt, Bryan	Graduate Student (research assistant)	4
Rafi, Monjur	Graduate Student (research assistant)	1
Vipparla, Lakshmi	Graduate Student (research assistant)	1

Full details of individuals who have worked on the project:

George L Engel
Email: gengel@siue.edu
Most Senior Project Role: PD/PI
Nearest Person Month Worked: 3

Contribution to the Project: Supervised graduate students and worked closely with students on the electrical design of the circuits used in the ICs that we are developing.

Funding Support: NONE

International Collaboration: No
International Travel: No

Sai Geetha Allipuram
Email: sallipu@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 3

Contribution to the Project: Wrote verilog descriptions of digital configuration and readout circuits. Created system verilog testbench to verify correctness of design. Later synthesized and placed and routed design using the Cadence EDI tools.

Funding Support: NONE

International Collaboration: No
International Travel: No

Jayasurya Burla
Email: jburla@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Performed physical layout for several CFD circuits. Also responsible for LVS and DRC of circuits. Used space based router for chip level assembly.

Funding Support: NONE

International Collaboration: No
International Travel: No

Sneha Edula
Email: sedula@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Designed, simulated, layed out, and verified the one-shot circuit used in CFD chip.

Funding Support: NONE

International Collaboration: No
International Travel: No

Prarthana Jani
Email: pjani@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Student designed circuits, ran simulations, and performed physical layout for digital-to-analog converter used in the CFD chip. Student also used MATLAB to quantify performance.

Funding Support: NONE

International Collaboration: No
International Travel: No

Anil Korkmaz
Email: akorma@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 6

Contribution to the Project: Designed, simulated, and layed out a wide variety of circuits for both CFD and HINP ICs. Student is designing the linear branch of the HINP chip.

Funding Support: NONE

International Collaboration: No
International Travel: No

Bryan Orabutt
Email: borabut@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 4

Contribution to the Project: Performed system level design, schematic entry, circuit level design, and wrote verilogA / SystemVerilog testbenches for system verification. He is, in large part, the student most responsible for the successful completion of the CFD chip.

Funding Support: NONE

International Collaboration: No
International Travel: No

Monjur Rafi
Email: mrafi@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Simulated, layed out, and verified the shaper circuit used in HINP chip.

Funding Support: NONE

International Collaboration: No
International Travel: No

Lakshmi Teja Vipparla
Email: lvippar@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Performed physical layout of several CFD chip circuits. Also responsible for DRC and LVS verifcation of those circuits.

Funding Support: NONE

International Collaboration: No
International Travel: No

What other organizations have been involved as partners?

Name	Type of Partner Organization	Location
Washington University	Academic Institution	St. Louis MO

Full details of organizations that have been involved as partners:

Washington University

Organization Type: Academic Institution
Organization Location: St. Louis MO

Partner's Contribution to the Project:
Collaborative Research

More Detail on Partner and Contribution: We work closely with the Nuclear Reactions Group from Washington University headed by Lee Sobotka. The ICs will ultimately be first used by his group. Their electronics expert, Jon Elson, is of great help to us. The success of our work has always been largely due to the close collaboration that my IC Design Group has has with the actual users of the ICs.

What other collaborators or contacts have been involved?
Nothing to report

Impacts

What is the impact on the development of the principal discipline(s) of the project?

Nothing to report.

What is the impact on other disciplines?

The integrated circuits that we are developing will provide improved instrumentation for a wide range of nuclear physics experiments where the detection / monitoring of ionizing radiation is required.

What is the impact on the development of human resources?

The project has given several graduate students over the past year an opportunity to work on a complex integrated circuit. The experience they gained over the past year will be of immense help to them when they enter the IC design field. Students benefit greatly by being involved in these types of real-world research projects.

What is the impact on physical resources that form infrastructure?
Nothing to report.

What is the impact on institutional resources that form infrastructure?
Nothing to report.

What is the impact on information resources that form infrastructure?
Nothing to report.

What is the impact on technology transfer?
Nothing to report.

What is the impact on society beyond science and technology?
Nothing to report.

Changes/Problems

Changes in approach and reason for change
Nothing to report.

Actual or Anticipated problems or delays and actions or plans to resolve them

We requested and received a **1 year no-cost extension.**

In this section I will briefly describe the reasons why I requested a 1-year extension.

In the proposal to NSF, we sought funding to modify, improve, and fabricate two existing micro-chips, one (referred to as PSD) for use with scintillators and one for use with Si-Strip detectors (christened HINP). The original micro-chip designs were executed using the ON Semiconductor 0.5 micron process and submitted through the U.S. wafer sharing company, MOSIS. I am pleased to report that the enhanced PSD chip, as described in the proposal, was submitted for fabrication (November 2017), returned from fabrication, and works well!

Unfortunately, in late Spring 2017, MOSIS informed us that they were essentially phasing out the ON 0.5 micron process. After considerable thought and after consulting the end-users of the chips (Washington University in St. Louis, Lee Sobotka), a decision was made to completely re-design our HINP micro-chip using a more modern process (Austrian Microsystems 0.35 micron). The re-design was started in November 2017.

Because of the complete redesign we decided that it was important to fabricate the Constant Fraction Discriminators (CFDs) circuits since they constitute the most complex part of HINP. This new micro-chip is called CFD and is discussed in the original proposal to NSF. While allowing us to test important circuitry that **must** be integrated into HINP, the CFD micro-chip will also be used with the aforementioned PSD chip to reduce overall instrument size and complexity. The CFD micro-chip was successfully submitted for fabrication on December 10, 2018.

On submitting the CFD design, however, we received some devastating news from MOSIS. They have made a decision to **no longer offer the AMS 0.35 micron process**, effective immediately. They gave us no advanced warning. Our plan was to integrate the CFD circuits (about ½ of HINP) along with many other circuits (the other ½ of HINP) which are nearing

completion into our new HINP design. Our plan was to test the CFD chip once it came back from fabrication, make any necessary changes to the HINP design based on CFD testing, and then fabricate HINP through MOSIS. Even this plan would have required a 6 month no-cost extension, but since we can no longer fab through MOSIS, we requested a 1-year extension.

We are currently investigating other wafer sharing companies (alternatives to MOSIS). Two companies have been identified, one in France and one in Belgium. We have already determined from their websites that they have AMS runs scheduled throughout 2019. We are hoping that we will be able to fabricate HINP through one of these two companies. Pricing (based on limited information from website) is comparable to MOSIS prices. Starting over, once again, in another MOSIS supported process is really not a viable option at this point. We are still optimistic that we can successfully fabricate the HINP chip as described in the original proposal.

Changes that have a significant impact on expenditures
Nothing to report.

Significant changes in use or care of human subjects
Nothing to report.

Significant changes in use or care of vertebrate animals
Nothing to report.

Significant changes in use or care of biohazards
Nothing to report.

Special Requirements

Responses to any special reporting requirements specified in the award terms and conditions, as well as any award specific reporting requirements.
Nothing to report.