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Federal Agency and Organization Element to Which Report is Submitted:	4900
Federal Grant or Other Identifying Number Assigned by Agency:	1625499
Project Title:	MRI: Development of ASIC's Suite for Analog Processing of Signals from Large Arrays of Silicon-Strip Detectors and PSD-Capable Scintillators
PD/PI Name:	George L Engel, Principal Investigator
Recipient Organization:	Southern Illinois University at Edwardsville
Project/Grant Period:	02/01/2017 - 01/31/2019
Reporting Period:	02/01/2017 - 01/31/2018
Submitting Official (if other than PD\PI):	N/A
Submission Date:	N/A
Signature of Submitting Official (signature shall be submitted in accordance with agency specific instructions)	N/A

Accomplishments

*** What are the major goals of the project?**

The major goals of the project are to develop two multi-channel integrated circuits for use in nuclear physics experiments. The two ICs are called PSD8C (Pulse Shape Discrimination - 8 Channel) and HINP16C (Heavy Ion Nuclear Physics - 16 Channel). The PSD8C provides particle identification and is generally used with scintillators while the HINP16 chip has excellent resolution and high dynamic range and is used with silicon strip detectors.

The PSD8C is an improved version of an IC which was initially developed as part of an MRI about 10 years ago. The HINP16C is also an improved version (better performance and additiaonal features) of an IC whose development dates back to around 2003. Existing versions of both ICs have been used successfully in numerous experiments to date. The improvements for both ICs are described in detail in the NSF-MRI proposal. The specific changes made to the PSD8C IC will be described in the following section of this report.

Another important, but perhaps not "major" goal, of the project is to assess the feasibilty of a third IC (christened CFD - Constant Fraction Discriminator) which would be a companion chip to PSD8C and would make the PSD8C IC much easier to use. This third IC would replace a rather large board of electronics which is generally required when PSD8C is used. The purpose of the CFD chip is to create digital pulses which that mark the arrival of the analog pulses to the PSD chip. These digital CFD inputs to the PSD chip are used to start the TVC circuits and the integrator delay (delay before start of integration) circuits residing on the PSD chip.

*** What was accomplished under these goals (you must provide information for at least one of the 4 categories below)?**

Major Activities:

Work on making the modifications (described in the following sub-section) to the PSD8C IC started soon after the start date for the grant. The majority of my group's efforts early on were directed towards modifiying PSD8C.

After submitting PSD8C for fabrication in November, we have turned our attention to the HINP16C IC. Several modifications to the HINP16C IC have been made. Before additional modification to the IC can be made, a series of electrical tests will need to be be performed. In order for these tests to be made, a test system needs to be developed and we are currently working on the development of this system.

The testbed (with some rather small changes) under developement will also allow us to perform electrical tests on the PSD8C IC when it returns from fabrication. The purpose of the testbed is to make it easier to make purely electrical tests on the ICs.

Specific Objectives:

Here is a summary list of modifications made to the PSD8C IC. (These modifications/enhancements are described in additional detail in a PDF which is included as part of this report.)

1. **We added level translators to the chip's digital pads** to make the IC compatible with modern FPGAs (3.3 Volt external logic levels) which we use to control and configure the PSD8C. With past generations of our ICs, this task was accomplished with commmercial ICs **external** to our chips. The addition of the level translators the PSD8C itself greatly simplifies the PCB layout and assembly of the printed-circuit boards upon which PSD8C chips reside.
2. Analog signals (4 differential pairs i.e. 3 integral and one time-to-voltage output) are generated by the PSD8C IC which are then converted to a digital representation by off-chip ADCs. In oder to use the entire range of the off-chip ADC, one needs to "swap" the inverting and non-inveting outputs for the three integral outputs depending on whether the input pulse to the IC is of positive or negative polarity, **The ability to "swap" the differential outputs was added to the PSD8C IC.** In earlier versions of our PSD chip, this swapping is done by the off-chip ADC. Unfortunately, there is only one commercially availabe ADC (Linear Technologies LTC1865 16-bit ADC) which has this feature and can meet our other specifications. The addition of on-chip "swapping" capability give the designer of the PSD chip board much greater latitude in selecting an ADC.
3. The time-to-voltage converter (TVC) on previous generations of the PSD chip has two full-scale ranges which the user could choose from. Those ranges were: 500 ns and 200 nsec. The resolution in the 500 nsec mode was measured at around 270 ps while the resolution (FWHM) in the 2000 ns mode was 825 ps. In both cases the TVC circuit starts on the rising edge of the CFD (Constant Fraction Discriminator) input for the channe. **Modifications were made to the PSD IC in order to improve the time resolution of the IC. The 500 ns TVC range was changed to 250 ns.** Simulations and analysis suggest that the resolution will improve to the 150 ps level. With such a short range it was necessary to delay the start of the TVC. In this newest generation IC, the TVC will start on the falling edge of the CFD circuit and the delay will be controlled by altering the width of the CFD signal.

Significant Results:

The PSD8C IC was successully modified and submitted for fabrication. Specifically, the IC was submitted to the ON Semiconductor 0.5 micron C5 process via MOSIS for

inclusion in the Dec. 4, 2017 run. The current status of the IC (as of Jan 5, 2017) is that it is a "candidate for fabrication" but is not currently in fab at the time of the writing of this report. We expect the IC to go out from MOSIS to the fab in the near future.

Key outcomes or Other achievements:

*** What opportunities for training and professional development has the project provided?**

The MRI has provided many opportunites for training and professional development for several graduates students. These students (to date) include: Po Wang (received MSEE May 2017). Turki Alnefaie (received MSEE December 2017), Ravi Chappidi (received his MSEE August 2017) Pratharna Jani (will receive MSEE May 2018), Sneha Edula (will receive MSEE May 2017), Byran Orabutt (will receive MSEE May 2018), and Monjur Rafi.

These graduate students have been performing a wide variety of tasks which are part of the development cycle of a mixed-signal ASIC (Application Specific IC). These tasks include

1. System-level design
2. Circuit design
3. Electrical simulation
4. Physical layout
5. Physical verification (LVS and DRC)
6. Testbench creation using both SystemVerilog and VerilogA languages
7. Verification of simulation results using MATLAB
8. Printed circuit board layout

Perhaps, an unsolicited email which I received recently from one of the students who worked on the project best exemplifies the value of MRIs to students.

>>>

Dr. Engel,
I hope my email find you well and happy new year. I don't know how to start but this experience that I had through with you gave me a good knowledge and a lot of things that improved my skills. All I want say to you is Thank you so much for the time that I spent with you to learn something new. I hope the best for your life. Yeah and I hope the PSD chip works well. :)

Kindest regards,Turki.

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The opportunity to work on an IC as a graduate student greaty improves a stduent's skill set and provides that student with a good understanding of the design flow required to produce an IC. It greatly improves a student's ability to find a job in the IC industry after graduation. As an example, I just recently learnded that one of the students, Ravi Chappidi, who worked on the project has been hired by Qualcomm (an IC company located in San Diego, CA).

The MRI has indirectly helped several other students who did not directly work on the project since I have been using circuits from our ICs as case studies in the graduate level IC courses which I teach here in the Department.

*** How have the results been disseminated to communities of interest?**

While formal papers will be authored in the future, our current methos of dissemination of our results to date has bee a powerpoint presentation which has been included as part of this report. The results have been shared with the nuclear reactions group (headed by Dr. Lee Sobotka) at Washington University.

*** What do you plan to do during the next reporting period to accomplish the goals?**

We plan to test and integrate the PSD8C chips into systems which can be used in experiments. We also plan to complete modifications to the HINP16C IC and submit it for fabrication and to continue to study the feasibility of a third IC (CFD) which would make it much easier for groups to use the PSD8C IC.

Supporting Files

Filename	Description	Uploaded By	Uploaded On
PSDchipRev4_NSF_Report.pdf	PDF which describes changes made to PSD8C IC in greater detail.	George Engel	01/06/2018

Products

Books
Nothing to report.

Book Chapters
Nothing to report.

Inventions
Nothing to report.

Journals or Juried Conference Papers
Nothing to report.

Licenses
Nothing to report.

Other Conference Presentations / Papers
Nothing to report.

Other Products
Nothing to report.

Other Publications
Nothing to report.

Patents
Nothing to report.

Technologies or Techniques
Nothing to report.

Thesis/Dissertations
Nothing to report.

Websites
Nothing to report.

Participants/Organizations

What individuals have worked on the project?

Name	Most Senior Project Role	Nearest Person Month Worked
Engel, George	PD/PI	3
Alnefaie, Turki	Graduate Student (research assistant)	2
Chappidi, Ravi	Graduate Student (research assistant)	0

Name	Most Senior Project Role	Nearest Person Month Worked
Edula, Sneha	Graduate Student (research assistant)	1
Jani, Prarthana	Graduate Student (research assistant)	4
Orabutt, Bryan	Graduate Student (research assistant)	4
Rafi, Monjur	Graduate Student (research assistant)	1
Wang, Po	Graduate Student (research assistant)	1

Full details of individuals who have worked on the project:

George L Engel
Email: gengel@siue.edu
Most Senior Project Role: PD/PI
Nearest Person Month Worked: 3

Contribution to the Project: Supervised graduate students and work closely with students on the electrical design of the ICs.

Funding Support: NONE

International Collaboration: No
International Travel: No

Turki Alnefaie
Email: talnefa@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 2

Contribution to the Project: Student worked on several design changes to PSD8C. He performed physical layout, physical verification, simulation, and performance characterization.

Funding Support: Student was not funded by MRI. He had a fellowship from his native country of Saudi Arabia.

International Collaboration: No
International Travel: No

Ravi Sai Chappidi
Email: schappi@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 0

Contribution to the Project: Performed circuit design, simulation, physical layout, and physical verification tasks

Funding Support: NONE

International Collaboration: No
International Travel: No

Sneha Edula
Email: sedula@siue.edu

Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Helped with physical layout, DRC, and LVS checks on PSD8C and HINP16C chip.

Funding Support: Funded as a teaching assistant for the ECE department,

International Collaboration: No
International Travel: No

Prarthana Jani
Email: pjani@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 4

Contribution to the Project: Student designed circuits, ran simulations, and performed physical layout of several circuits for both PSD8C and HINP16C.

Funding Support: NONE

International Collaboration: No
International Travel: No

Bryan Orabutt
Email: borabut@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 4

Contribution to the Project: Performed system level design, schematic entry, circuit level design, testbench creation, and wrote verilogA / SystemVerilog descriptions. Works on assessing the feasibiltiy of CFD chip. Working on Masters Thesis reporting on feasibility of IC.

Funding Support: NONE

International Collaboration: No
International Travel: No

Monjur Rafi
Email: mrafi@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Working on the testbed for HINP16C IC.

Funding Support: Also funded by Department as a teaching assistant.

International Collaboration: No
International Travel: No

Po Wang
Email: pwang@siue.edu
Most Senior Project Role: Graduate Student (research assistant)
Nearest Person Month Worked: 1

Contribution to the Project: Performed electrical design Ran electrical simulations Wrote VerilogA code Performed physical layout

Funding Support: NONE

International Collaboration: No
International Travel: No

What other organizations have been involved as partners?

Name	Type of Partner Organization	Location
Washington University	Academic Institution	St. Louis MO

Full details of organizations that have been involved as partners:

Washington University

Organization Type: Academic Institution
Organization Location: St. Louis MO

Partner's Contribution to the Project:
Collaborative Research

More Detail on Partner and Contribution: We work closely with the Nuclear Reactions Group from Washington University headed by Lee Sobotka. The ICs will ultimately be first used by his group. Their electronics expert, Jon Elson, is of great help to us. The success of our work has always been largely due to the close collaboration that my IC Design Group has has with the actual users of the ICs.

What other collaborators or contacts have been involved?
Nothing to report

Impacts

What is the impact on the development of the principal discipline(s) of the project?
Nothing to report.

What is the impact on other disciplines?

The ICs we are developing will provide improve instrumentation for a wide range of nuclear physics experiments where the detection / monitoring of ionizng radiation is required.

What is the impact on the development of human resources?
Nothing to report.

What is the impact on physical resources that form infrastructure?
Nothing to report.

What is the impact on institutional resources that form infrastructure?
Nothing to report.

What is the impact on information resources that form infrastructure?
Nothing to report.

What is the impact on technology transfer?
Nothing to report.

What is the impact on society beyond science and technology?

Nothing to report.

Changes/Problems

Changes in approach and reason for change
Nothing to report.

Actual or Anticipated problems or delays and actions or plans to resolve them
Nothing to report.

Changes that have a significant impact on expenditures
Nothing to report.

Significant changes in use or care of human subjects
Nothing to report.

Significant changes in use or care of vertebrate animals
Nothing to report.

Significant changes in use or care of biohazards
Nothing to report.

Special Requirements

Responses to any special reporting requirements specified in the award terms and conditions, as well as any award specific reporting requirements.
Nothing to report.