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COVER SHEET FOR PROPOSAL TO THE NATIONAL SCIENCE FOUNDATION

PROGRAM ANNOUNCEMENT/SOLICITATION NO./DUE DATE
NSF 15-504 **01/13/16**

☐ Special Exception to Deadline Date Policy

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1625499

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Edwardsville, IL. 620250001

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TITLE OF PROPOSED PROJECT **MRI: Development of ASIC's Suite for Analog Processing of Signals from Large Arrays of Silicon-Strip Detectors and PSD-Capable Scintillators**

REQUESTED AMOUNT	PROPOSED DURATION (1-60 MONTHS)	REQUESTED STARTING DATE	SHOW RELATED PRELIMINARY PROPOSAL NO. IF APPLICABLE
$ **204,565**	**24** months	**08/01/16**	

THIS PROPOSAL INCLUDES ANY OF THE ITEMS LISTED BELOW
☐ BEGINNING INVESTIGATOR (GPG I.G.2)
☐ DISCLOSURE OF LOBBYING ACTIVITIES (GPG II.C.1.e)
☐ PROPRIETARY & PRIVILEGED INFORMATION (GPG I.D, II.C.1.d)
☐ HISTORIC PLACES (GPG II.C.2.j)
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PHS Animal Welfare Assurance Number _____
☒ FUNDING MECHANISM **Research - other than RAPID or EAGER**

☐ HUMAN SUBJECTS (GPG II.D.7) Human Subjects Assurance Number _____
Exemption Subsection _____ or IRB App. Date _____
☐ INTERNATIONAL ACTIVITIES: COUNTRY/COUNTRIES INVOLVED (GPG II.C.2.j)

☒ COLLABORATIVE STATUS
Not a collaborative proposal

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CO-PI/PD				
CO-PI/PD				
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CERTIFICATION PAGE

Certification for Authorized Organizational Representative (or Equivalent) or Individual Applicant

By electronically signing and submitting this proposal, the Authorized Organizational Representative (AOR) or Individual Applicant is: (1) certifying that statements made herein are true and complete to the best of his/her knowledge; and (2) agreeing to accept the obligation to comply with NSF award terms and conditions if an award is made as a result of this application. Further, the applicant is hereby providing certifications regarding conflict of interest (when applicable), drug-free workplace, debarment and suspension, lobbying activities (see below), nondiscrimination, flood hazard insurance (when applicable), responsible conduct of research, organizational support, Federal tax obligations, unpaid Federal tax liability, and criminal convictions as set forth in the NSF Proposal & Award Policies & Procedures Guide,Part I: the Grant Proposal Guide (GPG). Willful provision of false information in this application and its supporting documents or in reports required under an ensuing award is a criminal offense (U.S. Code, Title 18, Section 1001).

Certification Regarding Conflict of Interest

The AOR is required to complete certifications stating that the organization has implemented and is enforcing a written policy on conflicts of interest (COI), consistent with the provisions of AAG Chapter IV.A.; that, to the best of his/her knowledge, all financial disclosures required by the conflict of interest policy were made; and that conflicts of interest, if any, were, or prior to the organization's expenditure of any funds under the award, will be, satisfactorily managed, reduced or eliminated in accordance with the organization's conflict of interest policy. Conflicts that cannot be satisfactorily managed, reduced or eliminated and research that proceeds without the imposition of conditions or restrictions when a conflict of interest exists, must be disclosed to NSF via use of the Notifications and Requests Module in FastLane.

Drug Free Work Place Certification

By electronically signing the Certification Pages, the Authorized Organizational Representative (or equivalent), is providing the Drug Free Work Place Certification contained in Exhibit II-3 of the Grant Proposal Guide.

Debarment and Suspension Certification

(If answer "yes", please provide explanation.)

Is the organization or its principals presently debarred, suspended, proposed for debarment, declared ineligible, or voluntarily excluded from covered transactions by any Federal department or agency? Yes ☐ No ☒

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This certification is required for an award of a Federal contract, grant, or cooperative agreement exceeding $100,000 and for an award of a Federal loan or a commitment providing for the United States to insure or guarantee a loan exceeding $150,000.

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The undersigned certifies, to the best of his or her knowledge and belief, that:
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Two sections of the National Flood Insurance Act of 1968 (42 USC §4012a and §4106) bar Federal agencies from giving financial assistance for acquisition or construction purposes in any area identified by the Federal Emergency Management Agency (FEMA) as having special flood hazards unless the:
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CERTIFICATION PAGE - CONTINUED

Certification Regarding Organizational Support

By electronically signing the Certification Pages, the Authorized Organizational Representative (or equivalent) is certifying that there is organizational support for the proposal as required by Section 526 of the America COMPETES Reauthorization Act of 2010. This support extends to the portion of the proposal developed to satisfy the Broader Impacts Review Criterion as well as the Intellectual Merit Review Criterion, and any additional review criteria specified in the solicitation. Organizational support will be made available, as described in the proposal, in order to address the broader impacts and intellectual merit activities to be undertaken.

Certification Regarding Federal Tax Obligations

When the proposal exceeds $5,000,000, the Authorized Organizational Representative (or equivalent) is required to complete the following certification regarding Federal tax obligations. By electronically signing the Certification pages, the Authorized Organizational Representative is certifying that, to the best of their knowledge and belief, the proposing organization:
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Certification Dual Use Research of Concern

By electronically signing the certification pages, the Authorized Organizational Representative is certifying that the organization will be or is in compliance with all aspects of the United States Government Policy for Institutional Oversight of Life Sciences Dual Use Research of Concern.

AUTHORIZED ORGANIZATIONAL REPRESENTATIVE	SIGNATURE	DATE
NAME **Jerry Weinberg**	**Electronic Signature**	**Jan 13 2016 11:48AM**

TELEPHONE NUMBER	EMAIL ADDRESS	FAX NUMBER
618-650-3018	**jweinbe@siue.edu**	**618-650-2555**

PROJECT SUMMARY

Overview:

This proposal seeks to exercise the only ASIC (Application Specific Integrated Circuit) program in the US dedicated to, and tightly integrated with, low and intermediate energy nuclear physics in an effort to facilitate the fielding, in a cost effective manner, large arrays of Si-strip detectors and scintillators. Three chips will be produced.

A. ASIC for Silicon strip detectors (HINP series).
This chip will provide an unrivaled dynamic range (200 keV to 400 MeV) but also be extendable by allowing external charge-sensitive preamplifiers to be used. This combines the functionality of two chips we have previously designed. This one chip then can be used in almost any Si-strip application.

B. ASIC for scintillators with Pulse Shape Discrimination capability (PSD series).
We previously had a small production run of an 8-channel chip that provides (for each channel) the charge from three user specified integration regions and a charge proportional to the time difference between each channel and an externally supplied reference signal. All of the chips from our prior production run are in use by PSD-scintillator-array projects. Producing more of these chips (with only minor modifications) will allow for expansion of two existing projects and another we envision to exploit a new generation of PSD capable scintillators.

C. ASIC for CFD (new CFD series)
The HINP series has a Constant-Fraction Discriminator embedded in it. Our last version of this chip greatly improved the circuit over the one in common use (in HINPc). Many projects (one is described below) could make use of a low-power, compact stand-alone CFD chip. Modifying the CFD from our current HINP by adding a variable delay range, is the third proposed ASIC.

Intellectual Merit :

Use of these chips will allow for the extension of studies of the near continuum structure of light proton-rich nuclei, to somewhat heavier nuclei than have been studied to date, and to the neutron-rich side of beta-stability. Work employing the previous ASIC our group has developed has revealed new decay modes and reaction phenomena, found many new resonances and improved the parameters (energy, decay width and decay modes) of previously known resonances. Some of the latter impact our understanding of nucleosynthesis. These data have allowed for testing state-of-the-art many-body theories dealing with open quantum systems.

Broader Impacts :

The previous ASICs developed by us are in widespread use and the specific enhancements proposed here should find even wider use at the new generation of secondary-beam facilities. Two of the three proposed chips are modifications of existing chips and the third is a chip the primary element of which is a generalization of a circuit element we have experience with on one of the other chips. It is clear that a chip based on this one element will find great utility as a stand-alone ASIC. Examples of detector systems that would be enabled by the proposed development are provided. The project is made efficient because the three development projects have many overlapping design features.

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For font size and page formatting specifications, see PAPPG section II.B.2.

*Proposers may select any numbering mechanism for the proposal. The entire proposal however, must be paginated. Complete both columns only if the proposal is numbered consecutively.

3. PROJECT DESCRIPTION

Justification for Development

This proposal seeks funds to complete the development of an analog pulse-processing Application Specific Integrated Circuit (ASIC) "tool-box" for use in low-energy nuclear physics. The proposed development builds on the ASICs designed previously by our group that have found use by many projects (detailed below). ASIC development is a substantial development effort in its own right that requires close interaction between active experimentalists in the field and analog CMOS engineers and provides the only cost effective way to field high-channel-count systems.

The study of nuclei far removed from stability is a growing area of research with major national and international investment in the required accelerator and separator facilities. To make efficient use of such facilities, complicated, and often large-channel-count detector systems, must be deployed. Without the proposed technology, users would be forced to use much more expensive digital-signal-processing technology (DSP). While DSP is often required, just as frequently it is not and without the cost-effective alternatives proposed here, creative research (often initiated by small university groups) will be throttled by limited funds and forced into the large collaboration herds. (It has become characteristic of nuclear physics that large projects compete with each other for the available funds, squeezing to the margins smaller, but often creative, projects.) In the following section several projects are mentioned that are now operational because a chip-based analog processing scheme was available. We contend that these projects could not have been deployed – likely not even proposed – if macroscopic analog or DSP technology were the only options. Also in the next section we offer two examples of how this dynamism can continue if the technology we are now proposing became available. In short, only with the development proposed can modest sized university groups realistically envision fielding Si-strip or scintillator arrays with channel counts approaching or exceeding 1000.

This proposal will not simply produce the ASICs but incorporate these chips into entire pulse-processing systems. The components of this system are interchangeable and therefore substantial intra- and inter-group flexibility is generated. For example, components built in the past for one project and group have been shipped and used by different groups in the US and abroad. This is akin to shipping NIM (nuclear instrument modules) around, but a small shoe-box sized shipment enables the receiver to add another 512 channels to their system. While our previous ASICs have created this community of users, the present proposal will extend the functionality of the ASICs and make them easier to use and by doing so, likely even further expand the community of users.

Research Activities to be Enabled

The intended use of the proposed technology is for the study of nuclei removed from the valley of stability. The focus of the work of our local collaborators (Washington University's nuclear reactions group of Charity and Sobotka) has used the invariant mass technique to reconstruct the continuum of light nuclei. Specific accomplishments of that program have been: a) finding the only case of sequential 2p-2p decay, b) discovery of a new type of 2p decay – between excited isobaric states – when there is no energy and isospin allowed single-nucleon decay, c) study the

decay of the Hoyle state in exacting detail, d) observe a reaction mechanism generating extreme nuclear alignments via a spin-flip (a mechanism enabled by unique nuclear structure of the reactants), and e) complete or greatly reduce uncertainties of several isospin multiplets thus allowing for improved examination of isospin symmetry breaking. Along the way, this effort has generated new resonance data for states in the A = 5, 6, 7, 8, 9, 11, 12, 13 and 16 isobars. (A complete list of references to these works can be found on the web sites for Charity or Sobotka.)

As this effort has moved to heavier and heavier systems there is a growing experimental challenge to be able to detect light charged particles (p, d, t and alpha particles) and heavy ions in the same detectors (e.g. Si-strip). This problem was confronted in a recent revision of our initial HINP chip [1] for which we added dual active shapers [2]. With this addition, along with changes to the internal charge amplifier, peak tracker and discriminator, the present design has sensitivity from 250 keV to 400 MeV. As this chip had enough new elements to make its production "high risk", we chose not to include the feature of allowing external Charge-Sensitive preAmplifiers (CSAs) to be used. Now, with the successful production and deployment of this extended range chip, we are now confident that we can add the external CSA option. This addition would, e.g. allow for the use of the dual-range shapers with thin dE detectors, detectors with capacitances that cannot be dealt with in CMOS.

To provide a concrete example of the utility of the proposed technology: consider the search for the ground-state of ^{11}O, the mirror of ^{11}Li. ^{11}O will decay by 2-proton emission to ^{9}C. (The physics here is that the percentage of the 2nd s orbital in the wave function will be inversely reflected in the energy of this resonance.) Presently this experiment can only be done at high energy using a Si-CsI(Tl) array. The resolution in such experiments is determined by the CsI(Tl) scintillator. Higher resolution would be achieved at lower energy (expected from reaccelerated beam facilities) employing stopping in a highly pixilated dE-E silicon-silicon telescope array. This not only requires a system with large dynamic range but the capability to generate excellent resolution for high-capacitance (dE) detectors. The large capacitive slopes (resolution vs capacitance) of chip based CSA's requires pulse processing using macroscale (external) CSA's. No such chip exists and instrumenting thousands of channels in conventional electronics (not to mention DSP) is cost prohibitive. The present proposal would solve this problem and in essence present all Si-strip projects, which choose to go analog, to have one choice: internal or external CSA, but either way, the downstream electronics would be the same and provide huge dynamic range and excellent timing. Such commonality across experiments allows more varied experiments to be contemplated, working under the constraints of limited resources.

This project (we call it project A) combines features of two pre-existing and well-tested chips. The original chip in this series was developed (by us) for the HiRA [3] project and that development project has allowed for (to date) 19 papers on continuum structure and reaction mechanisms, 4 papers on the evolution of spectroscopic factors with asymmetry using transfer, 3 on the mechanism of knockout reactions, one paper each on the asymmetry dependence of the nuclear equation of state and another on the mass of a potential rapid-proton capture waiting-point nucleus. Just as important as the HIRA based work is the utility that results from the flexible nature of the designed circuits. The previous HINP chip has been used at the NSCL, TAMU, RIKEN/HIMAC, ANL, FSU and ND. The major detectors built by other collaborations using our HINP chip are: SuperORUBBA [4], ANASEN [5] and an upgraded FAUST [6]. A

testament to the flexibility of the system we developed, with our colleagues from Washington University, is the recent case of a set of experiments done at the Texas A&M cyclotron institute using FAUST that were executed with the electronics built for HiRA that were not in use.

Our most recent version of the HINP chip (designed for a project at RIKEN [2]) added dual active gain ranges but does not have the external charge-sensitive amplifier (CSA) capability. The proposed development adds the external CSA to the dual-active-gain capability. This would not only allow the HiRA program to expand (up the proton-drip line and make use of both low and high-energy facilities) but allow others to expand, or more highly pixilate, existing Si devices and yet others plan 1000+ channel systems without 6-figure electronics costs. The uniform use of this technology could allow users to switch from internal to external CSA's and yet maintain the huge dynamic range offered by the dual-shaper system and the simplicity offered by the compact pulse processing of an ASIC.

Our second project (B) is to generate more mass integrator chips capable of yielding particle identification from scintillators with pulse-shape discrimination. Seven years ago we fielded an ASIC which, when used in conjunction with external discrimination, could be used to generate the integrals from three user selected regions of the light pulse from a scintillator [7]. This chip greatly simplifies the task of creating a large array of scintillators that contain particle identification information in the pulse shape. Do date, one device for basic nuclear science has been fielded using this chip [8], an advanced survey meter has been designed [9] (and forwarded by LANL for commercialization) and another device for basic science is being constructed [10]. There are no more of these chips available and in fact to execute the last of the devices mentioned above, LANL has agreed to donate some of the chips they bought of our original design back to us. With little effort, we can make a slight improvement to the design and get another batch of these PSD integrator chips. While it would take more effort, if we felt the need were sufficient, we could double the number of channels from 8 to 16. (The original chip was intended to be 16 channels, of 3 integrators each, but we held back for financial reasons and because the initial projects employing this chip [8,9] had modest channel counts.)

To focus the reader's attention on what would be possible with the PSD chip complemented by the CFD chip described below, consider a highly granular discrete element array for neutron detection using the recently developed inorganic [9] and plastic [11] scintillators with PSD. Such a large array would open the n-rich side up to the kind of high-precision work the Washington University group has done on the p-rich side. (The existing work on the neutron-rich side, done at high energy and with detectors such as MONA-LISA [12], while providing provocative data on such cases as ^{16}Be [13] and ^{26}O [14], sufferer for poor statistics and, compared to the proton-rich side, poor resolution.) An array to be deployed at low (reaccelerated beam) energies with thousands of optically isolated PSD elements made from the new generation of plastics would revolutionize the study of multiple n-decay from what are generally high-isospin states. (The problem of detector-to-detector scattering cross-talk can also be improved with discrete pixilated – rather than using large bars – by corrugating the detectors in the same way as the conventional discrete array DEMON has [15]. While we are enamored with the above idea, it is premature to propose such an array before the ground-work for scalable electronics, as we propose here, is successfully completed. (In fact the coupling of the scintillator – from Eljen – to the new blue sensitive SiPMs – from SensL – is simple compared to the development of the scalable

electronics.) To this end however, the evaluation of parts B and C (see below) of the present proposal is then to develop a circuit board using the PSD and CFD chips (see below) to process signals from the new generation of PSD-capable plastic scintillators [11].

The third project in this proposal (C) is the modification of the discriminator (CFD) circuit used in our most recent HINP chip. The significant modification to the circuit would be to add a user controllable delay, a modification that will allowed the circuit to be deployed for a variety of scintillators (LaBr:Ce to CsI:Tl or :Na to standard plastics and, for what might be the most interesting untapped opportunity, the new class of PSD capable plastics [11)]. The circuit modification is presented in the technical section below as are some circuit simulations. This chip is essentially fully analog with the only interfacing being the control of the (RC) delay feature mentioned above and the threshold. This chip will be 16 channels and, because it will be small (we estimate about 4 mm x 4 mm), relatively inexpensive to fabricate.

Results from Prior NSF Support

In order to comply with the rules of the MRI solicitation, we briefly describe results from prior NSF support. The PI has not received any relevant NSF support in the past 5 years. The only relevant support was a NSF-MRI in 2006 when Prof. Engel received a $192,754 grant to design and fabricate the PSD chip referenced in this proposal.

The PI has received completely unrelated NSF funding in the past 5 years. He was awarded a sub-award from a NSF STTR Phase II-B Award (IIP-0924010), entitled "STTR Phase II (B): Blended Clocked and Clockless Integrated Circuit Systems". The sub-contract to SIUE (with Prof. Engel serving as PI for the sub-award) of $86,420 was for the period July 1, 2012 – Jun 30, 2014.

i. Intellectual Merit

The work performed at SIUE yielded a paper and a patent:

Delay Tolerant Asynchronous Interface (DANI), Patent No. 8.826,058, 2014, United States of America (with J. R. Cox, J. Moscola, T .J. Chaney).

Engel, G.L.; Ziebold, J.; Cox, J.; Chaney, T.; Burke, M.; Gulotta, M. Multi-Cycle Path Challenges in Multi-Synchronous Systems. *ICCAD 2012 (MSCAS Workshop)*, San Jose, CA - November 8, 2012.

ii. Broader Impacts

The work performed at SIUE was instrumental in helping Blendics, Inc. acquire over a million dollars of investment from the National Innovation Fund (NIF). For more information on Blendics see www.blendics.com.

Description of the Research Instrument and Needs

Three chip projects are described below. The order presented below is from what the reader might be familiar with to a new design. The modifications of the Si processing chip (HINP) are minor, but changes in layout might be significant. The changes to the chip for pulse shape discrimination (PSD) are minor and, in fact, the layout is already complete for the 8-ch version. (This proposal will fund a chip submission and provide parts to make one and expand another device.) The third project (a universal CFD chip) is new but builds on the CFD in the HINP chip. This last chip is required for a high-channel-count n/γ array using a new class of scintillators. This last (CFD) element is the innovative aspect, and thus prime motivator, of the proposal. It will also serve as the class project for an analog design class for the 2016 Spring (present) term. However with the team assembled for the design, simulation, layout, fabrication and testing of the universal CFD ASIC, all the other ASICs can be updated.

All chips will be designed for and fabricated in the 0.5 μm technology which we have used previously. This is an inexpensive process offered regularly by the MOSIS chip manufacturing consortium. While the feature size is far from state-of-the-art, it is motivated by the fact that this technology allows for voltage rails of 5V (actually a bit more). These chips also use internal 5V logic. A general feature (change from existing designs) of the chips discussed in this proposal is to employ pads for the logic that converts (external) 3.3 V signals to (internal) 5.0 V signals. This change will also allow us to seamlessly (without external voltage translation) employ 3.3 V logic external to the chip, a voltage compatible with the Xilinx Spartan 3AN series of FPGAs. At the same time we will be able to push the analog rails to 5.5 V, further increasing the dynamic range by 10% over existing chips. The present design compels the system designer to either use hard to find 5V Spartan chips or voltage translate on the chip boards, the latter is what is presently done. The pad modification will slightly increase the cost of chips but greatly decrease the complexity, size and cost of the chip boards (CBs).

A. Silicon-strip processing chip – HINP-d

A block diagram of a single channel of the Silicon-Strip processing chip (HINP-dual) is presented in Fig. 1. Our initial chip in this series (HINP-c: used in all the major projects to date and employed in over two-dozen science publications) had two internal CSA ranges but one had to select one or the other. The present design has dual *active* ranges. Another improvement is that an amplifier has been added before the leading-edge comparator. A recent chip run proved that both of these features worked providing an effective range of 250 keV to 400 MeV. This chip also repaired a feature that did not work on the chip presently in wide-spread use – a user selectable coincidence time window (time before the chip auto resets) that ranges from μs to ms.

Extensive range and linearity tests have been done on this dual range chip. The performance of a representative channel is shown in Fig. 2. Some channels (random) exhibit a compressive linearity above half range on both low and high gain. We suspect that this calibratable non-linearity is introduced by transistor mismatch in the peak-tracker circuit which was used on the chip. While one could consider this non-linearity a “feature”, in that it further extends the range and is can be calibrated, it is a nuisance as the nonlinearity exhibits channel-to-channel variations. Another minor problem with the present design of the dual-gain chip is that the pulser

input cross talks to one of the input channels. While not a problem when taking data as the pulser is switched off at the chip, the pulser gain on this channel is larger than the other channels.

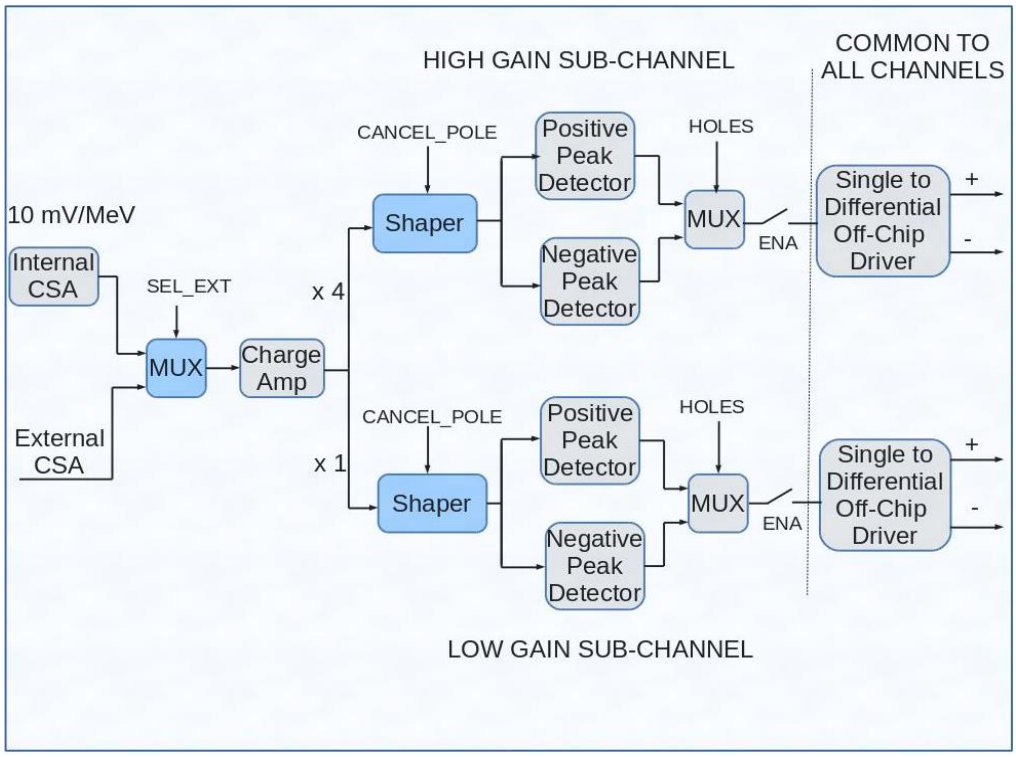


Figure 1*: Schematics of the new Si-strip signal processing chip. The nominal full ranges of the two active ranges are 100 and 400 MeV. The most significant change to be implemented in this chip, not present in our most recent fabrication run, is the addition of the capability to handle external CSA's and thus allow for this processing system to handle large capacitance detectors. For this change, the elements in blue must be added or modified.*

The redesign of HINP-d would allow for one major and several minor improvements.

Major (addition)

Add the option to run with external preamplifiers. The circuit modifications shown in Fig. 1 (switchable MUX and pole cancellation in the shaper – blue elements), will restore this functionality.

Minor (improvements)

1. Change the pads for logical signals to allow for the use of 3.3 V external logic. This will ensure future FPGA compatibility and remove the need for the employment of voltage converters on the chip boards. (This reduces the cost of system fabrication and CB size as it removes components that occupy a full one-third of each CB.) We also expect a

reduced CB complexity will decrease the difficulties in production and improve reliability.

2. Add additional buffering of a control signal that will speed downloading and repair timing on the negative branch.
3. Remove a pulser-input cross coupling to one channel (7). This cross coupling was due to a poor arrangement of the input pads.
4. Remove (random) channel-dependent nonlinearity.

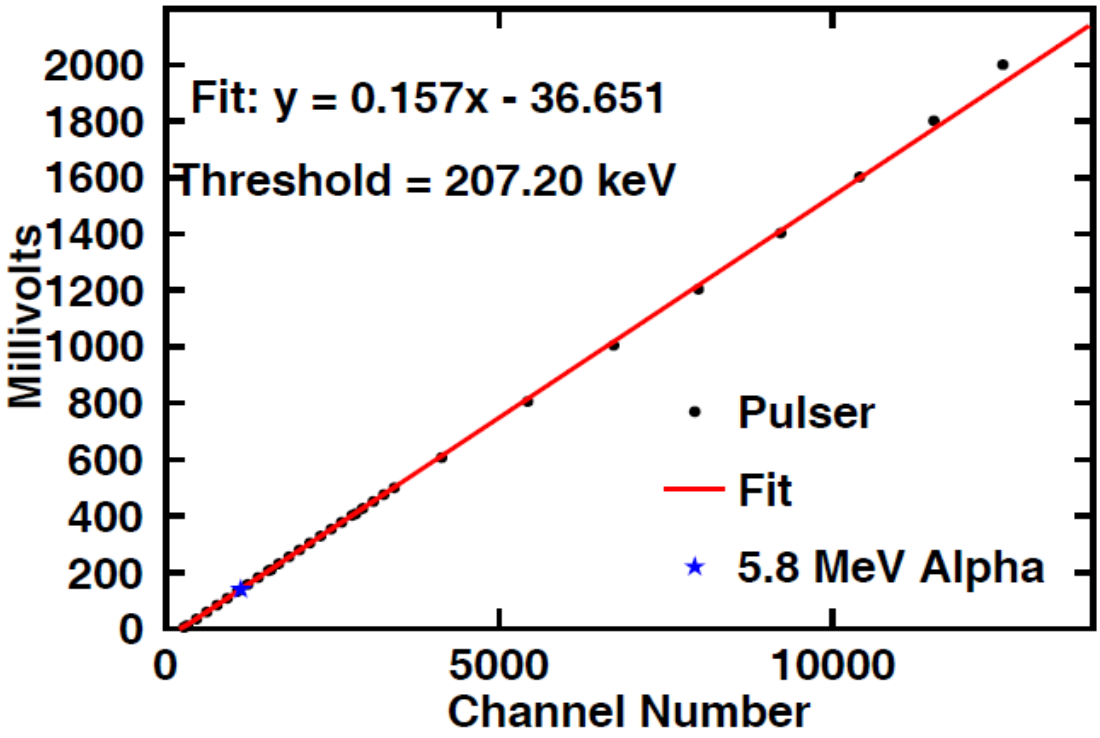


***Figure 2**: Pulser and α linearity test of the high-gain channel of the dual-range chip. Not all channels are this linear. The linear fit is on the dense data at low pulse height.*

B. Mass integrator - PSD chip

Six years ago we had a modest-sized production run of a mass integrator chip designed to aid in processing the signals from signficant arrays of PSD-capable scintillators [7]. Figure 3 illustrates how this chip (PSD8c) is deployed in a system. Note that external discrimination is required. This chip has been deployed, as illustrated in Fig. 3, in two devices [8,9]. A recent request [10] exhasuted all existing chips and neither that project nor the expansion desires of what is called the Phoswich Wall [8] can be surviced as no more of these chips exist. The slight modification of the chip to allow for 3.3V logic and to fix an error, circumvented by external logic on the existing systems, have already been completed, simulated and incorporated into the 8-ch design. The present proposal would supply funds for another submission. This project falls naturally within the present proposal in that the collaboration assembled for the other tasks are those required to usher the design through the submission and packaging processes and to test the

produced ASIC. Our intended use of this chip is in conjuction with the CFD chip discussed below. This generating and testing a CB doing the entire processing shown in Fig. 3 will be done.

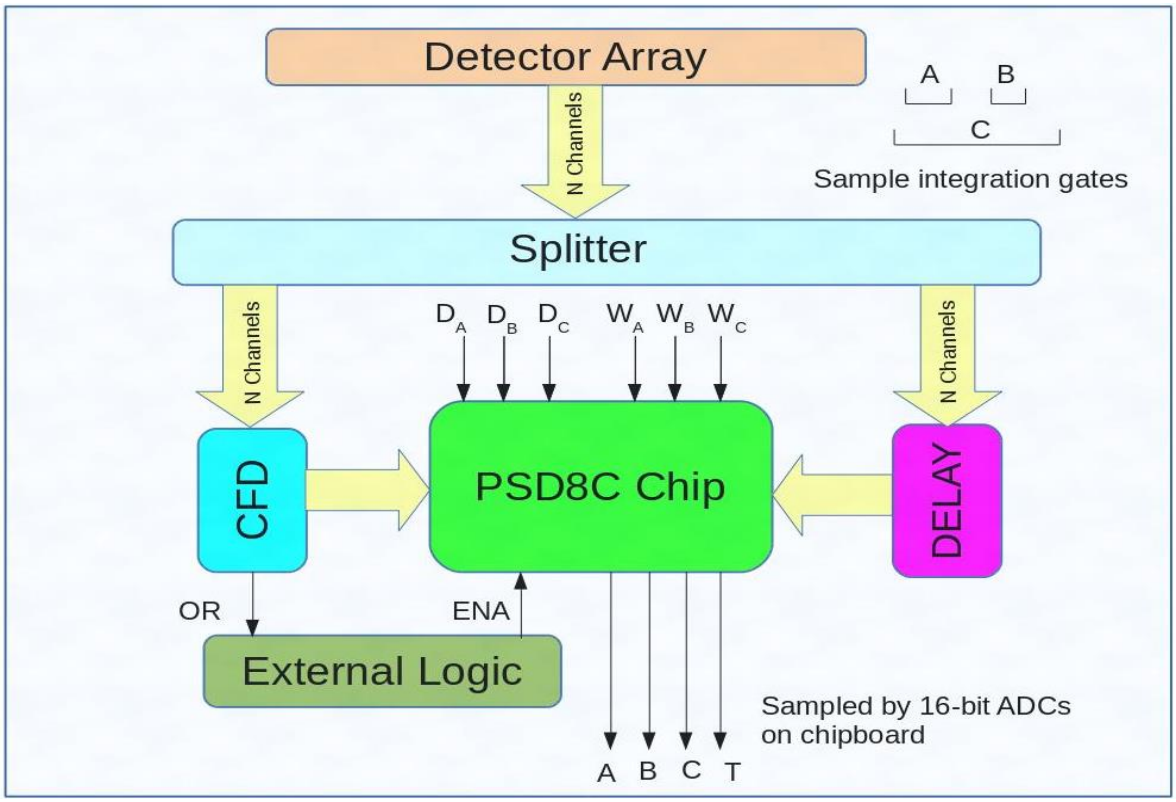


***Figure 3**: Illustration of a system employing both the CFD and PSD ASICs [7]. The three delays and widths (D_A,D_B, D_C and W_A, W_B, W_C) are selectable and can be referenced to individual CFD times. The external logic supplies a signal to the PSD chip to prevent a clearing operation and to initiate readout of charges (A, B, and C) and time. See references [8] or [9] for specific examples using the PSD chip with macroscopic CFDs. The splitter and delay components are also macroscopic. In the proposed design, the splitter, CFD-ASIC, delay and the PSD-ASIC will all be on the same circuit board. However an option to bypass on-board delay chips and employ external (cable delay) will be provided. In some cases, the use of the compact (LC) delay chips might cause unacceptable signal slewing.*

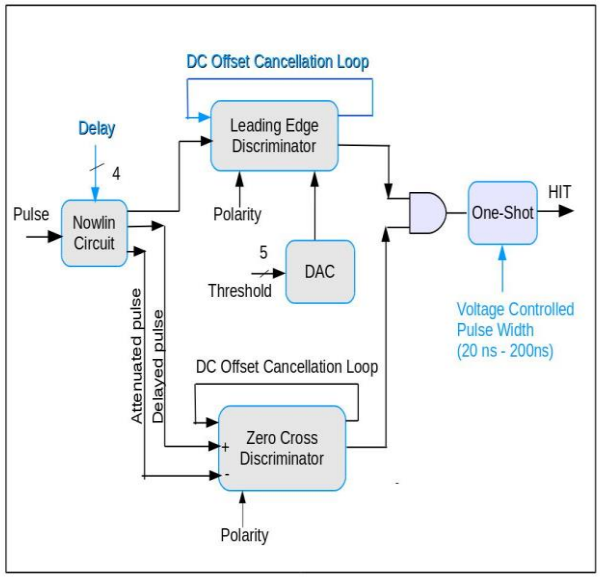
C. Stand-alone discriminator - CFD chip

From one standpoint is it a bit surprising that a stand-alone (i.e. general purpose) CFD ASIC has never been produced. However this omission to the ASIC tool bag can be understood. Most ASIC development projects are directed at a specific, and generally rather large and well-funded, project. In such projects, the discriminator is built into an ASIC and optimized for a single task. Our university based ASIC development program (where students rather than highly-paid

professionals do the detailed design and layout) has reduced the cost of designing an ASIC to the point where we have become to view ASIC components much like NIM modules.

To create a general purpose CFD ASIC, one has to build in the flexibility one finds in macro circuit designs to properly process signals with varying signal shapes. The basic design is a generalization of what was done in 1.2 μm CMOS some time ago [16]. With the experience gained on HINP and simulations done recently, we believe the generalizations required to make the ASIC broadly useful can be done. A block diagram depicting a single channel of our proposed multi-channel discriminator IC is presented in Fig. 4a. The leading-edge discriminator circuit consists of a cascade of 2-3 very high bandwidth (but low gain) differential amplifiers. A "slow" DC offset cancellation loop drives the input referred offset for the cascaded amplifier to the sub-mV level. The amplified (offset-free) output is then compared with a programmable threshold using a continuous-time comparator. The output from the leading-edge circuit qualifies the output from the zero-cross circuit. The zero-cross circuit, like the leading-edge circuit, consists of a cascade (but here 5 – 6 stages are required) of very high bandwidth (but relatively modest gain) differential amplifiers followed by a high-speed analog comparator.

a)



b)

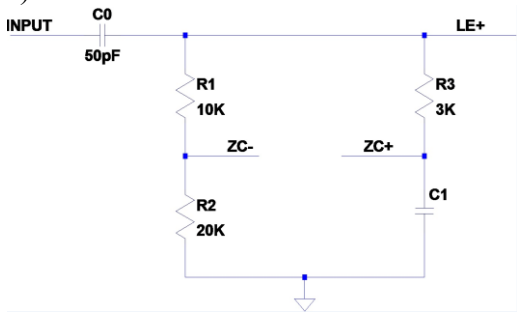


***Figure 4**: a) (left) Overall CFD logic for stand-alone CFD ASIC. A leading-edge circuit qualifies the zero-cross discriminator. The features in blue are either new or modifications of the CFD in the HINP ASIC. b) (right) Nowlin circuit. R3 and C1 determine delay. The present plan allows for 16 different (i.e. selectable) delays*

The circuit generating a signal suitable for CFD logic (called a Nowlin circuit when discrete elements – rather than cable - are used to generate the required delay) is shown in Fig. 4b. The capacitor C_0 along with the series resistance of R_1 and R_2 implement a "fast" shaper. The output of this high-pass filter is applied to the leading-edge discriminator. Also, a fraction, $[R_2/(R_1+R_2)]$, of the "fast" shaper output is applied to the inverting input of the zero-cross discriminator along with a delayed version of the input pulse connected to the non-inverting input. As is well-known, the time at which the differential voltage crosses through zero is independent of the input amplitude.

Schematic level simulations of the circuit have been performed and a representative case (signal rise time constant of 3 ns) is shown in Fig. 5. Shown are the input and output signals to the Nowlin circuit, i.e. after the fast shaper and the signal for which the zero crossing is sought. When the Nowlin delay is adjusted to a large fraction of the rise time, the CFD logic produces a bipolar pulse with a rapid transition through zero, the position of which is close to amplitude independent.

Our present schematic level simulations, which can be found at [17], indicate that both walk and jitter of less than 5% can be achieved with noiseless signals. We expect this to be achieved for a large part of the designed factor of 100 dynamic range (20 mv to 2000 mv) but clearly will not for the lowest amplitudes. These simulations are just the initial phase of the design work that must be done, see [17] for details. Additional design at the electrical level will be completed in the present spring term, i.e. before funding of this grant would commence.

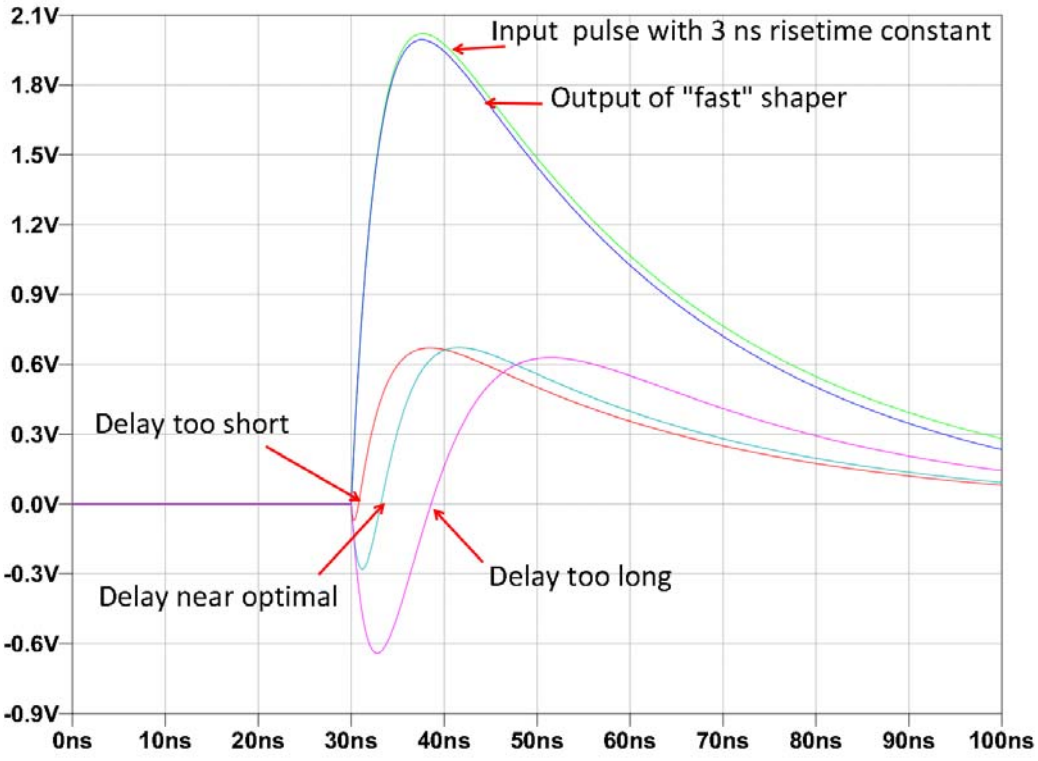


***Figure 5**: Simulated response to input signal with 3-ns rise time constant. A programmable delay allows matching of the Nowlin delay to the signal rise time.*

Impact on Research and Training Infrastructure

This proposal is to fund the ASIC development aspects of a collaboration that is the only one in the US devoted to ASIC production for low-energy nuclear physics. The foci of this effort are: the Southern Illinois University at Edwardsville, a branch of the Southern Illinois University system with a strong analog IC engineering training program and Washington University, a

university with a significant basic nuclear science effort. (The latter effort is separately funded.) The two campuses are in close proximity and the groups have worked together for over a decade. The Washington University group is committed to participating in the design discussions, incorporation of the ASICs into workable systems and in the evaluation of these systems.

The primary impact on research will be to provide the tools (ASICs and the support hardware and software) required for those tasks for which digital processing technologies are cost prohibitive. Examples are large arrays of discrete element scintillators with n/γ PSD and arrays of Si-strip detectors requiring huge dynamic range.

This proposal will educate a small cohort of students in the design, production and deployment of analog micro-circuits. While our aim is to generate user friendly (non-expert) systems, those trained in this project will be the system experts who will be both a valuable resource for the greater user community and capable of further ASIC development for the basic science community at large.

The PI, Professor Engel, teaches a graduate level IC analog design course in the present term (Spring 2016). The class project will be to explore the design of some of the functional blocks required by the CFD chip. Not only will this allow for a wide spread real-world training experience, but a more complete set of simulations can be done and cross checked. (The enrollment of this class is approximately 15.) By the summer of 2016 , many of the schematic level CFD simulations will be complete and, if this grant is approved, the chosen outstanding students moved on to complete the electrical design and the detailed IC layout. This also presents the potential to capture the interest of young and well-trained analog-IC engineers in efforts to advance the state-of-the-art in radiation detection and measurement. One outstanding student, taking the class mentioned above, has already self-identified with this interest. In this particular individual we see the possibility to train a colleague, and ultimate replacement, for Mr. J. Elson of Washington University who has served as the technical point person for the ASIC's developed for low-energy nuclear science by this collaboration.

Every student who has previously worked in any aspect of the SIUE/Washington University ASIC effort has remained engaged in US STEM fields. During the lifetime of the collaboration two students have graduated with a Ph.D. in basic science (from WU) and about a half dozen with a M.S. in engineering (the highest degree offered by SIUE). Several of the master's students now work at INTEL, where their analog expertise is coveted for the design of test circuitry and for their almost unique experience – for students - of fielding a real device. The other engineering students are at smaller tech-sector companies. We do not know of another active effort of mixing analog/digital chip design for basic science conducted at the student level. (The employment of students for the design and layout of the ICs is the reason this effort can operate on modest budgets. There is also the downside that new students must be continually trained – but that of course is part of the university and NSF mission.)

The ASICs we propose to develop with this MRI will further fuse several university groups in their use of common technology. The group of our close collaborators at Washington University (Charity/Sobotka), two groups at TAMU, and others at MSU, LSU, WMU, as well as a group in Romania will likely convert to the new HINP-d. Another local group at WU-STL

(Reviol/Sarantites) and one at FSU will make use of both the PSD and CFD chips. The consequence for funding agencies will be that proposals will be submitted from small to modest sized university groups that could only be envisioned because the pulse-processing electronics come at modest cost. These proposals will be technically sound because they will have benefitted from the testing and evaluation done with the present grant. Decoupling of the signal-processing development from the detector development is desirable from several standpoints. We can optimize the engineering effort to produce multiple chip designs and the time lines for the signal processing development (on the one hand) and physical detector construction (on the other) can each be accommodated in standard grant cycles without the need for multiple extensions.

Broader Impacts of the Proposed Work

In summary, the previous ASICs developed by us are in widespread use and the specific enhancements proposed here should find even wider use at the new generation of secondary-beam facilities. Two of the three proposed chips are modifications of existing chips and the third is a chip where the primary element of which is a generalization of a circuit element we have experience with on one of the other chips. It is clear that a chip based on this one element will find great utility as a stand-alone ASIC. Several examples of detector systems that would be enabled by the proposed development were provided in this proposal.

Assessment of risks

The fabrication of chips is generally a high-risk venture. Mistakes, no matter how minor, cannot be truly fixed. However logic errors can (and have been in present designs) be worked around by FPGA programing. In our present systems each pair of ASICs share an FPGA to download the chip's registers and to control the flow of analog data off the chip and ultimately digital data to more remote FPGA's. All present systems employ three levels of FPGA, i.e. one shared by two chips (on what we call the chip broad – CB), another on what we call the mother board (MB) common to 32 chips, and the last in the commercial VME module that digests the digital data. (In the proposed designs, the VME module is purely digital with all digitization occurring remotely and in parallel on the CB's.) With the voltage conversion for logic done in the pads (see Fig. 6) all these FPGA's will be in the Spartan 3AN series. There is very little risk in this conversion. There is also little risk to a PSD-8c run as the chip modifications are minor.

On the other hand, both the CFD and HINP-d have considerable risk. While the changes at the schematic level to HINP are modest (addition of a MUX, a associated switchable resistor to add a node to ensure prompt baseline restoration for the external CSA, changing the size of a few components to restore linearity, adding some signal buffering to improve digital download and control and changing the pads to allow for seamless use of external 3.3 V logic), the layout will have to be extensively modified. Changing the layout is required for efficient packaging (to make the chip less eccentric in its two dimensions). The layout work is time consuming and mistakes can be introduced. Fortunately, from our previous work, a full suite of simulation scripts exist. It does however take months to run this suite and test the entire HINP functionality.

The CFD has new schematic elements and is also a new chip. While many of the schematic features will be common to the CFD used in HINP, there are many new elements (see elements

in blue in Fig. 4a) requiring both separate optimization and an entirely new layout for a standalone chip. Risk is minimized by having the same people design, layout, and cross check the HINP-d and the new CFD. The much smaller, and thus less expensive, CFD chip will be submitted before HINP-d is submitted not only to minimize the risk for the more expensive chip but also so relevant improvements can be back ported to HINP.

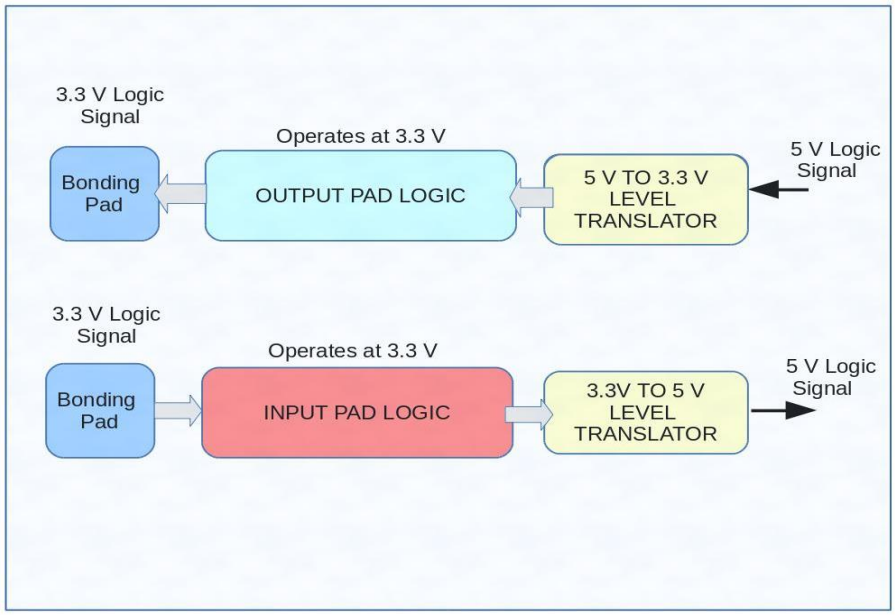


Figure 6*: Pad logic allowing for use of 5 V (internal) linear rails but 3.3 V (external) logic.*

Management Plan

Estimated Time Breakdown, Fabrications Costs and Time Line

The management and dissemination of information will be orchestrated by the following activities.

1. During the active design periods, our group will (as we have in the past) get together biweekly with our colleagues at Washington University with the intervening weeks serviced by a SKYPE conversation. Every other month, a note will go out to all potential users inviting them to join the SKYPE meeting. Such meetings will be preceded by an agenda and a file containing the results to be discussed.

2. A WEB site will contain all chip simulation results (supplied by G. Engel) and a second site will contain the actual chip testing results (supplied by J. Elson) [17]. All potential future users will be prompted by an email when new results are available. These announcements will be linked to the open SKYPE meetings. The CFD chip design and simulation effort will be the basis of an MS thesis. A second thesis describing HINP-d is also contemplated. These theses will be the ultimate repository for the simulation results

and the detailed layout of the generated design. These will be downloadable from the Prof. Engel's website as will be reports on the two other upgrades. The actual chip testing results will be presented in Nucl. Instru. and Meth. papers. These practices are standard for our collaboration.

3. As we have done for our previous development projects, we (along with our colleagues at Washington University) will host demonstration and testing sessions. (In the past groups from MSU, ORNL, TAMU, FSU and LSU have attended these sessions.) We anticipate two such sessions, one for CFD and PSD in the middle of the second year, and the second – for HINP-d at the end of this grant.

The time estimated for schematic development, layout and to simulate (from the detailed extracted layout) as well as the estimated areas and costs of the proposed IC's are provided in Table I. In the extremes, there is no development time for the PSD chip, while the new CFD chip requires extensive development. A minor change to the PSD logic has already been implemented and the pad-layout changes have also already been ported into the design. Thus the modified PSD-8c is ready for submission. The changes to HINP will take several months (see Table 1) and we expect to do this after the CFD design is complete. (This is so we can make use any portable changes to the CFD design suitable for Si-strip detectors.) The specific time-line for the various steps of the CFD project is provided in Table II. Our intention is that the (8-channel) version of the PSD chip will be resubmitted immediately on grant approval and the HINP modification will proceed in parallel to CFD testing.

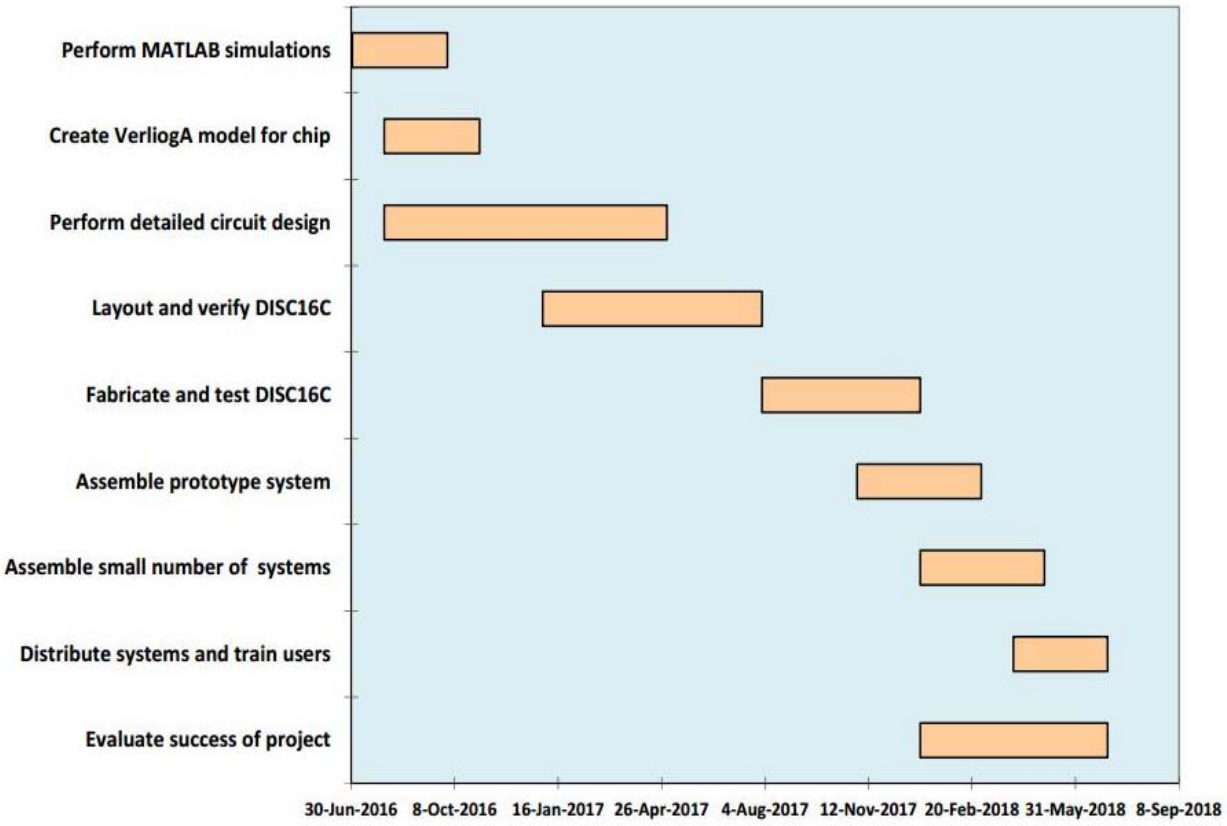
Table 1: Estimated time and Fabrication costs[a]

Chip	Dev/Layout/sim Time (mo)	CB layout[b] (mo)	Sys. Debug[b] (mo)	~Area (mm^2)	# of chips	Cost k$
HINP	**3 / 3 /4**	**0.5**	**2**	**60**	**160**	**30**
PSD	**0 / 0 /1**	**0.5**	**0.5**	**25**	**80**	**20**
CFD	**4 / 5 /4**	**0.5**	**2[b]**	**20**	**80**	**15**
						65

[a]The costs are all based on recent MOSIS submissions or cost schedule for the ON Semiconductor-C5 process.

[b] CB development and system debugging will be done in conjunction with the Washington University group and make use of their laboratory. This includes a system using both the PSD and CFD chips designed for use with the new generation of plastic scintillators.

Table 2: Schedule for CFD development.



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For chip design specifications, schematics and simulation results see:
http://www.siue.edu/~gengel/
Testing results generated by our colleagues at Washington University will be found at:
http://pages.wustl.edu/jelson

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A. PROFESSIONAL PREPARATION:

St. Louis University	St. Louis, MO	Mathematics and Physics	B.A.	1982
Washington University	St. Louis, MO	Electrical Engineering	B.S.	1984
Washington University	St. Louis, MO	Electrical Engineering	M.S.	1985
Washington University	St. Louis, MO	Electrical Engineering	D.Sc.	1990
Washington University	St. Louis, MO	Electrical Engineering	PostDoc	1990-1993

B. APPOINTMENTS:

2007 - present	Co-founder/Vice-President of Blended Integrated Circuit Systems
2007 – present	Professor of Electrical and Computer Engineering, SIUE
1999 - 2007	Associate Professor of Electrical and Computer Engineering, SIUE
1993 - 1999	Assistant Professor of Electrical and Computer Engineering, SIUE

C. PRODUCTS:

(i) Products Most Closely Related to the Proposed Project.

1. George L. Engel, "Two CMOS Solutions for Two Different Signal Processing Problems" *ANSiP-2011: Advanced School & Workshop on Nuclear Physics Signal Processing,* Acireale, Italy - November 21-24, 2011.

2. George L. Engel, VikramVangapally, Naveen Duggireddi, Lee G. Sobotka, Jon M. Elson, Robert J. Charity. "Multi-Channel Integrated Circuits for Use in Research with Radioactive Beams", Application of Accelerators in Research and Industry, AIP Conf. Proc. 1336, 608-613 (2011).

3. George L. Engel, Naveen Duggireddi, VikramVangapally, Lee G. Sobotka, Jon M. Elson, Robert J. Charity, "Multi-Channel Integrated Circuits for the Detection and Measurement of Ionizing Radiation", Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 652, Issue 1, 462 – 465 (2011).

4. G.L. Engel, M.J. Hall, J.M. Proctor, J.M. Elson, L.G. Sobotka, R. Shane, R.J. Charity (2009) Design and Performance of a Multi-Channel, Multi-Sampling, PSD-Enabling Integrated Circuit, *Nucl. Instru. Meth. A*, 612, 161-170.

5. G.L. Engel, M. Sadasivam, M. Nethi, J.M. Elson, L.G. Sobotka, R.J. Charity (2007) A Multi-Channel Integrated Circuit for Use in Low- and Intermediate-Energy Nuclear Physics - HINP16C, *Nucl. Instru. Meth. A*, 573, 418-426.

(ii) Other Significant Products.

1. Delay Tolerant Asynchronous Interface (DANI), Patent No. 8.826,058, 2014, United States of America (with J. R. Cox, J. Moscola, T .J. Chaney).

2. Method and apparatus for authenticating a magnetic fingerprint signal using compressive amplification, Patent Number: 7377433, 2008, United States of America (with R.E. Morley, E.J Richter).

3. Design of instantaneously restartable clocks and their use such as in connecting clocked subsystems using clockless sequencing networks, Patent Number: 7243255, 2007, United States of America (with J.R. Cox, D.M. Zar).

4. Electronic filters, repeated signal conversion apparatus, hearing aids and methods, Patent Number: 5225836, 1993, United States of America (with R.E. Morley, A.M. Engebretson, T.J. Sullivan).

5. Electronic filters, signal conversion apparatus, hearing aids and methods, Patent Number: 5111419, 1992, United States of America (with R.E. Morley, A.M. Engebretson, T.J. Sullivan).

D. SYNERGISTIC ACTIVITIES:

1. Membership in Phi Beta Kappa, Eta Kappa Nu, IEEE, Phi Kappa Phi
2. Received B.A. degree from St. Louis University in Physics/Mathematics, Summa Cum Laude
3. Received B.S. degree in Electrical Engineering from Washington University, Magna Cum Laude
4. Recipient of 2012 Paul Simon Outstanding Teacher-Scholar Award
5. Received "IEEE Third Millenium Award" for Outstanding Achievements and Contributions.

E. COLLABORATORS & OTHER AFFILIATIONS:

(i) Collaborators and Co-Editors During the Past Four Years - TOTAL =7

Lee Sobotka (Washington University), Robert Charity (Washington University), Jon Elson (Washington University), Jerry Cox (Blendics, Inc.), David Zar (Blendics, Inc), Tom Chaney (Blendics, Inc.), Ian Jones (ORACLE)

(ii) Investigator's Graduate and Postdoctoral Advisors - TOTAL = 2

Postdoctoral Sponsor: Robert E. Morley, Washington University
Ph.D. Advisor: Robert E. Morley, Washington University
M.S. Advisors: Robert Gregory, Retired

(iii) Thesis Advisor and Postgraduate-Scholar Sponsor- TOTAL = 2

M.S. Students w/Thesis: (Total = 2)
Completed: Samuel Dunham (Intel);
In Progress: Clayton Faber (SIUE)

SUMMARY PROPOSAL BUDGET

YEAR 1

FOR NSF USE ONLY		
PROPOSAL NO.	DURATION (months) Proposed	Granted
AWARD NO.		

ORGANIZATION
Southern Illinois University at Edwardsville

PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR
George Engel

A. SENIOR PERSONNEL: PI/PD, Co-PI's, Faculty and Other Senior Associates (List each separately with title, A.7. show number in brackets)	NSF Funded Person-months CAL	ACAD	SUMR	Funds Requested By proposer	Funds granted by NSF (if different)
1. **George L Engel - Professor**	0.00	0.33	0.00	**4,024**	
2.					
3.					
4.					
5.					
6. (**0**) OTHERS (LIST INDIVIDUALLY ON BUDGET JUSTIFICATION PAGE)	0.00	0.00	0.00	**0**	
7. (**1**) TOTAL SENIOR PERSONNEL (1 - 6)	0.00	0.33	0.00	**4,024**	
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. (**0**) POST DOCTORAL SCHOLARS	0.00	0.00	0.00	**0**	
2. (**0**) OTHER PROFESSIONALS (TECHNICIAN, PROGRAMMER, ETC.)	0.00	0.00	0.00	**0**	
3. (**2**) GRADUATE STUDENTS				**24,000**	
4. (**1**) UNDERGRADUATE STUDENTS				**5,280**	
5. (**0**) SECRETARIAL - CLERICAL (IF CHARGED DIRECTLY)				**0**	
6. (**0**) OTHER				**0**	
TOTAL SALARIES AND WAGES (A + B)				**33,304**	
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)				**1,131**	
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A + B + C)				**34,435**	
D. EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $5,000.)					
IC Fabrication (PSD Chip) **$ 20,000**					
TOTAL EQUIPMENT				**20,000**	
E. TRAVEL 1. DOMESTIC (INCL. U.S. POSSESSIONS)				**0**	
2. INTERNATIONAL				**0**	
F. PARTICIPANT SUPPORT COSTS					
1. STIPENDS $ **0**					
2. TRAVEL **0**					
3. SUBSISTENCE **0**					
4. OTHER **0**					
TOTAL NUMBER OF PARTICIPANTS (**0**) TOTAL PARTICIPANT COSTS				**0**	
G. OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES				**2,500**	
2. PUBLICATION COSTS/DOCUMENTATION/DISSEMINATION				**0**	
3. CONSULTANT SERVICES				**0**	
4. COMPUTER SERVICES				**0**	
5. SUBAWARDS				**0**	
6. OTHER				**3,000**	
TOTAL OTHER DIRECT COSTS				**5,500**	
H. TOTAL DIRECT COSTS (A THROUGH G)				**59,935**	
I. INDIRECT COSTS (F&A)(SPECIFY RATE AND BASE)					
MTDC (Rate: 44.5000, Base: 39935)					
TOTAL INDIRECT COSTS (F&A)				**17,771**	
J. TOTAL DIRECT AND INDIRECT COSTS (H + I)				**77,706**	
K. SMALL BUSINESS FEE				**0**	
L. AMOUNT OF THIS REQUEST (J) OR (J MINUS K)				**77,706**	

M. COST SHARING PROPOSED LEVEL $ **0** AGREED LEVEL IF DIFFERENT $

PI/PD NAME
George Engel

ORG. REP. NAME*
Jerry Weinberg

FOR NSF USE ONLY		
INDIRECT COST RATE VERIFICATION		
Date Checked	Date Of Rate Sheet	Initials - ORG

 ***ELECTRONIC SIGNATURES REQUIRED FOR REVISED BUDGET**

SUMMARY PROPOSAL BUDGET

YEAR 2

FOR NSF USE ONLY		
PROPOSAL NO.	DURATION (months) Proposed	Granted
AWARD NO.		

ORGANIZATION
Southern Illinois University at Edwardsville

PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR
George Engel

A. SENIOR PERSONNEL: PI/PD, Co-PI's, Faculty and Other Senior Associates (List each separately with title, A.7. show number in brackets)	NSF Funded Person-months CAL	ACAD	SUMR	Funds Requested By proposer	Funds granted by NSF (if different)
1. **George L Engel - Professor**	0.00	0.32	0.00	**4,020**	
2.					
3.					
4.					
5.					
6. (**0**) OTHERS (LIST INDIVIDUALLY ON BUDGET JUSTIFICATION PAGE)	0.00	0.00	0.00	**0**	
7. (**1**) TOTAL SENIOR PERSONNEL (1 - 6)	0.00	0.32	0.00	**4,020**	
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. (**0**) POST DOCTORAL SCHOLARS	0.00	0.00	0.00	**0**	
2. (**0**) OTHER PROFESSIONALS (TECHNICIAN, PROGRAMMER, ETC.)	0.00	0.00	0.00	**0**	
3. (**3**) GRADUATE STUDENTS				**39,000**	
4. (**0**) UNDERGRADUATE STUDENTS				**0**	
5. (**0**) SECRETARIAL - CLERICAL (IF CHARGED DIRECTLY)				**0**	
6. (**0**) OTHER				**0**	
TOTAL SALARIES AND WAGES (A + B)				**43,020**	
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)				**1,130**	
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A + B + C)				**44,150**	
D. EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $5,000.)					
IC Fabrication (DISC Chip) $ **15,000**					
IC Fabrication (HINP Chip) **30,000**					
TOTAL EQUIPMENT				**45,000**	
E. TRAVEL 1. DOMESTIC (INCL. U.S. POSSESSIONS)				**0**	
2. INTERNATIONAL				**0**	
F. PARTICIPANT SUPPORT COSTS					
1. STIPENDS $ **0**					
2. TRAVEL **0**					
3. SUBSISTENCE **0**					
4. OTHER **0**					
TOTAL NUMBER OF PARTICIPANTS (**0**) TOTAL PARTICIPANT COSTS				**0**	
G. OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES				**3,500**	
2. PUBLICATION COSTS/DOCUMENTATION/DISSEMINATION				**0**	
3. CONSULTANT SERVICES				**0**	
4. COMPUTER SERVICES				**0**	
5. SUBAWARDS				**0**	
6. OTHER				**9,000**	
TOTAL OTHER DIRECT COSTS				**12,500**	
H. TOTAL DIRECT COSTS (A THROUGH G)				**101,650**	
I. INDIRECT COSTS (F&A)(SPECIFY RATE AND BASE)					
MTDC (Rate: 44.5000, Base: 56650)					
TOTAL INDIRECT COSTS (F&A)				**25,209**	
J. TOTAL DIRECT AND INDIRECT COSTS (H + I)				**126,859**	
K. SMALL BUSINESS FEE				**0**	
L. AMOUNT OF THIS REQUEST (J) OR (J MINUS K)				**126,859**	

M. COST SHARING PROPOSED LEVEL $ **0** AGREED LEVEL IF DIFFERENT $

PI/PD NAME
George Engel

ORG. REP. NAME*
Jerry Weinberg

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INDIRECT COST RATE VERIFICATION		
Date Checked	Date Of Rate Sheet	Initials - ORG

 ***ELECTRONIC SIGNATURES REQUIRED FOR REVISED BUDGET**

SUMMARY PROPOSAL BUDGET

Cumulative

FOR NSF USE ONLY		
PROPOSAL NO.	DURATION (months) Proposed	Granted
AWARD NO.		

ORGANIZATION
Southern Illinois University at Edwardsville

PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR
George Engel

A. SENIOR PERSONNEL: PI/PD, Co-PI's, Faculty and Other Senior Associates (List each separately with title, A.7. show number in brackets)	NSF Funded Person-months CAL	ACAD	SUMR	Funds Requested By proposer	Funds granted by NSF (if different)
1. **George L Engel - Professor**	0.00	0.65	0.00	**8,044**	
2.					
3.					
4.					
5.					
6. ( ) OTHERS (LIST INDIVIDUALLY ON BUDGET JUSTIFICATION PAGE)	0.00	0.00	0.00	**0**	
7. (**1**) TOTAL SENIOR PERSONNEL (1 - 6)	0.00	0.65	0.00	**8,044**	
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. (**0**) POST DOCTORAL SCHOLARS	0.00	0.00	0.00	**0**	
2. (**0**) OTHER PROFESSIONALS (TECHNICIAN, PROGRAMMER, ETC.)	0.00	0.00	0.00	**0**	
3. (**5**) GRADUATE STUDENTS				**63,000**	
4. (**1**) UNDERGRADUATE STUDENTS				**5,280**	
5. (**0**) SECRETARIAL - CLERICAL (IF CHARGED DIRECTLY)				**0**	
6. (**0**) OTHER				**0**	
TOTAL SALARIES AND WAGES (A + B)				**76,324**	
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)				**2,261**	
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A + B + C)				**78,585**	
D. EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $5,000.) $ **65,000**					
TOTAL EQUIPMENT				**65,000**	
E. TRAVEL 1. DOMESTIC (INCL. U.S. POSSESSIONS)				**0**	
2. INTERNATIONAL				**0**	
F. PARTICIPANT SUPPORT COSTS					
1. STIPENDS $ **0**					
2. TRAVEL **0**					
3. SUBSISTENCE **0**					
4. OTHER **0**					
TOTAL NUMBER OF PARTICIPANTS (**0**) TOTAL PARTICIPANT COSTS				**0**	
G. OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES				**6,000**	
2. PUBLICATION COSTS/DOCUMENTATION/DISSEMINATION				**0**	
3. CONSULTANT SERVICES				**0**	
4. COMPUTER SERVICES				**0**	
5. SUBAWARDS				**0**	
6. OTHER				**12,000**	
TOTAL OTHER DIRECT COSTS				**18,000**	
H. TOTAL DIRECT COSTS (A THROUGH G)				**161,585**	
I. INDIRECT COSTS (F&A)(SPECIFY RATE AND BASE)					
TOTAL INDIRECT COSTS (F&A)				**42,980**	
J. TOTAL DIRECT AND INDIRECT COSTS (H + I)				**204,565**	
K. SMALL BUSINESS FEE				**0**	
L. AMOUNT OF THIS REQUEST (J) OR (J MINUS K)				**204,565**	

M. COST SHARING PROPOSED LEVEL $ **0** AGREED LEVEL IF DIFFERENT $

PI/PD NAME
George Engel

ORG. REP. NAME*
Jerry Weinberg

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INDIRECT COST RATE VERIFICATION		
Date Checked	Date Of Rate Sheet	Initials - ORG

C ***ELECTRONIC SIGNATURES REQUIRED FOR REVISED BUDGET**

Budget Justification

	ITEM	YEAR 1		YEAR 2		TOTAL	
		NSF Request	Cost Sharing	NSF Request	Cost Sharing	NSF Request	Cost Sharing
1	G. Engel Effort	4,024	-	4,020	-	8,044	-
2	G. Engel Fringe Benefits	1,131	-	1,130	-	2,261	-
3	Graduate Student (2 students)	24,000	-	39,000	-	63,000	-
4	Undergraduate Student (1 student)	5,280	-	-	-	5,280	-
5	IC Fabrication (PSD Chip)	20,000	-	-	-	20,000	-
6	IC Fabrication (CFD Chip)	-	-	15,000	-	15,000	-
7	IC Fabrication (HINP Chip)	-	-	30,000	-	30,000	-
8	Printed Circuit Board (PCB) charges	500	-	2,000	-	2,500	-
9	Electronic Parts	1,000	-	2,500	-	3,500	-
10	Machine Shop Charges	500	-	2,500	-	3,000	-
11	Charges for Stuffing Services	1,000	-	3,500	-	4,500	-
12	Misc. Supplies	1,500	-	1,000	-	2,500	-
13	Mentor Graphics Renewal	1,000	-	1,000	-	2,000	-
14	Indirect Costs (MTDC)	17,771	-	25,209	-	42,980	-
	TOTAL	**77,706**	-	**126,859**	-	**$ 204,565**	-
	The Total Project Cost (TPC) is the sum of the last two cells in the last two columns in the last row.						

A. Senior Personnel - $8,044

Dr. George Engel, will serve as Principal Investigator for the SIUE portion of the project. Dr. Engel will be responsible for administrative oversight as well as programmatic oversight of the SIUE portion project. Dr. Engel is requesting YR1 0.33 month and YR2 0.32 of academic year salary. Salary is based upon a monthly rate of $11,840. Salary dollars include an anticipated 3% merit increase per project year. Dr. Engel will be responsible for the following programmatic aspects of the project:

- Guiding students in the design, simulation, detailed layout, testing, and documentation of new CFD integrated circuit.
- Guiding students in the design, simulation, detailed layout, testing, and documentation of modified HINP IC.
- Preparing all three ICs (PSD, HINP, and CFD) discussed in the proposal for fabrication and then ensuring that they are integrated into working chip boards for use in systems.
- Working closely with the Washington University Department of Chemistry Nuclear Reactions group to ensure that all 3 ICs meet all of the group's specifications to ensure a successful project.

B. Other Personnel - $68,280

Personnel Position	Effort/Anticipated Responsibility
Graduate Student	Dr. Engel is requesting one GA for 12 months in YR1 and 10 months in YR2. Both years will be at 50% effort. This GA will be responsible for aiding in the design, simulation, and detailed layout of the integrated circuits described in the proposal. Student will write a thesis describing design of the modified HINP IC.
Graduate Student	Dr. Engel is requesting a second GA for 12 months in YR1 and 10 months in YR2. Both years will be at 50% effort. This GA will be responsible for aiding in the design, simulation, and detailed layout of the integrated circuits described in the proposal. Student will write a thesis describing design of the CFD IC.
Graduate Student	Dr. Engel is requesting a third GA for 10 months in YR2 (50% effort). In addition to helping with IC related tasks, student will perform PCB layout and assemble the ICs onto chip boards for incorporation into systems.
Undergraduate Student	Dr. Engel is requesting one undergraduate student in YR1 for 12 months at 25% effort. This student will be responsible for helping thoroughly document the IC designs.

C. Fringe Benefits - $2,261

Fringe benefits are calculated for Dr. Engel at the current federally negotiated faculty rate of 28.1%. Student support does not include fringe benefits.

D. Equipment (>$5,000) – $65,000

The PI is requesting funds to fabricate the ICs proposed. The costs are based on recent MOSIS submissions and/or MOSIS published costs for the ON Semiconductor 0.5 micron C5N process.

Fabrication of PSD chips	$20,000	(80 chips)	YR 1
Fabrication of CFD chips	$15,000	(80 chips)	YR 2
Fabrication of HINP chips	$30,000	(160 chips)	YR 2

E. Travel – N/A

F. Participant Support Costs – N/A

G. Other Direct Costs - $18,000

1. Materials & Misc. Supplies - $6000
The PI is requesting $1,500 YR1 and $1,000 YR2 in miscellaneous supplies. Supplies include replacement of hard disk drives, monitors, plotting supplies, computer maintenance, etc. He is also requesting $1000 to purchase electronic parts during YR 1 and $2500 for parts in YR2. These components (FPGAs, op amps, reference circuits, ADCs, etc) will be used on the chip boards where the custom ICs will reside.

2. Publication Costs/Documentation/Dissemination – N/A

3. Consultant Services – N/A

4. Computer Services – N/A

5. Subawards – N/A

6. Other - $12,000
The PI is requesting services of Mentor Graphics Software License Renewal ($1000 per year) for both YR1 and YR2 of the project. These services are for renewal of a license for software (Calibre) that allow us to verify that the IC layout meets all design rules and that the layout netlists match the electrical schematics.

In order to assemble the fabricated ICs into working systems he is seeking funds to create printed circuit boards (PCBs), $500 for YR1 and $2000 for YR2. Moreover, funds of $500 YR1 and $2500 YR2 are requested for the services of a machine shop. Finally, funds for stuffing services (from Pico Systems) for the PCBs ($1000 in YR1 and $3500 in YR2) are also being sought.

H. Total Direct Costs – $161,585

I. Total Indirect Costs - $42,980
Indirect costs are calculated on a modified total direct cost ($96,585) at the current federally negotiated rate of 44.5%. Cognizant Agency: DHHS.

J. Total Direct & Indirect Costs - $204,565

Current and Pending Support

(See PAPPG Section II.C.2.h for guidance on information to include on this form.)

The following information should be provided for each investigator and other senior personnel. Failure to provide this information may delay consideration of this proposal.

Investigator: George Engel

Other agencies (including NSF) to which this proposal has been/will be submitted.

Support: ☐ Current ☒ Pending ☐ Submission Planned in Near Future ☐ *Transfer of Support

Project/Proposal Title: **This Proposal** MRI: Development of ASIC's Suite for Analog Processing of Signals from Large Arrays of Silicon-Strip Detectors and PSD-Capable Scintillators

Source of Support: National Science Foundation

Total Award Amount: $ 204,565 Total Award Period Covered: 08/01/16 - 07/31/18

Location of Project: Southern Illinois University Edwardsville

Person-Months Per Year Committed to the Project. Cal:0.00 Acad: 0.33 Sumr: 0.00

Support: ☐ Current ☐ Pending ☐ Submission Planned in Near Future ☐ *Transfer of Support

Project/Proposal Title:

Source of Support:

Total Award Amount: $ Total Award Period Covered:

Location of Project:

Person-Months Per Year Committed to the Project. Cal: Acad: Sumr:

Support: ☐ Current ☐ Pending ☐ Submission Planned in Near Future ☐ *Transfer of Support

Project/Proposal Title:

Source of Support:

Total Award Amount: $ Total Award Period Covered:

Location of Project:

Person-Months Per Year Committed to the Project. Cal: Acad: Sumr:

Support: ☐ Current ☐ Pending ☐ Submission Planned in Near Future ☐ *Transfer of Support

Project/Proposal Title:

Source of Support:

Total Award Amount: $ Total Award Period Covered:

Location of Project:

Person-Months Per Year Committed to the Project. Cal: Acad: Sumr:

Support: ☐ Current ☐ Pending ☐ Submission Planned in Near Future ☐ *Transfer of Support

Project/Proposal Title:

Source of Support:

Total Award Amount: $ Total Award Period Covered:

Location of Project:

Person-Months Per Year Committed to the Project. Cal: Acad: Summ:

---

*If this project has previously been funded by another agency, please list and furnish information for immediately preceding funding period.

8) FACILITIES, EQUIPMENT AND OTHER RESOURCES

The computing facilities in the IC Design Research Laboratory at SIUE consist of five workstations running Centos 6 Linux for Workstations. The workstations are equipped with two 19-inch monitors. A sixth computer operates as a file server.

All workstations run state-of-the-art computer-aided design software. This includes a complete suite of the Cadence IC design tools and MATLAB.

The lab also has a PC running Microsoft Windows which is used for FPGA development and for document preparation. In addition to standard test equipment, the lab has access to the following:

- Agilent E4402B Spectrum Analyzer
- Agilent 8648 Signal Generator
- HP/Agilent 54833A 1GHz 2CH 4GSamples/s Infiniium Oscilloscope
- TDS420A Oscilloscope, 4 Channel, 200 MHz, 100 MS/s, Includes XL Option: 120K Memory, FFT, Math
- Surface mount assembly station and stero microscope for constructing/repairing printed circuit boards.
- A small pick and place machine
- A wide variety of state-of-the-art FPGA (Xilinx and Altera) development boards.

Data Management Plan

I. Expected Data

The project will generate several different types of data. These include

1. MATLAB Code / Simulation Results
2. MathCAD Design Sheets
3. VerilogA Code / Simulation Results
4. Simulation scripts
5. Design Data (Cadence) / Simulation Results
6. Documentation in terms of a series of interim reports culminating in two student Masters Theses.

II. Data Format

The design of the ICs will be conducted using Cadence IC Design Software (Version 5). All design data (schematics and layout) will be in standard Cadence design formats. In order, to make the design more accessible, all schematics will be converted to PDF prior to posting to the WEB. All technical documentation will be prepared using Microsoft Office products and/or Latex.

III. Access to Data and Data Sharing Practices and Policies

1. During the active design periods, our group will (as we have in the past) get together biweekly with our colleagues at Washington University with the intervening weeks serviced by a SKYPE conversation. Every other month, a note will go out to all potential users, inviting them to join the SKYPE meeting. Such meetings will be preceded by an agenda and a file containing the results to be discussed.

2. A WEB (http://www.siue.edu/~gengel/) site will contain all interim reports describing circuit operation and chip simulation results (supplied by the PI, G. Engel) along with PDF versions of all circuit schematics. Student theses will also be posted to this site. A second site (http://pages.wustl.edu/jelson) will contain the actual chip testing results (supplied by J. Elson at Washington University). All potential future users will be prompted by an email when new results are available. These announcements will be linked to the open SKYPE meetings. The CFD chip design and simulation effort will be the basis of an MS thesis as will the design and simulation of the modified HINP-d IC. These theses will be the ultimate repository for the simulation results and the detailed layout of the generated designs. These will be downloadable from the Prof. Engel's website. The details of the design and chip testing results will also be presented in Nucl. Instru. and Meth. papers. These practices are standard for our collaboration.

3. As we have done for our previous development projects, we (along with our colleagues at Washington University) will host demonstration and testing sessions. (In the past groups

from MSU, ORNL, TAMU, FSU and LSU have attended these sessions.) We anticipate two such sessions, one for CFD and PSD in the middle of the second year, and the second – for HINP-d at the end of this grant.

IV. Policies for Re-use, Re-distribution

There will be no disclaimers or restrictions regarding the data available on the website. The actual Cadence design databases will not be available on the WEB, but we are willing to make the Cadence design databases available to others upon request.

V. Archiving of Data

All design data will be archived on several hard drives. The design databases and all relevant documentation will be archived on both the SIUE IC Design Research Laboratory file server as well as the SIUE ECE departmental server. Also, at the end of the project, all design databases, documentation, etc. will also be archived on a file server residing at Washington University (Chemistry, Nuclear Reactions Group).

SOUTHERN ILLINOIS UNIVERSITY
EDWARDSVILLE

January 8, 2016

Dr. Randy Phelps
National Science Foundation
4201 Wilson Boulevard
Arlington, VA 22230

Dear Dr. Phelps,

I am writing on behalf of Southern Illinois University Edwardsville and in support of the proposal titled, "MRI: Development of ASIC's Suite for Analog Processing of Signals from Large Arrays of Silicon-Strip Detectors and PSD-Capable Scintillators." The application by PI George Engel represents the development for three chips that will allow many groups across the nation to field, in a cost effective manner, large arrays of Si-strip detectors and scintillators.

Almost all fields of modern contemporary physics stand on the shoulders of cutting edge engineering. This has been the case in nuclear physics since E. O. Lawrence. Over the past decade Prof. Engel has greatly advanced analog pulse processing for studies of exotic nuclei, and this proposal seeks to build on, and greatly advance, this effort. The development he proposes is vital if the nation is to make optimal use of the recently approved FRIB (Facility for Rare Isotope Beams) project, a nearly ¾ of a billion dollar national investment. The beam time at this facility must be optimally employed and this calls for large and complicated detectors that in turn require optimized – and affordable – electronics. Prof. Engel's effort, and this proposal in particular, is perfectly tailored to this engineering-physics need. For this reason the University is committed to, and excited about, supporting this interdisciplinary effort.

Southern Illinois University Edwardsville is looking forward to the innovative and collaborative opportunities made possible through the development of the ASIC's suite and is committed to ensuring its successful deployment in front-line nuclear physics experiments.

Best Regards,

Jerry B. Weinberg

Jerry B. Weinberg
Associate Provost for Research &
Dean of the Graduate School for Stephen Hansen, Interim Chancellor

MRI Awards Made to Southern Illinois University Edwardsville in the Last Five Years

Project PI: Christopher Gordon
Award Cycle: MRI 2011
Award Title: MRI: Acquisition of a 3D Laser Scanner to Support Multi-Disciplinary Research in Data-Driven Management of Cultural, Physical, and Biological Resources
Award Amount: $100,000
Project period: Sept. 1 2011 – Aug. 31, 2012.
Status: Leica C10 Laser scanner and Polyworks modeling software were procured during this time period. Final project report was submitted November 30, 2012 and approved December 20, 2012. Three senior design projects have been completed using the scanner and software to date. The scanner has been incorporated into CNST 484: Surveying Computations and Applications, and has been demonstrated in ANTH 475: Archeology Field School.
FINAL REPORT SUBMITTED: 11/30/2012

Project PI: Sohyung Cho
Award Cycle: MRI 2010
Award Title: MRI: Acquisition of Major Components Required for Constructing Supply Chain Test-Bed
Award Amount: $192,844
Project period: Sep. 1, 2010 – Aug. 31, 2011.
Status: All portions of the equipment list have been ordered and received as of current date. The system is currently used in various courses in Industrial and Manufacturing Engineering Program and is a key resource in student theses and research. The grant was closed in November 2011. Presentations about this system have been given at two conferences since that time. The system is currently used as a whole or components for student and industry projects. In addition, the PI is in discussion with a local industry (Continental Tire) for the use of the developed system to test the operating policies of their manufacturing facility.
FINAL REPORT SUBMITTED: 10/20/2011

Project PI: Julie Holt
Award Cycle: MRI-R²
Award Title: ARRA: MRI-R2: Acquisition of Raman and Infrared Microscopes for Interdisciplinary Research
Award Amount: $572,417
Project period: Feb. 15, 2010 – May 2, 2013
Status: In spring of 2011, instruments from Bruker, Co. were delivered and installed; preliminary training was given on campus. PI Holt went to Bruker for additional training in December 2012, and Bruker will return to campus for further training. Instruments are used to characterize materials in research projects by faculty and students. Holt's sabbatical research in fall of 2012 focused on using IR to characterize archaeological Native American ceramics from Illinois. Interim reports were submitted in 2011 and 2012.
FINAL REPORT SUBMITTED: 04/30/2013

Washington University in St. Louis
ARTS & SCIENCES
Department of Chemistry

Jan. 11, 2016

To: NSF MRI Coordinator:

By signing below I acknowledge that I am listed as a collaborator of the MRI proposal, entitled "**Development of ASIC's Suite for Analog Processing of Signals from Large Arrays of Silicon-Strip Detectors and PSD-Capable Scintillators**," with Prof. George Engel as the Principal Investigator. I agree to undertake the tasks assigned to me, as described in the proposal, and I commit to provide or make available the resources therein designated to me.

Lee G. Sobotka Jan. 11, 2016
Washington University

Washington University in St. Louis, Campus Box 1134, One Brookings Drive, St. Louis, Missouri 63130-4899
Department Phone: (314) 935-6530 Fax: (314) 935-4481 http://www.chemistry.wustl.edu

SOUTHERN ILLINOIS UNIVERSITY
EDWARDSVILLE

To: NSF MRI Coordinator

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By signing below I certify that Southern Illinois University Edwardsville is classified as a non-Ph.D.-granting as defined in Section IV of the MRI solicitation.

Signed: Jerry B. Weinberg Print Name: Jerry B. Weinberg

Title of Signatory: Associate Provost for Research & Dean of the Graduate School for Stephen Hansen, Interim Chancellor

Date: 1/5/16