SINGLE-TO-DIFFERENTIAL BUFFER AMPLIFIER

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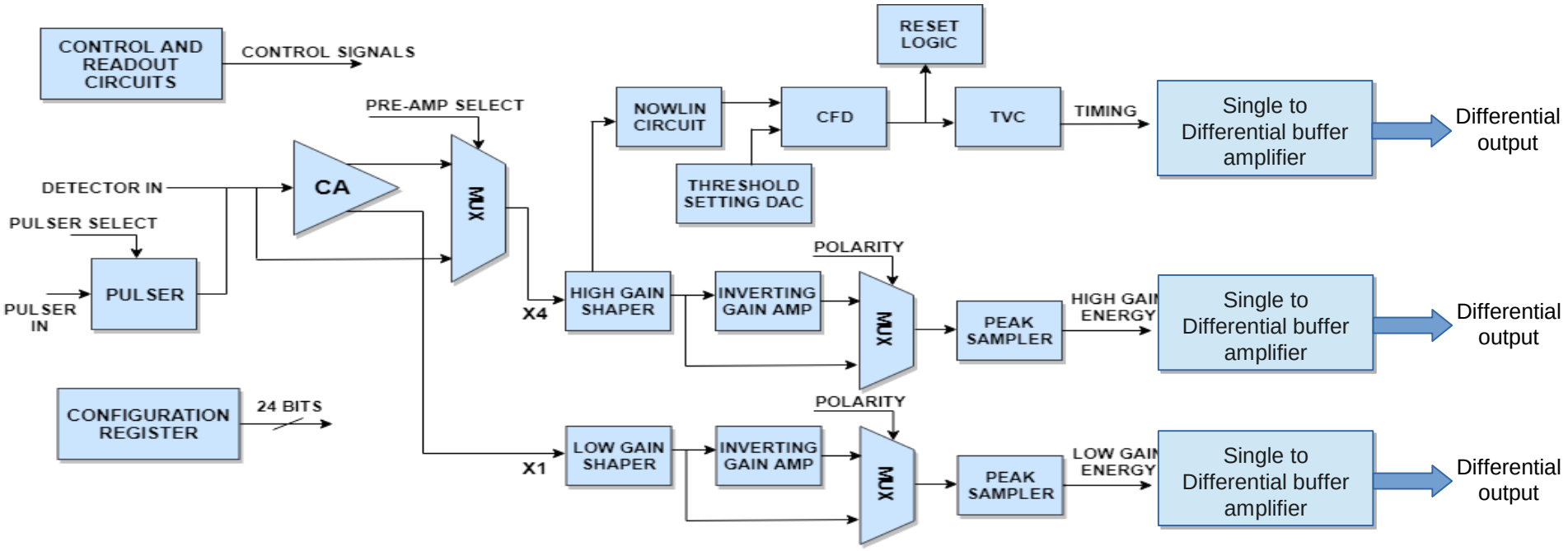
Introduction

The HINP16C chip produces sparsified analog pulse trains for both linear (pulse height) and timing (relative to an external reference) and allows the user to choose one of the two internal gains. The chip may also be used with an external amplifier.



SINGLE-TO-DIFFERENTIAL BUFFER AMPLIFIER

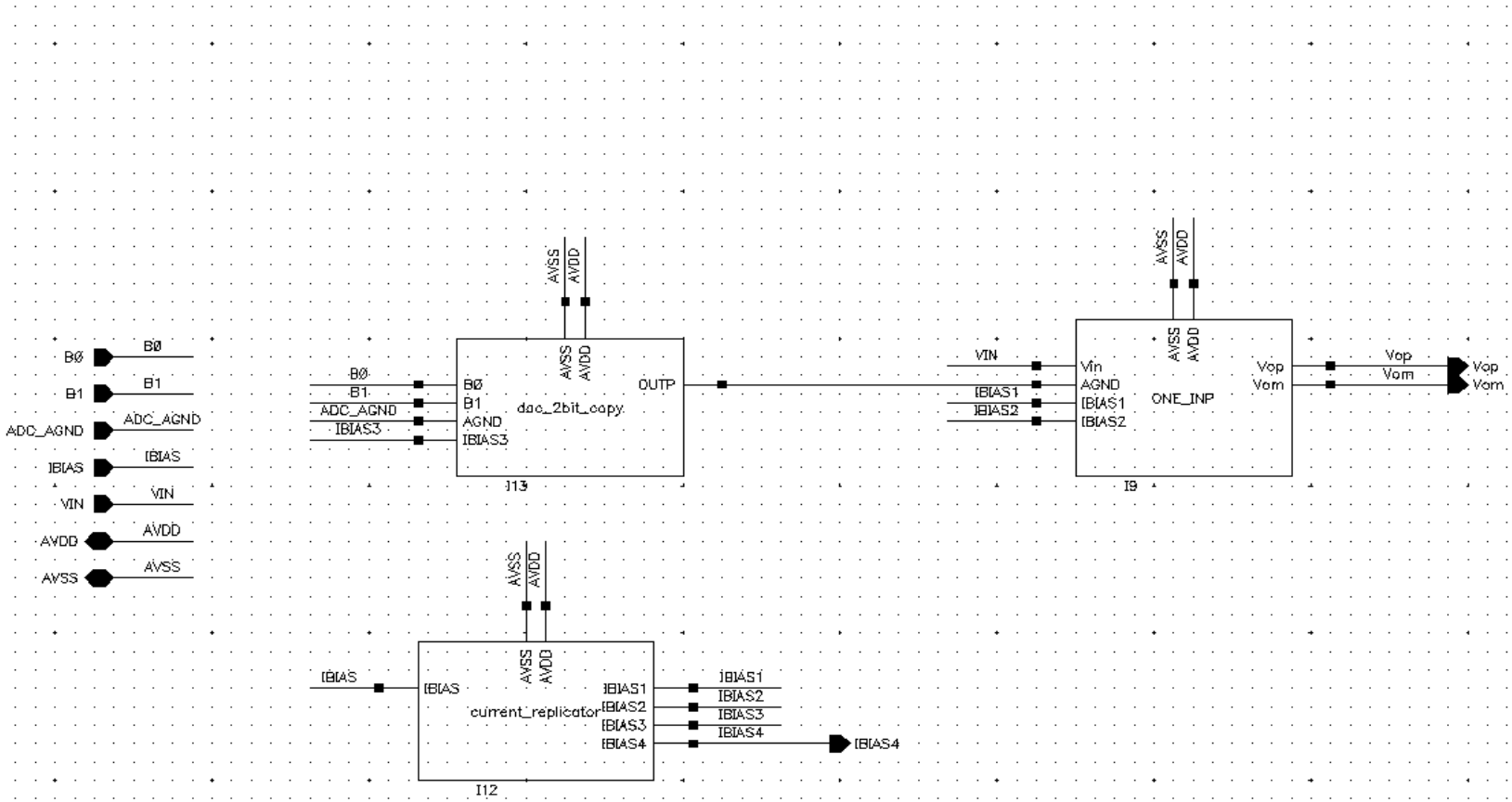
- This single ended input to differential output circuit converts a single ended input of +1.65V which decreases by 100mV every time period of 200μs into a differential output of 0V to 3.3V on a single +3.3V supply.

- The circuit is composed of two amplifiers.

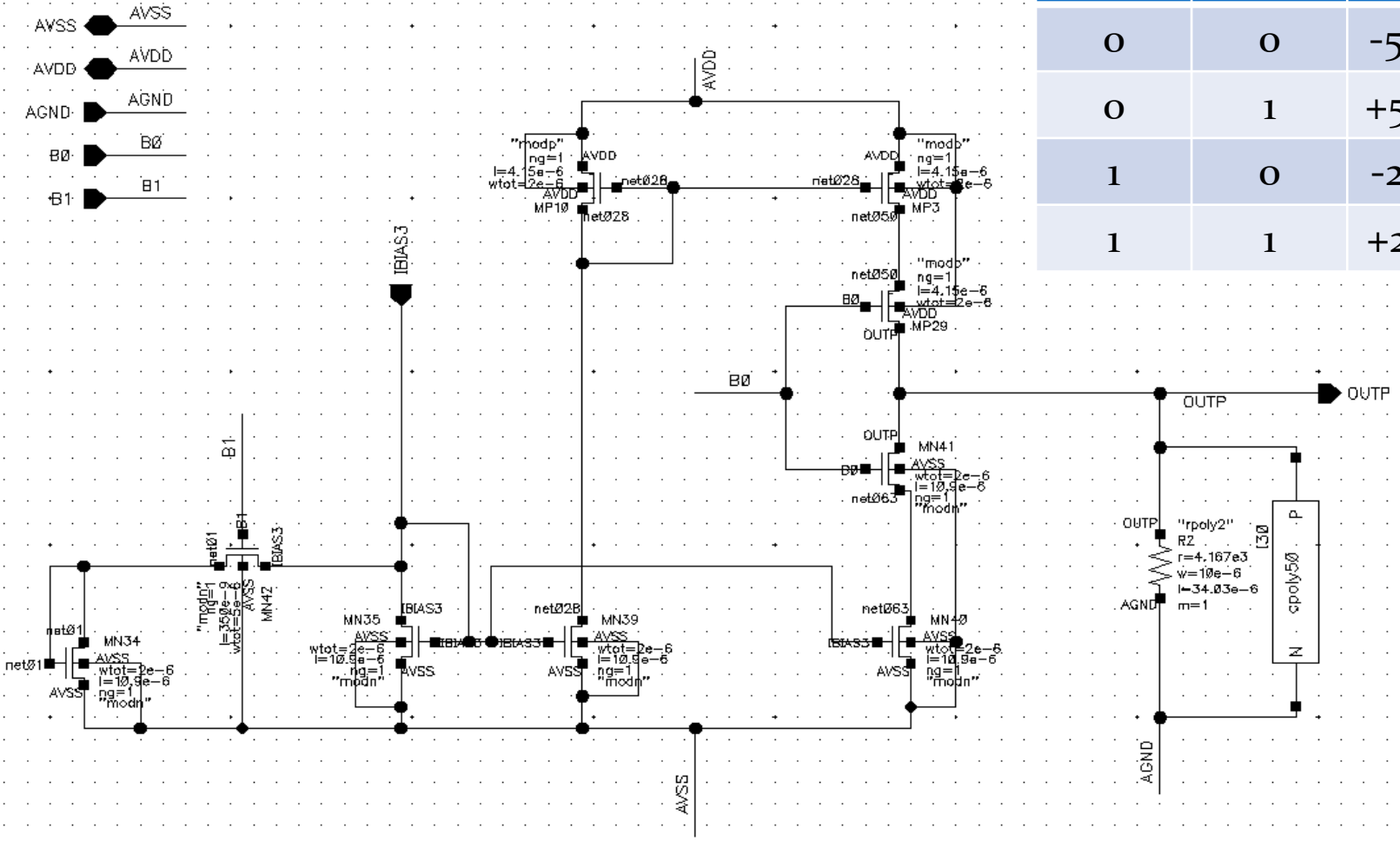
- One amplifier acts as a buffer and creates a voltage, Vout+. The second amplifier inverts the input and adds a reference voltage to generate Vout-. Both Vout+ and Vout- range from 0V to 3.3V.

- The difference, Vdiff, is the difference between Vout+ and Vout-. This makes the differential output voltage range +3.3V.

ADC Buffer Block with Detail View

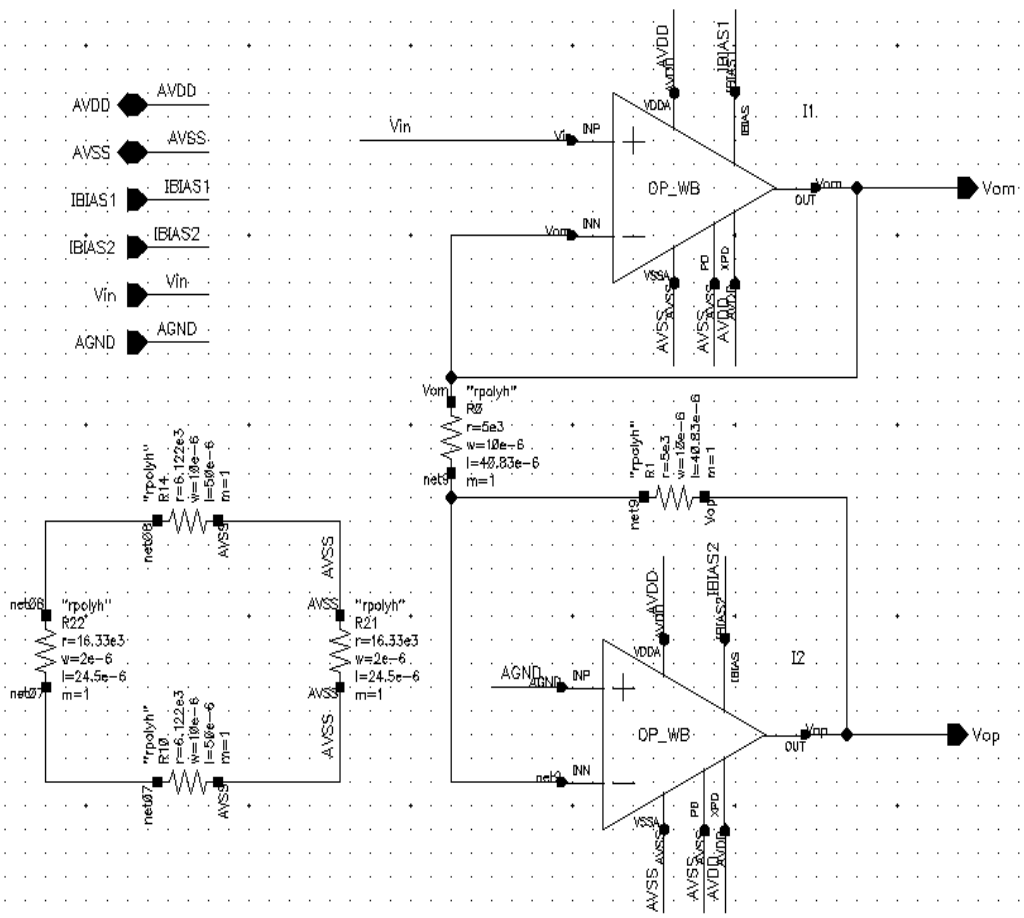


DAC 2 Bit Schematic

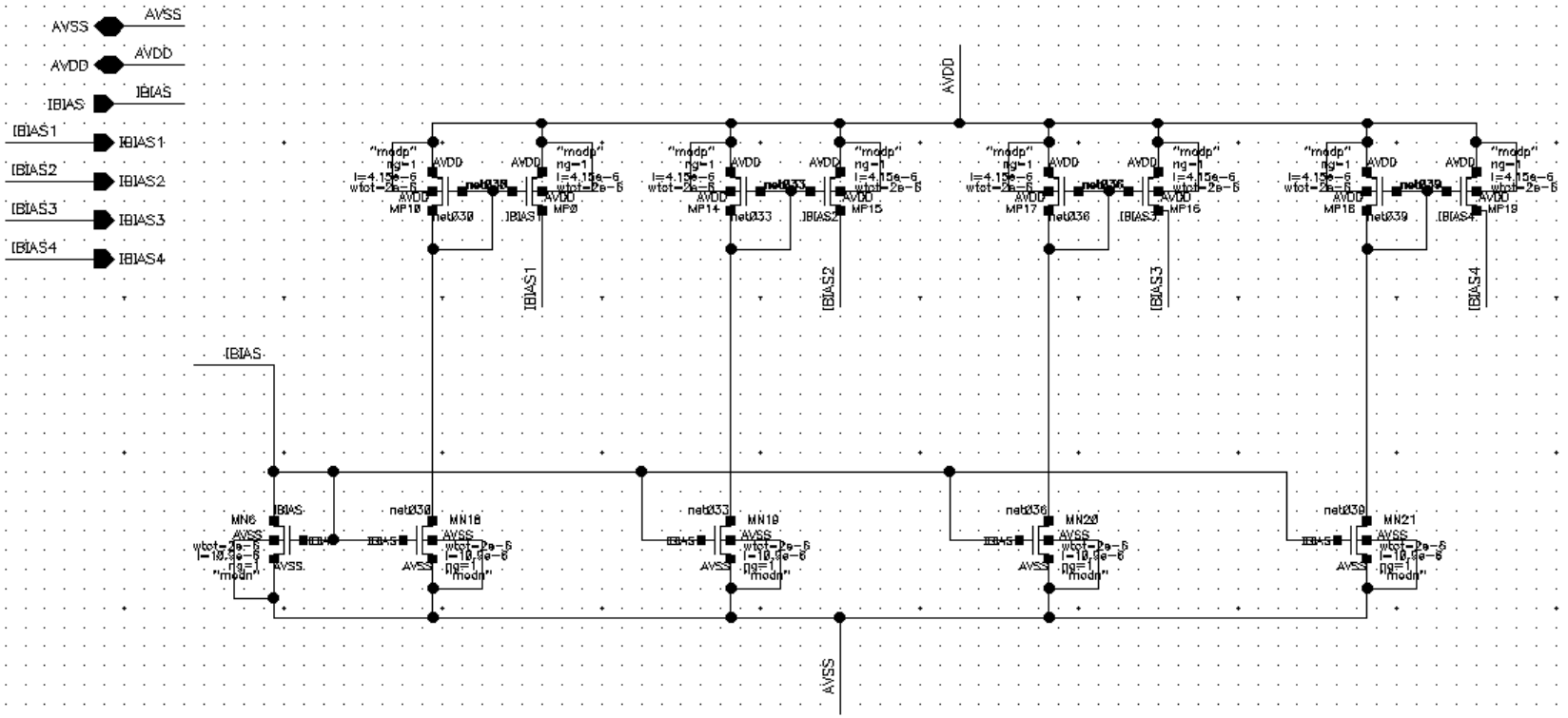


B1	Bo	Out
0	0	-50mv
0	1	+50mv
1	0	-25mv
1	1	+25mv

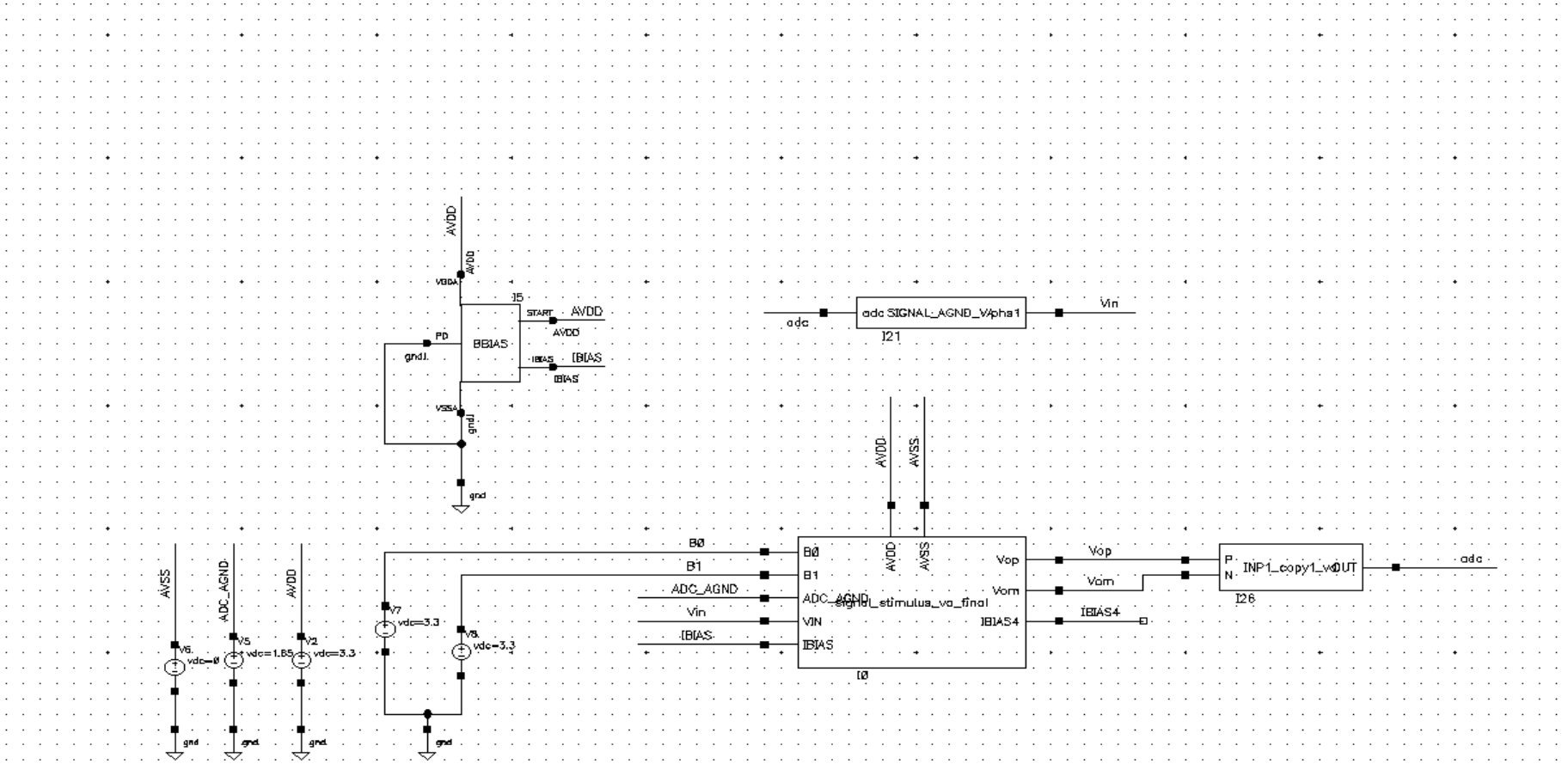
Differential Output Schematic



Current Replicator Schematic

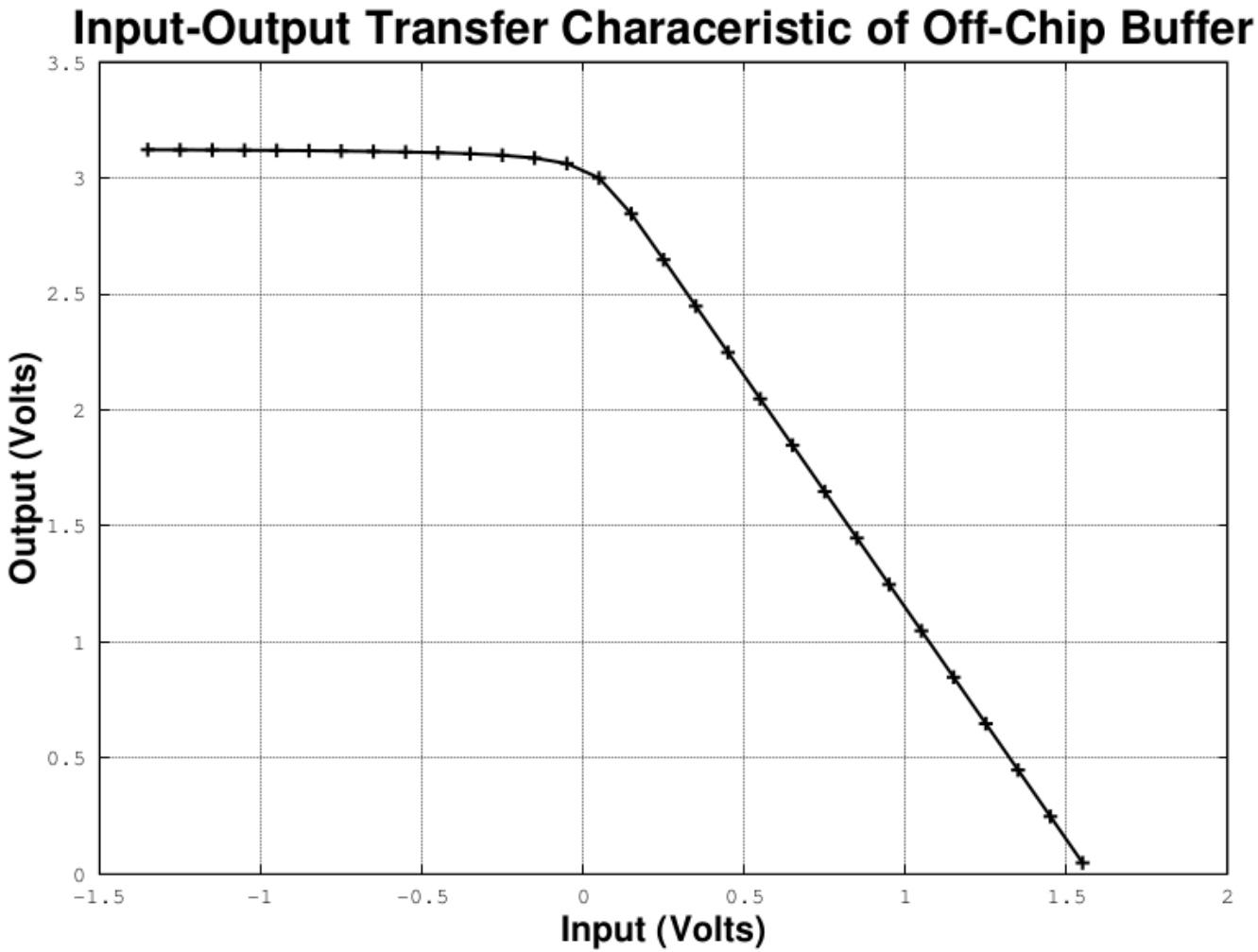


ADC Buffer Block Test Bench

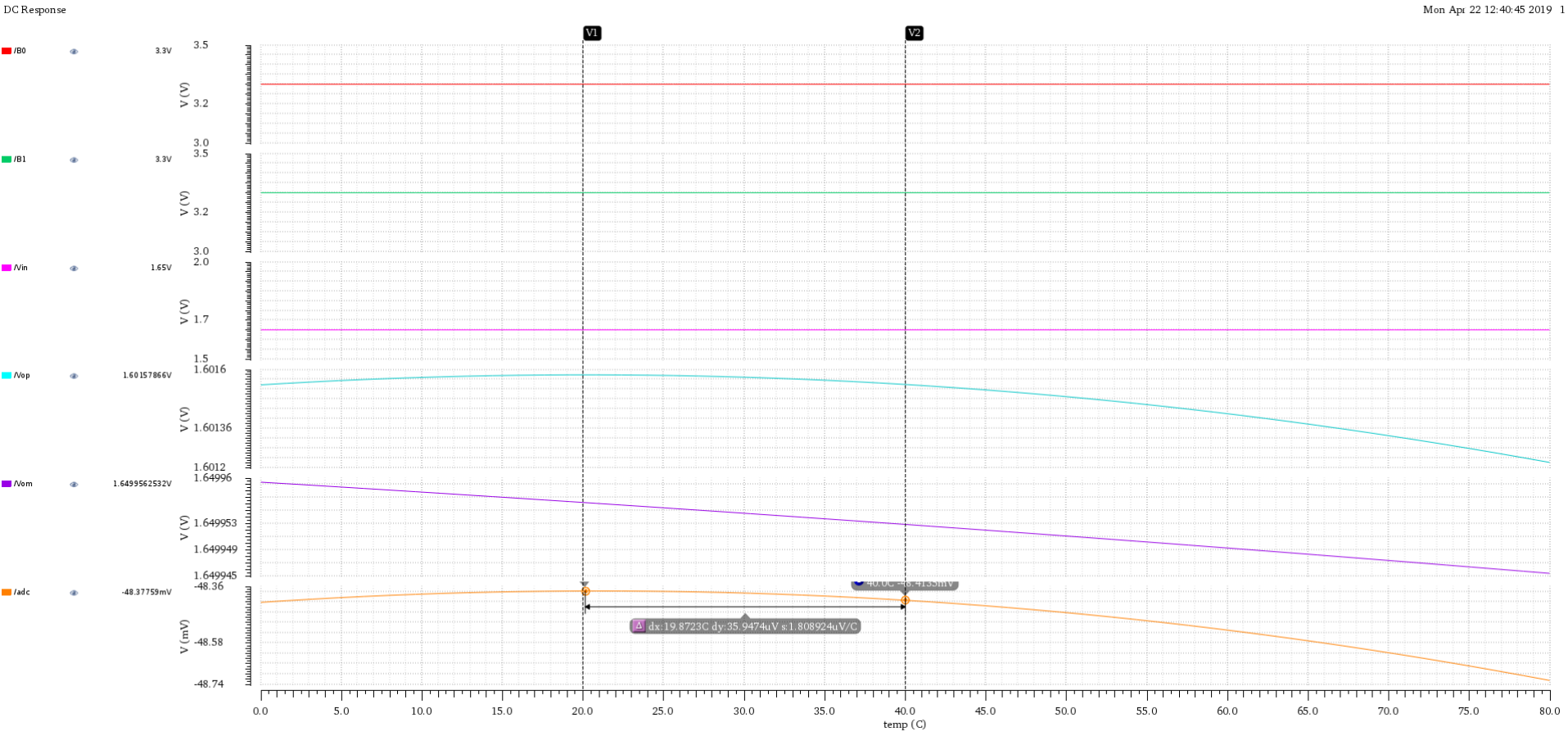


Transient Output

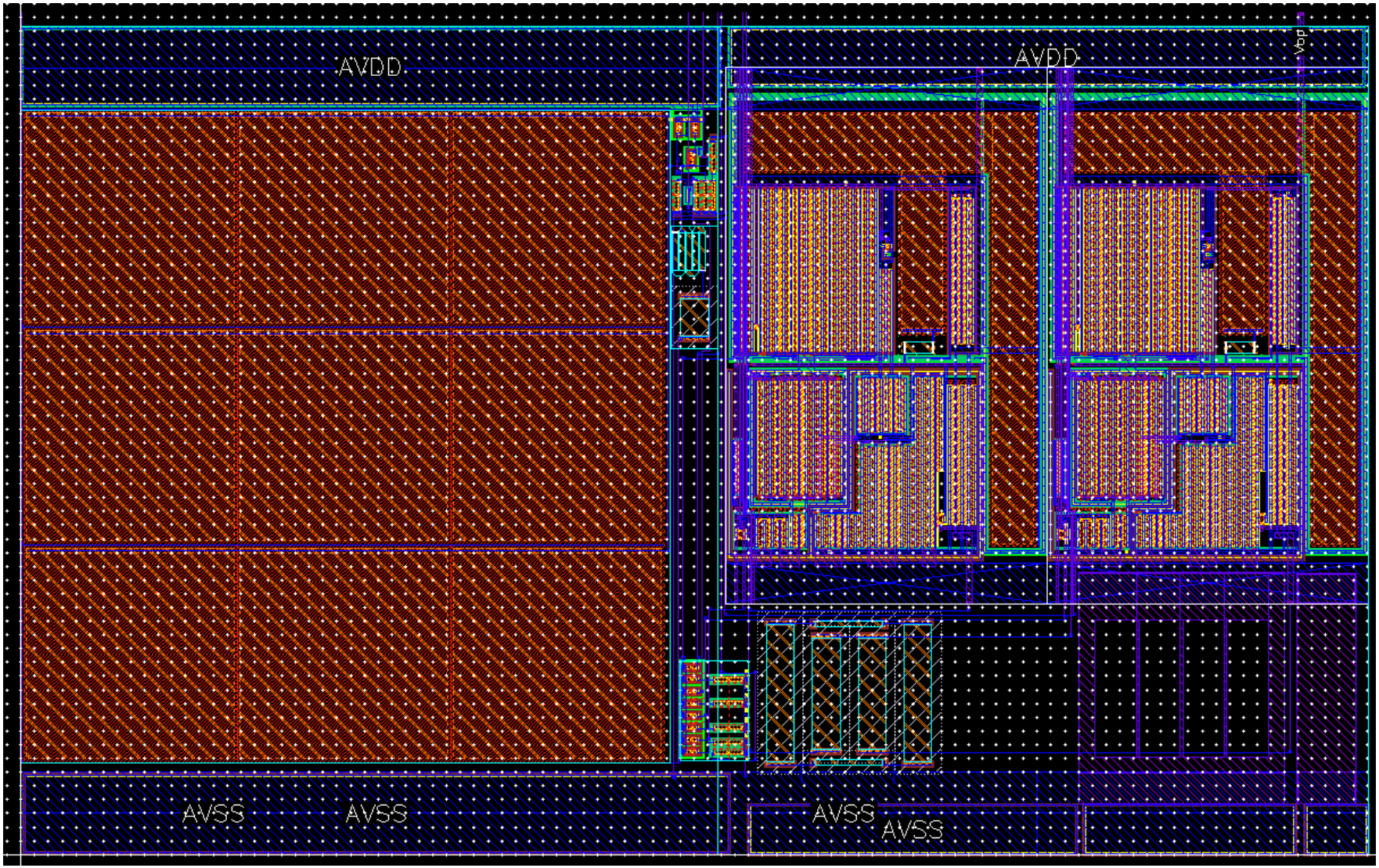
Linearity plot



Temperature Plot



Layout



Conclusion

- Designed a DAC to generate ± 50 mV and ± 25 mV such that the output is always +ve because the ADC in HINP16 cannot take the -ve output values .
- Designed a differential output block to make sure the output is within required bounds.
- Designed a current BIAS replicator with 4 outputs of 12 µA each.
- A Verilog-A block is designed to generate the incremental step output with 100mV every time period.
- A Verilog-A block is used to sum the two outputs of the differential block to determine the linearity.
- Octave is used to plot the linearity of the output.
- The total integrated noise is 77 µV.
- The voltage change with respect to temperature is 1.8 µV/°C.
- A layout was designed with in the required dimensions where common channel has a width of 241.5 µm (excluding AVDD and AVSS rails) and length being 490.6 µm.

QUERIES ?

THANK YOU