MRI (# 1625499) : Development of Auto Reset Circuit for Signal Channel for HINP Chip

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Table of Contents

Introduction

- Each strip is a p-n reverse biased junction
- Segmented in square strips, each strip has 32 silicon detectors (16 horizontal and 16 vertical)
- To measure the energy of the charged particle being hit

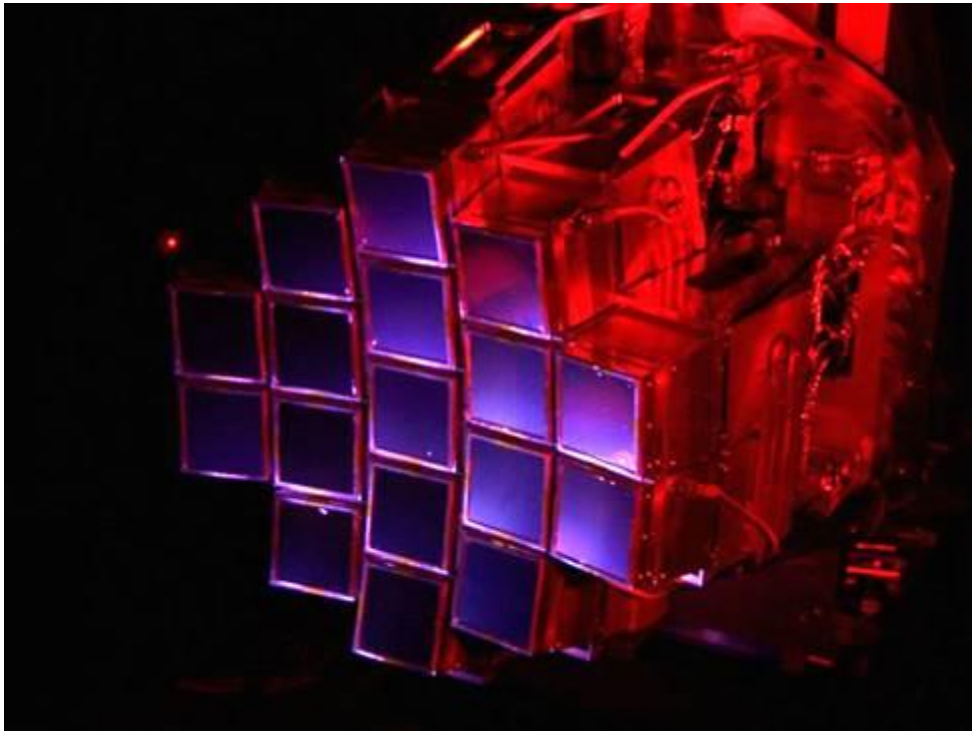


Fig.1 HiRA (High resolution Array)

Why do we need auto reset ?

- Data sparsification
- When we are looking for particular events to read out

When do we need auto reset ?

- Multiplicity output helps physicists whether to read the data out or not
- To reset all analog circuits automatically when take_event signal is not asserted

Why do we need variable delay widths ?

- Widely variable delay pulse to allot time for physicists to decide whether to read out the data or not

Working:

- The auto reset generation block produces a time-out pulse of programmable width/delay (supports 16 different programmable delays).
- The input reference current of 12 µA is divided down to produce different pulse width when the qualified CFD narrow pulse fires.

Block Diagram

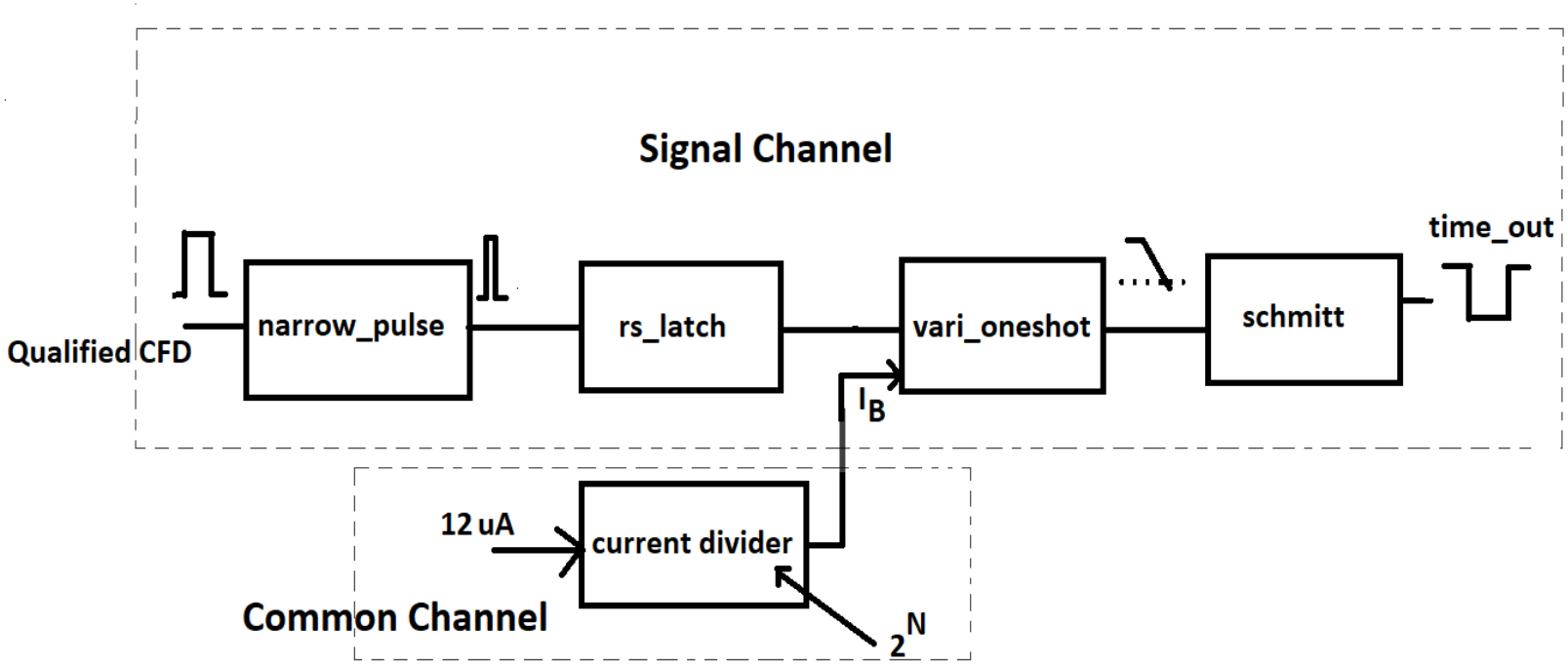


Fig.2 Block diagram of auto reset circuit

Circuit Diagrams

Zero Temperature coefficient Current Library

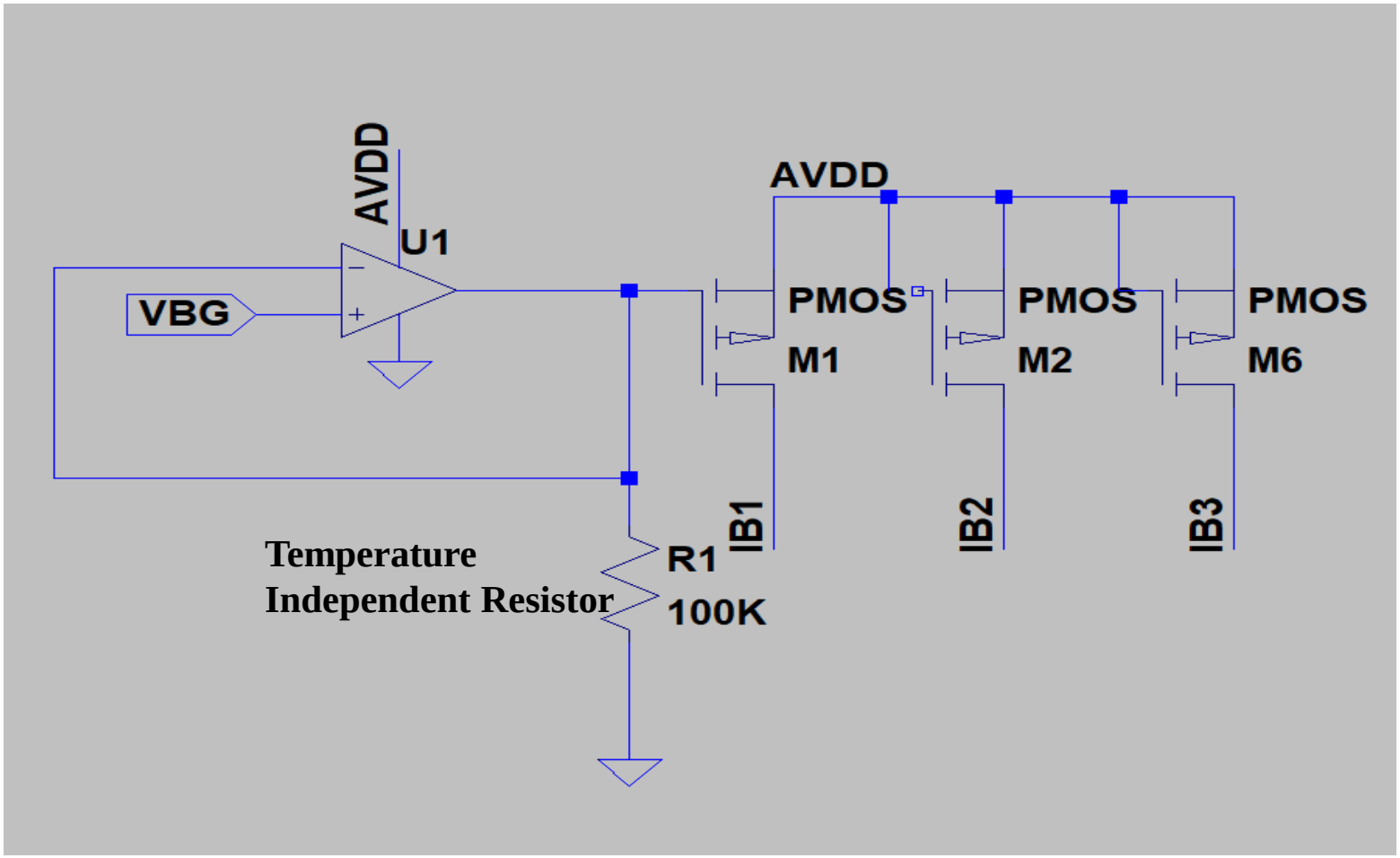


Fig. 3 Circuit Diagram for ZTC

Current divider in Common Channel

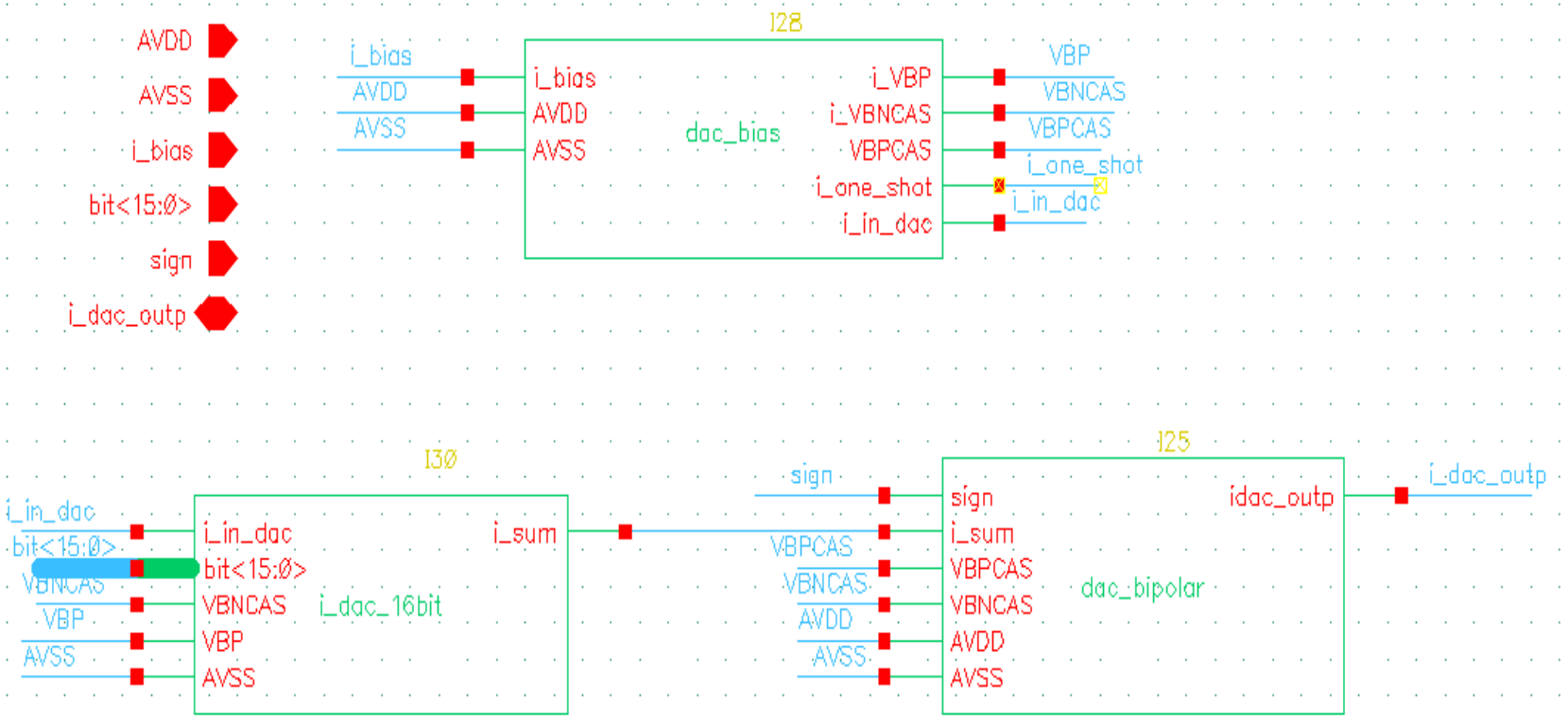
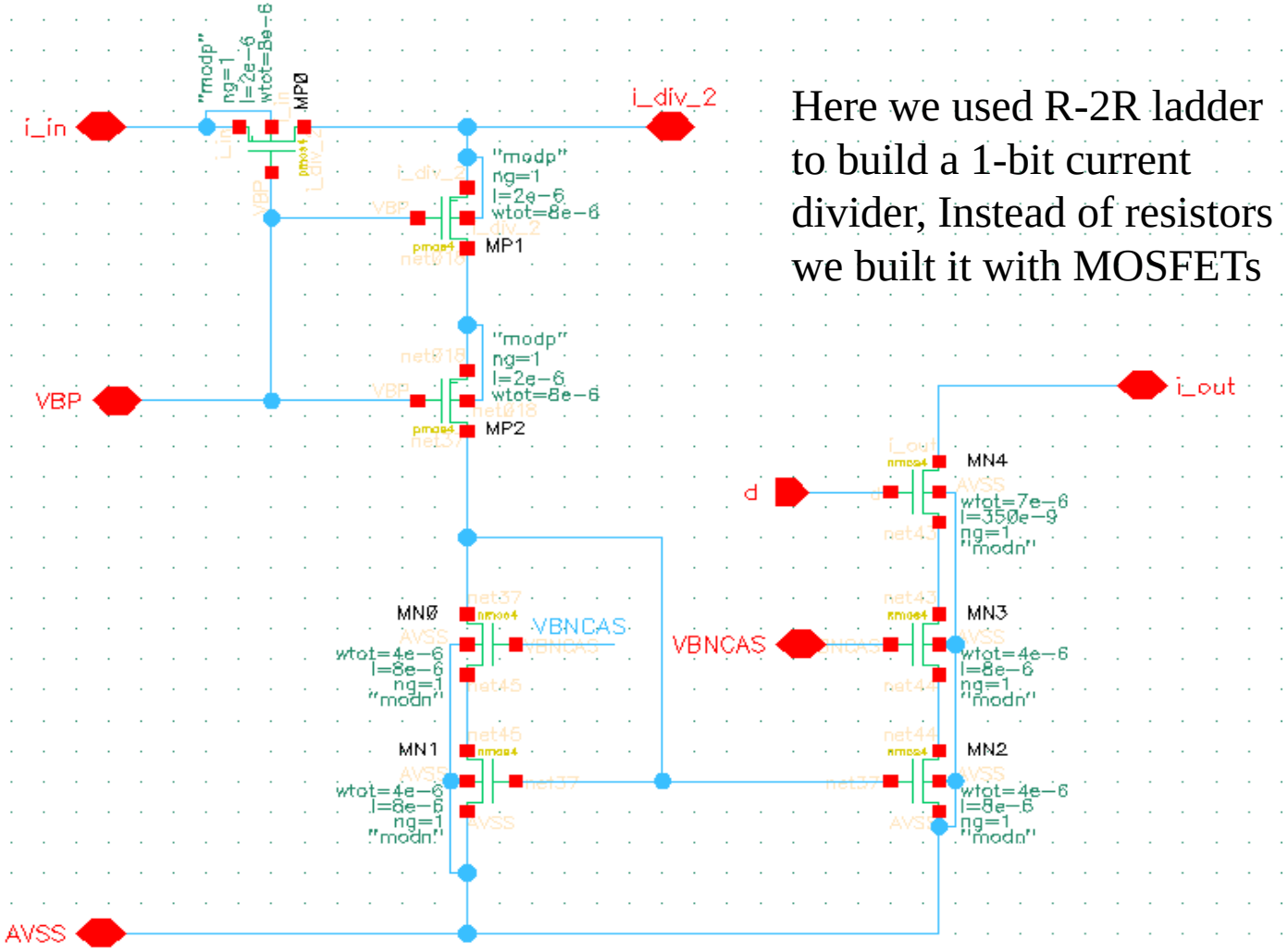


Fig. 4 Circuit diagram for auto reset current divider in Common Channel



Here we used R-2R ladder to build a 1-bit current divider, Instead of resistors we built it with MOSFETs

Fig. 5 Circuit diagram of 1-bit Current divider

Auto Reset Circuit in Signal Channel

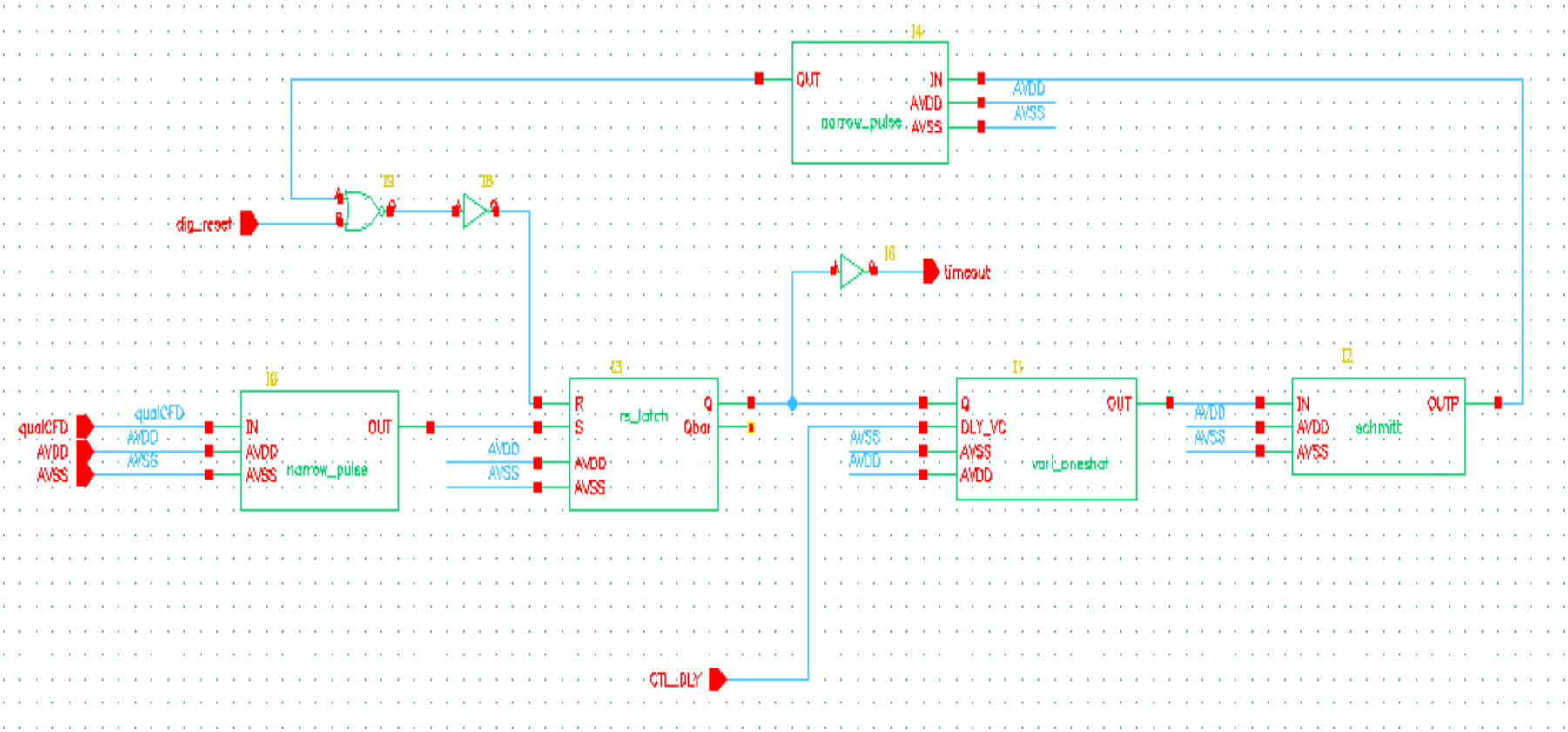


Fig.6 Circuit Diagram for auto reset Circuit in Signal Channel

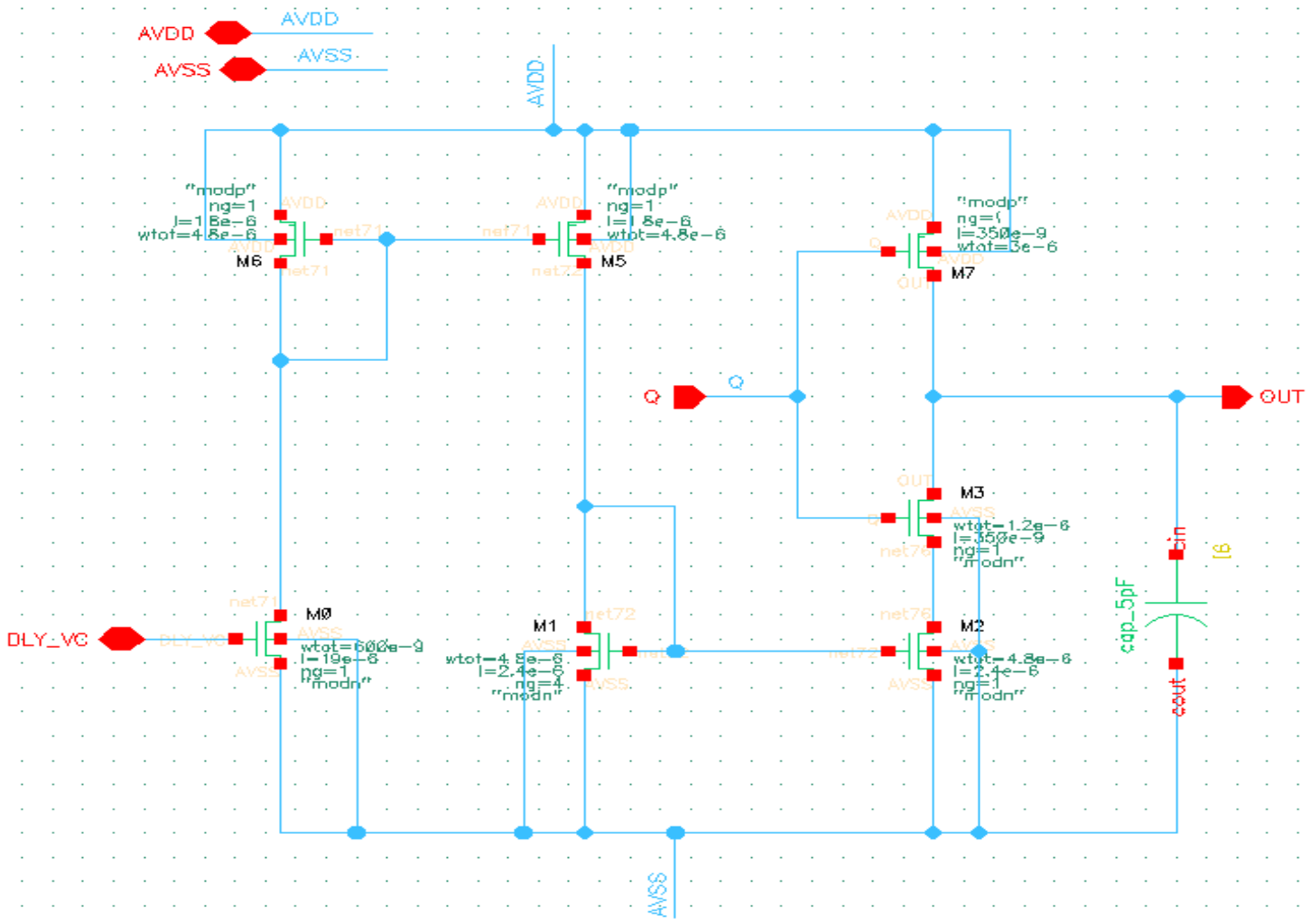


Fig.7 Circuit diagram of vari-oneshot circuit

Test Bench

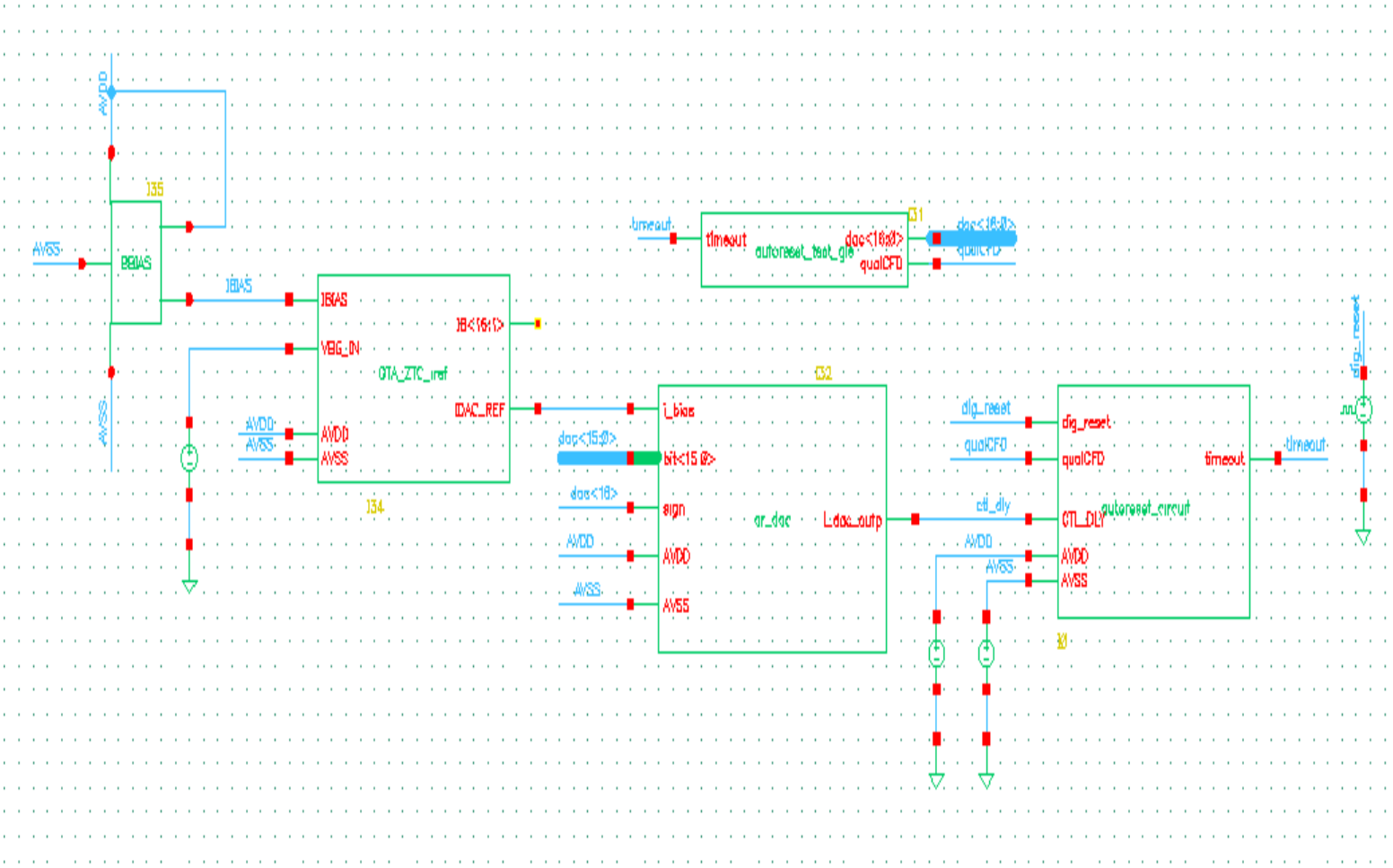
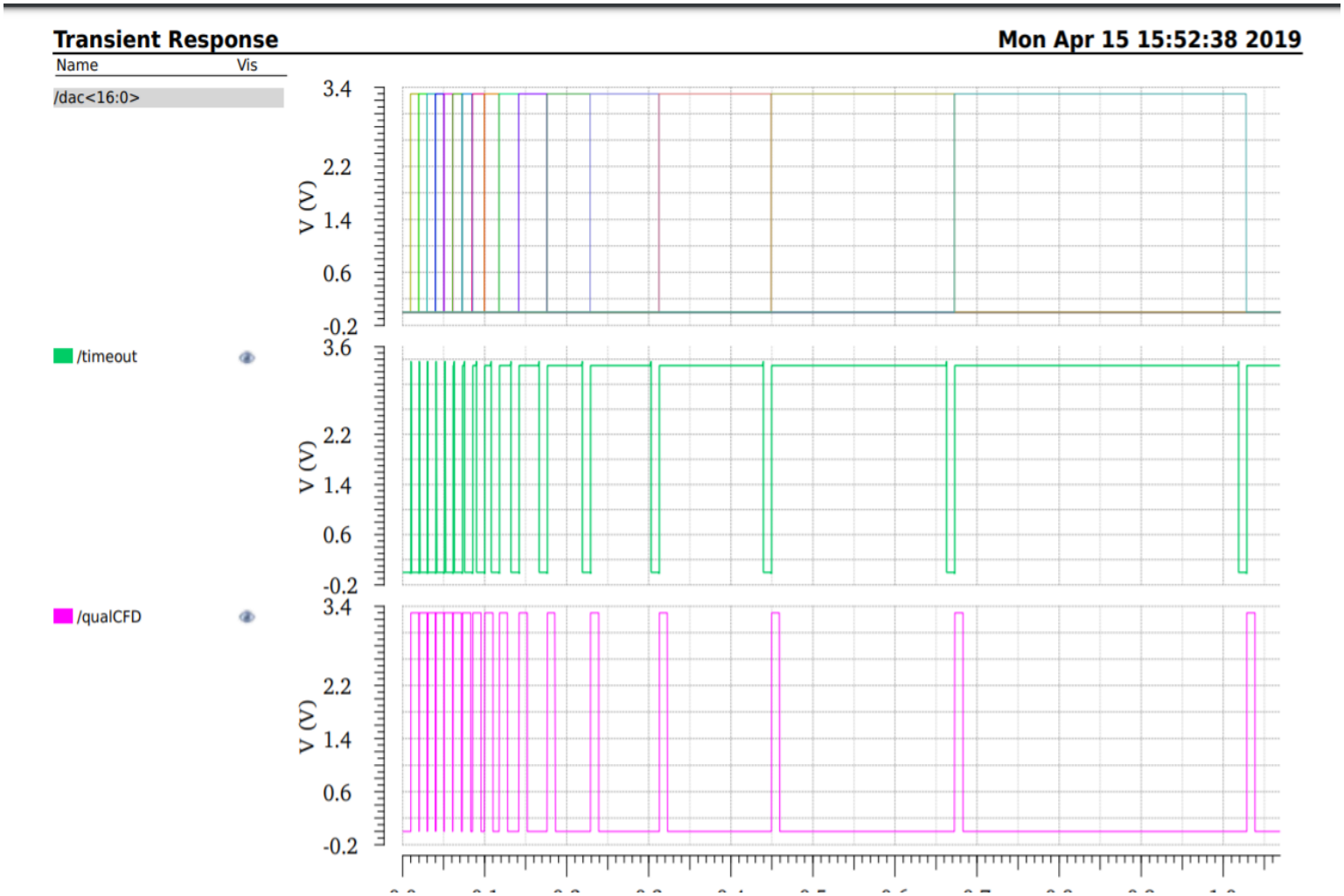


Fig.8 Test Bench for Auto reset Circuit

Simulation Results



Digital bit v/s Timeout

Digital Bit	Time Out
0000	1.3 µs
0001	1.9 µs
0010	3.8 µs
0011	7.9 µs
0100	15.1 µs
0101	30 µs
0110	57.4 µs
0111	109 µs

Digital Bit	Time Out
1000	207 µs
1001	394 µs
1010	748 µs
1011	1.42 ms
1100	2.7 ms
1101	5 ms
1110	9.2 ms
1111	16.1 ms

Linearity Plot

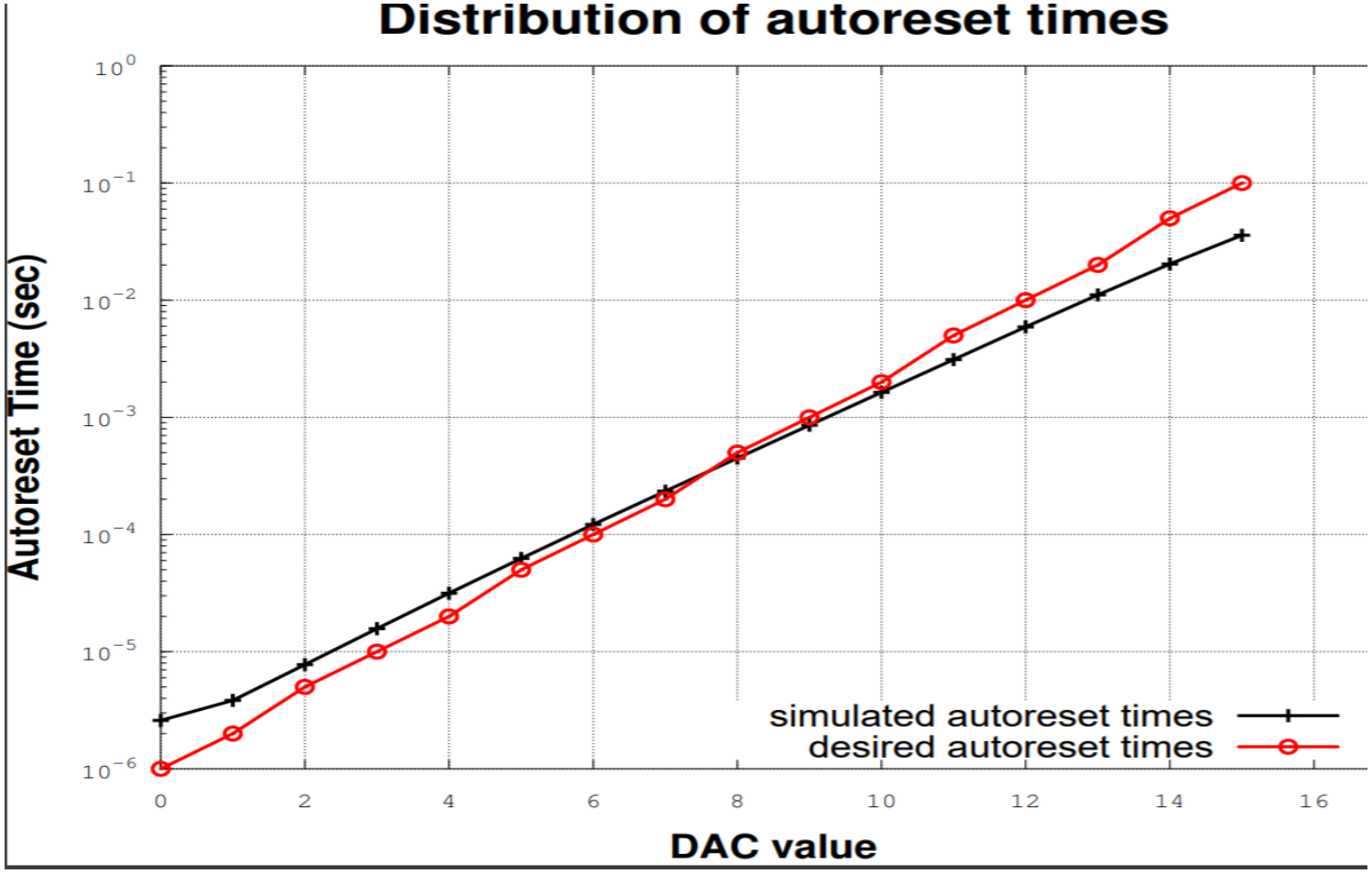


Fig. 9 Linearity plot of the time-out pulse

Layout

In Common channel:

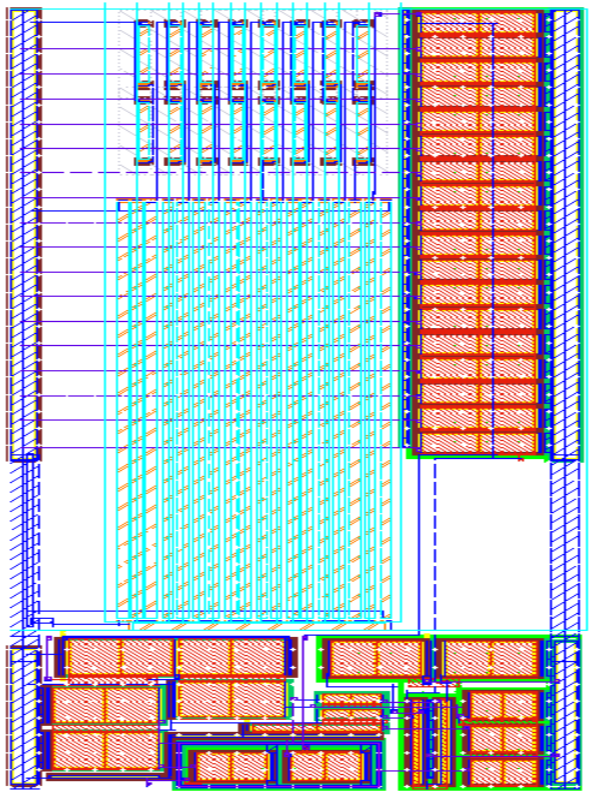


Fig. 10 Layout of ZTC

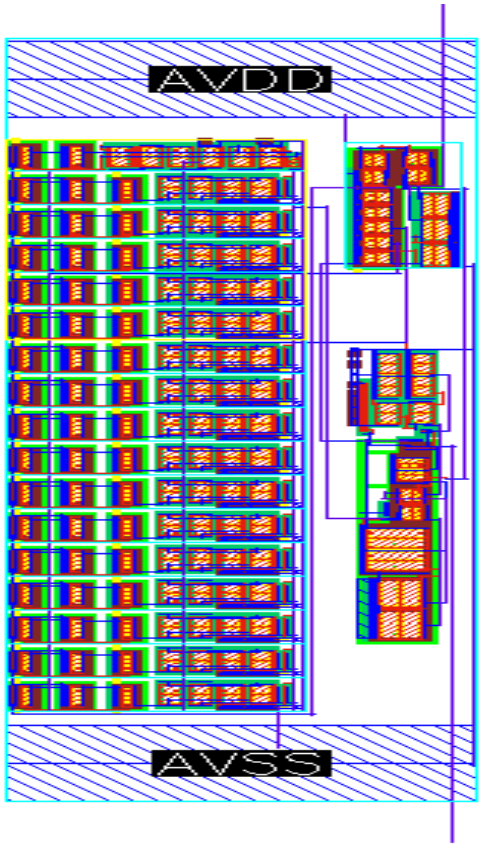


Fig. 11 Layout of Current divider Circuit

In Signal channel:

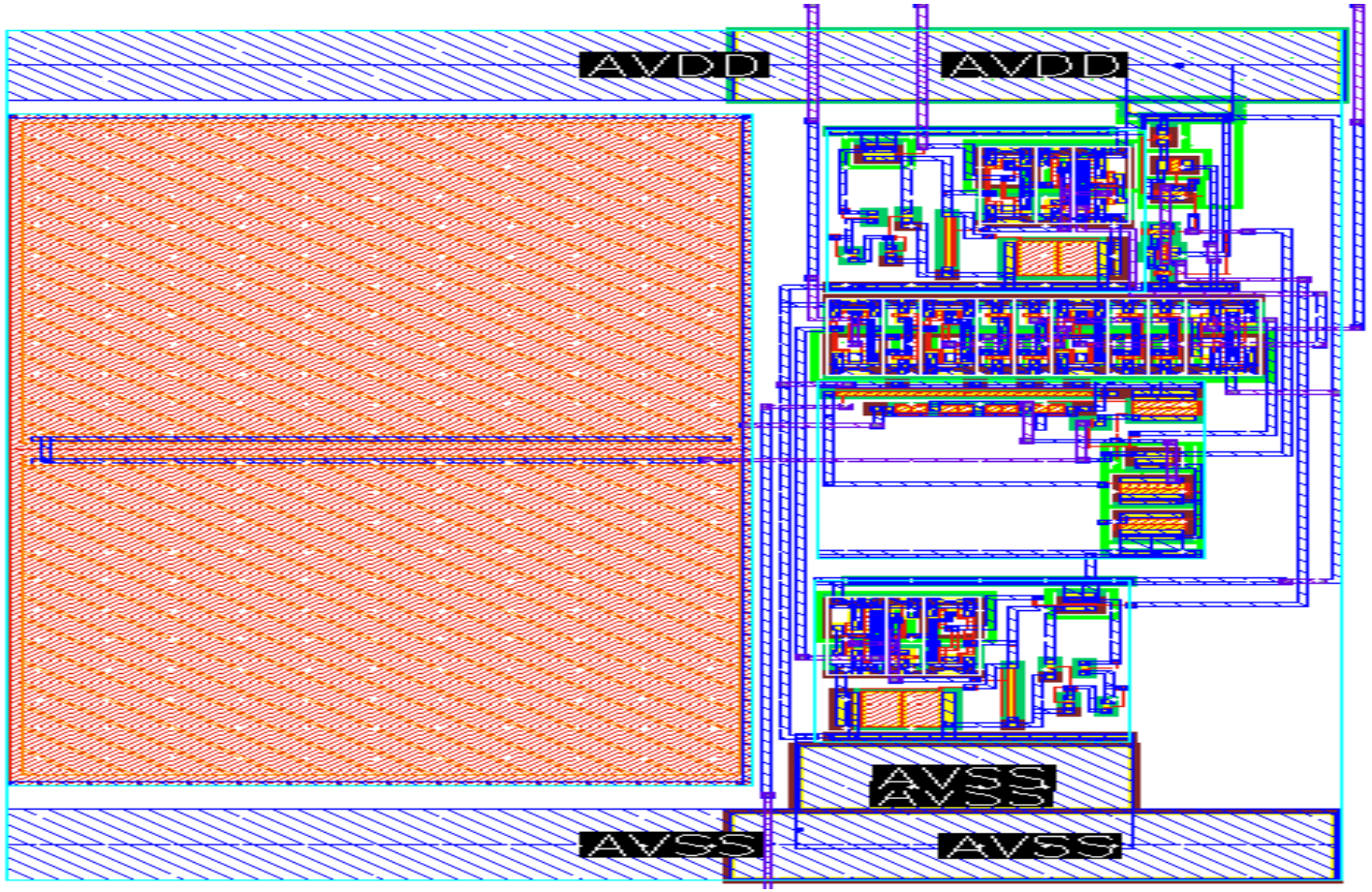


Fig. 12 Layout of Auto reset Circuit

Conclusion

- Designed a Zero temperature coefficient current of 12 µA
- Designed Current divider circuit to divide 12 µA, depends on digital bit
- Verilog-A module: To produce 16 different digital bits, and Qualified CFD pulse
- Auto reset time-out pulse has been generated with widely variable widths.
- Octave script: Linearity plot
- Layout dimensions:

  Signal channel : 144 µm* 100.5 µm

  Common channel: 301.55 µm* 86.25 µm

QUERIES ?

THANK YOU