Design and Analysis of the Linear Branch of an Integrated Circuit for Use in Nuclear Physics Experiments Employing Si-Strip Detectors

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ABSTRACT

DESIGN AND ANALYSIS OF THE LINEAR BRANCH OF AN INTEGRATED CIRCUIT FOR USE IN NUCLEAR PHYSICS EXPERIMENTS EMPLOYING SI-STRIP DETECTORS

by

ANIL KORKMAZ

Chairperson: Professor George L. Engel, D.Sc

This thesis describes the design of the linear branch of a signal processing channel which will be part of a multi-channel integrated circuit for use in radiation monitoring. The thesis describes the design of a charge amplifier, a Gaussian filter, and a peak sampling circuit. The IC is expected to be fabricated through in Fall 2019. The IC has been named HINP5 (Heavy Ion Nuclear Physics IC - Version 5). The design presented here was implemented using a 0.35 μm AMS (Austrian Micro-Systems) CMOS process.

The charge amplifier consists of a very low-noise, high dynamic range two-stage OTA (GBW in excess of 130 MHz) and three double-poly capacitors, each shunted by a small pseudo-resistor (used for pole-zero cancellation) realized using just a few small FETs, thereby greatly reducing silicon area. The charge amplifier has dual outputs, each of which connect to the input of a Gaussian filter used for signal shaping.

The respective charge gain for the two sub-channels is X1 (low-gain) and X4 (high-gain). The use of dual outputs significantly relaxes the noise and dynamic range requirements of the shaper and peak sampling circuits which follow and allows us to achieve outstanding energy resolution (lower than 25 keV - FWHM) for the high-gain output while maintaining a highly linear response for energies as large as 400 MeV in the "low-gain" sub-channel.

The outputs from both sub-channels is brought out of the chip differentially and then sampled by off-chip ADCs.

The peak sampler is composed of an OTA (Operational Transconductance Amplifier) along with a diode-connected NFET and a sampling capacitor. The circuit makes use of correlated double sampling (CDS) to dramatically reduce the output 1/f noise and DC offset associated with the use of small transistors.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

This chapter will introduce the reader to the field of ionizing radiation and describe how a family of custom multi-channel integrated circuits are being developed by the IC Design Research Laboratory at Southern Illinois University Edwardsville (SIUE) and the Nuclear Reactions Group at Washington University in Saint Louis (WUSTL). Their efforts are helping to re-shape this field.

1.1 Research Background

Radiation is generally referred to as energy emitted from a source. Radiated energy types can be heat, light, X-rays, gamma rays or other particles. Moreover, ionizing radiaton is a type of radiation which can remove tightly bound electrons from the orbit of an atom during an interaction, causing the atom to become ionized. Ionizing radiation can occur in two types, namely particles or waves [Ball and Key, 2014]. Furthermore,the particle form of the ionizing radiation can be divided into two sub-groups, directly and indirectly ionizing radiation.

Alpha and beta particles are considered as directly ionizing particles because they carry a charge which can be negative or positive and interact directly with other atomic electrons. This interaction can result in opposite charges attracting each other and same charges repelling each other. On the other hand, neutron particles, X-rays and gamma rays are neutral in terms of electrical charge. Thus, they are considered as indirectly ionizing particles [Siegbahn, 1965].

Some atoms have the same number of protons but a different number of neutrons, in other words, a different number of atomic mass. These type of atoms are called isotope atoms. The chemical properties of the isotope atoms tend to be identical, however their physical properties can differ due to their different atomic mass. Although they are

identical in terms of chemical features, some isotopes are stable while some of them are unstable [Knoll, 1989]. Unstable isotope atoms are defined as radioactive. For example,the hydrogen atom has two other isotope atoms, namely deuterium and tritium. However, only tritium is unstable and thus radioactive. Another example is carbon-12 which has 6 protons and 6 neutrons; meanwhile, carbon-10 has 6 protons and 4 neutrons. Carbon-12 is a stable atom but carbon-10 is unstable and a radioactive atom. [Charity et al., 2007] These unstable atoms generally emit particles which are called alpha, beta, gamma, neutron, *etc.*

Alpha particles are defined as the nucleus of a helium atom, including two neutrons and two protons. Their energy levels are generally higher than the beta particles and gamma rays. They release this high energy while penetrating through tissue, however their penetration power is not as high as gamma rays. Beta particles are ejected electrons of an unstable nucleus. They carry lower energy than the alpha particles, on the other hand their penetration power is strong enough to pass through skin. Alpha and beta particle are emitted from the unstable nucleus and cause a secondary reaction which is an emission of photons. If this photon radiation is produced within the nucleus, it is called gamma rays, otherwise it is called X-rays. X-rays typically have lower energy than gamma rays. Both X-rays and gamma rays have stronger penetration power than alpha and beta particles and they can pass through the human body. A radioactive isotope atom can also eject a single neutron. Neutron particles have no charge and they can penetrate farther than other particles. They can also interact with other neutrons and protons in other atoms causing transfer of energy [Siegbahn, 1965].

The Nuclear Chemistry Group at WUSTL is highly interested in the study of ionizing radiation and are focused on answering the following questions;

- Why are some nuclei stable and others not?
- What are the limits of nuclear stability in terms of mass, charge to mass, angular

momentum and excitation energy and how do nuclei decay at the limits of stability?

- Why are some nuclei deformed and others not?
- How were nuclei synthesized in the early universe and stellar environments?
- How does the density of states of the nuclear system evolve with excitation energy and angular momentum? Or in general, how can, or should, one describe the thermodynamics of small quantum systems?
- What is the Equation of State (EoS) of nuclear matter (the material that comproses greater than 99% of the (non-dark) matter of the universe?

These questions have created the need for application specific integrated circuits (ASICs) for modern detectors to study ionizing radiation within scientific experiments, which require a high degree of precision and accuracy.

1.2 Need for an Integrated Circuit

ASIC (Application Specific Integrated Circuit) development requires close interaction and exchange of ideas between theoretical scientists, experimental scientists, and design engineers. This interactive relationship not only provides the most efficient designs but also lowers the cost of producing the integrated circuits (ICs) which is crucial in academic environments. Thus, the "Integrated Circuits Design Research Laboratory" at SIUE and the Nuclear Reactions Group at WUSTL have been working together on a family of multi-channel custom integrated circuits (ICs) since 2001. These ICs are used for the detection and measurement of ionizing radiation. The three main reasons for this collaborative effort to develop custom circuits for use in nuclear physics experiments are:

- None of the commercial chips' specifications matched the interest of the experimentalists, and commercial chips were not able do what researchers wanted to do.

- Scientists have evolving needs which makes it vital for the researcher to be on top of the design decision mechanism and to be able to change or update the design if needed.

- The micro-chips could serve the widespread low- and intermediate-energy nuclear physics community which is working on a wide variety of important applications.

Silicon (Si) strip detectors are used to detect ionizing radiation and measure energy levels. Si-strip detectors are formed by p-n junctions referred to as diodes. An ion beam collides with a stable atom and causes the stable atom to become unstable. As mentioned in the Research Background section, unstable atoms radiate and emit alpha, beta, gamma, and other ionizing particles. Si-strip detectors need to be placed strategically [Wallace et al., 2007] because every particle follows a unique radiation path [Ball and Key, 2014]. An example alignment of 17 Si-strip detector arrays is shown in Figure 1.1. When particles interact with these detectors, scientists collect the data related to the incident radiation. The data regarding the position and angle of the incoming radiating particle can be determined via the x and y coordinates within the detector where the particle struck. See Figure 1.2 for a single Si-strip detector array.

When radiation strikes a Si-strip detector, a charge packet (proportional to the energy of the radiation) is released in a very short period of time. The output of the detector can be modeled as a current impulse. The purpose of the the HINP chip described herein is to convert the current impulse into a voltage (also proportional to the energy of the particle that struck the detector) that can then be sampled by an off-chip ADC (Analog-to-Digital Converter). The ADC data is then transmitted to a host computer for analysis. In order to produce a compact instrument, a single HINP IC supports 16 detectors. It is the design of the circuits which convert the current impulse to a voltage that is proportional to the energy of the ionizing radiation (linear branch of HINP) which is the subject of this thesis.

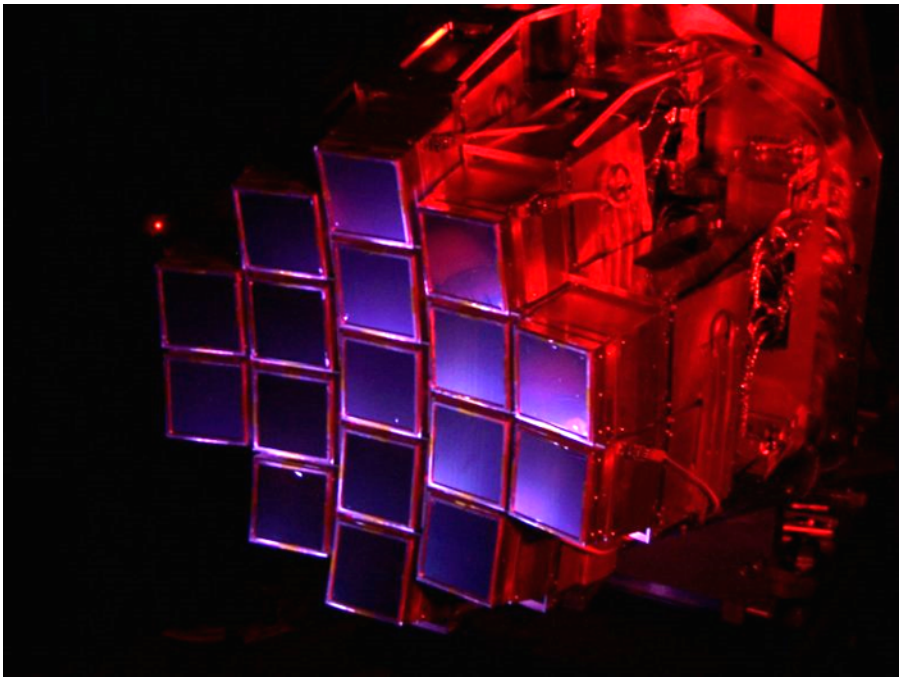

Figure 1.1: A High-Resolution Si-Strip Detector Array (HiRA)

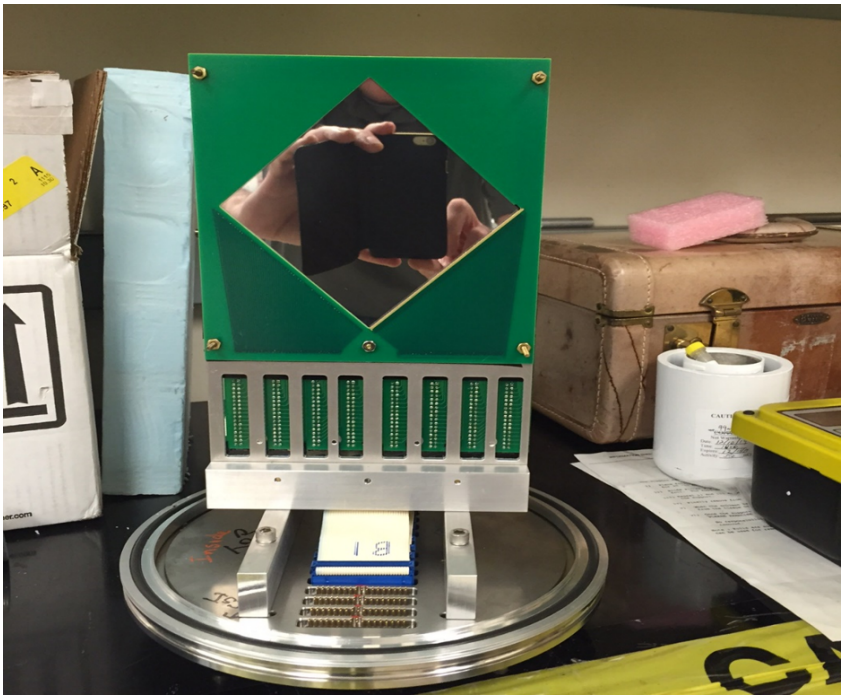

Figure 1.2: A Single Silicon Strip Detector Array

In addition to determining energy level, the HINP IC must also be able to create a voltage which is proportional to the time of arrival of the current impulse relative to an externally supplied time reference (timing branch of HINP). The design of the timing branch is the work of another student in our group and described else where.

The actual instrument used in experiments consists of a motherboard (MB), see Figure 1.3, which can host 16 chipboards (CBs). Each CB, see Figure 1.4, consists of two HINP ICs, three ADCs, a Field Programmable Gate Array (FPGA), and a some other supporting circuits. As described above, the analog outputs of the HINP chip needs to be digitized by a high-resolution (16 bits), high-speed (250 kSamples / sec) ADCs. The FPGA is used for configuration of the HINP chips and to provide a direct interface to the serial ADCs. In short, a single motherboard can service up to 512 Si-Strip detectors. The number of the channels can be increased for other projects by using multiple motherboards.

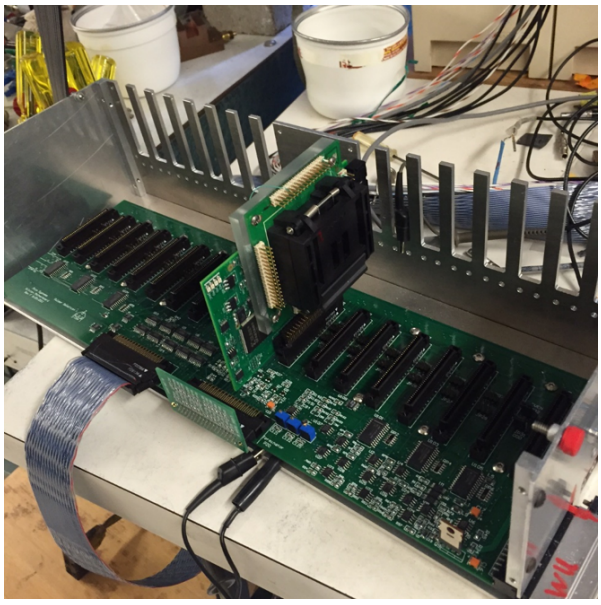

Figure 1.3: HINP Motherboard (Contains up to 16 chip boards)

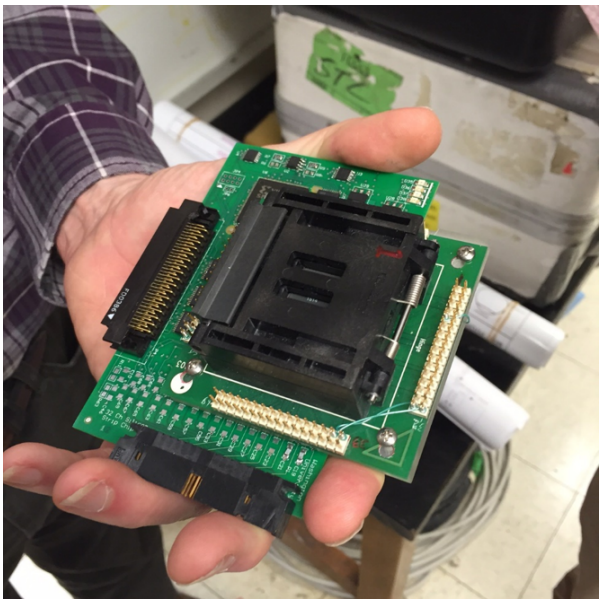

Figure 1.4: HINP Chip Board (Contains 2 HINP ICs, an FPGA and an ADC)

1.3 HINP5 System Level Design

The measurement of energy levels for unstable nuclei beams are particularly challenging especially at low levels. In this regard, the HINP chip was designed to provide very high energy resolution as well as very high dynamic range. These properties make it well-suited for the measurement of low and intermediate energy levels.

We now present the specifications for the HINP5 IC described in this thesis.

- Very high energy resolution ($<$ 25 keV FWHM *i.e.* Full-Width-Half-Maximum).
- Must support energy levels as high as 400 MeV.
- Detection of both electrons and holes.
- Two different gain modes, namely high-gain and low-gain, operating in parallel. High-gain mode measures energy levels up to 100 MeV and low-gain mode measures energy levels as high as 400 MeV.
- Should accommodate the use of external charge amplifiers.

- Should accommodate the use of an external pulser for verification and calibration purposes. Even and odd channels should be able to be pulsed separately so that crosstalk between channels can be assessed.

- Built-in high-precision, low-walk, low-jitter timing circuitry (not discussed in this thesis).

- Easily configured.

- Must be easy to read out the results in the form of three analog pulse trains (high-gain, low-gain, time) synchronized to digital channel addresses.

- Must provide data sparsification. In other words, whenever the physicists decide not to read out the data, the analog and digital circuits in each of the channels must automatically reset themselves after some time (programmable over a wide dynamic range) has elapsed after channel has been hit by radiation.

At the system level (see Figure 1.5), the HINP chip consists of three main blocks, denoted as the linear branch, the timing branch and configuration/control circuitry. The linear branch and timing branch are located in each of 16 channels and the configuration/control circuitry is predominantly located in the common channel. The linear branch is mostly analog circuitry and consists of three main blocks called the charge amplifier, slow shaper, and the peak detector. The timing branch is a mix of analog and digital circuits and has three main blocks called the Nowlin circuit, constant fraction discriminator (CFD) and time-to-voltage converter (TVC) [Engel et al., 2007]. The configuration/control circuitry consists of primarily digital circuits and has two main blocks called the control/readout circuits and the configuration logic.

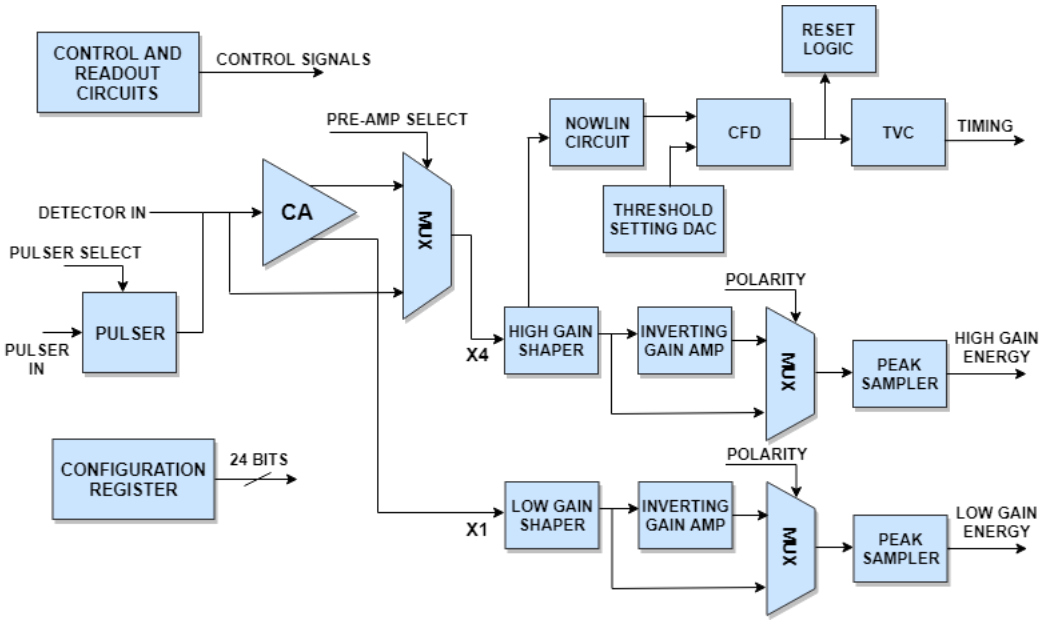

Figure 1.5: HINP5 Block Diagram

1.4 Sample Applications

The HINP chip can be used in any low- and intermediate- energy application where Si-strip detectors are in use due to its very low noise and high dynamic range properties. An ideal application for use of Si-strip detectors is detection and measurement of ionizing particles with low energies. A particle that generates 24,000 electrons while penetrating through a 300 μm thick Si-strip detector can provide adequate positional information [Ghosh, 2015]. The amount of charge collected by the detector directly depends on the depletion region thickness within the detector. The charge collection time is generally between 10 ns for negative polarity (electron collection) and 25 ns for positive polarity (hole collection) [Ghosh, 2015].

The advantages for using Si-strip detectors for particle detection are their high efficiency, small relative size compared to other sensors which increases their positional resolution and their composition in the solid state which induces high material stability. The disadvantages to using Si-strip detectors are their requirement for advanced readout

circuits with large amplification and very low noise properties as well as their DC leakage current and susceptibility to degradation due to radiation.

Recent progress in ASIC design, improvement in material quality, significant reduction of cost, growth in expertise and improvement of assembly has led exponential growth the applicability of Si-strip detectors. Applications that Si-strip detectors are in use [Sadrozinski, 2001];

- Tracking purposes in High Energy Proton-Proton Collision, Large Hadron Collider (LHC), High Luminosity Large Hadron Collider (HL-LHC).
- Tracking purposes in astrophysics such as SilEye (Silicon Eye) detectors used with a helmet to observe space.
- Tracking purposes in medicine such as Nanodosimetry which are used to measure the interaction of radiation with DNA.
- X-ray imaging in medicine, for example Mammography. Mammography is a method of breast screening to detect possible cancer formation.
- Compton Telescope and Nuclear Compton Telescopes in astrophysics to observe space.
- Compton Cameras in medicine, especially in Magnetic Resonance Imaging (MRI) and Computed Tomography (CT)

1.5 Previous Work

As mentioned in the previous sections, scientists' needs are evolving with time and a close interaction between the theoreticians, experimentalists, and IC design engineers is an effective way to answer these new requirements. There have been four previous versions of the HINP chip prior to the one described here in this thesis. Every new HINP

design tried to solve the problems of the previous HINPs and added new features based on new needs.

The first IC had 16 channels and suffered from linearity issues for energy levels up to 15 MeV, and its noise performance was insufficient. The second version of the IC, HINP2, was never really used in experiments because of design issues. HINP3 was a great success and used in many experiments. The next generation chip, HINP4, was fabricated to increase the dynamic range of the IC. This was done by using dual shapers so that the low- and high-gain modes could operate in parallel. (Prior to HINP4, the user had to select either low-gain OR high-gain mode.) But mismatch/process variability issues affecting linearity made it only a partial success.

In this design, HINP5, the mismatch and process errors were carefully evaluated with Monte Carlo simulations. Moreover, in HINP3 and HINP4 two different peak samplers were used to detect positive and negative peaks. However in this design, a 2-to-1 analog multiplexer along with an inverting gain amplifier allowed us to remove one of the peak samplers from the channel. This change helps reduce silicon area occupied by HINP5. Also, in HINP5 the peak samplers automatically leave *write* mode and enter *read* mode.

Moreover, in the previous version, pseudo-resistors (implemented using small FETs) for the charge amplifier circuitry could not be implemented completely for both polarities due to the high 1/f noise associated with the NFETs in the process, thus real resistors were used for one polarity. The use of real resistors in the charge amplifier made it physically quite large. On the other hand, in the HINP5 design, described herein, the use of pseudo-resistors for both polarities helps reduce the area and helps improve the dynamic range of the charge amplifier. The new core amplifier design provides the opportunity to reach superior noise properties. Finally, it should be noted that all earlier versions of the IC were implemented using the ON Semiconductor 0.5 μm CMOS process while the HINP5 design was carried out using the AMS 0.35 μm CMOS process.

1.6 Object and Scope of Work

The objective of this thesis work was to design, analyze, simulate, and physically layout the linear branch of the HINP5 IC which will be used in nuclear physics experiments where there is a need to detect and monitor ionizing radiation. The linear branch is the analog signal processing module of the HINP5 chip which converts a charge packet generated in a Si-strip detector (when radiation strikes the detector) into a voltage which is proportional to the energy of the radiation which impacted the detector.

The linear branch has three main blocks; namely, a charge amplifier, a pair of shapers, and a pair of peak detectors. The design of the charge amplifier is discussed in Chapter 2. Chapter 3 describes the the design of the shaper circuit. The design of the peak detector is convered in Chapter 4 of this thesis. The final chapter in the thesis summarizes our findings and identifies future work which must be completed before fabricating the IC. In each chapter, the design will be discussed and then the performance of the design will be evaluated using simulation. The timing branch and configuration/control circuits are out of the scope of this thesis work and they will not be discussed.

CHAPTER 2

CHARGE AMPLIFIER

In this chapter, the first module of the linear branch, the charge amplifier, will be discussed. As is generarlly true in analog circuit design, the performance of this block, in large part, determines the overall performance of the linear branch [De Geronimo et al., 2000]. Thus, it was crucial to meet the design specifications given in Section 2.1.

The HINP5 chip is to be fabricated in the AMS 0.35 μm n-well CMOS process. The process offers two poly layers, and four metal layers. Metal 4 is an extra-thick metal layer which is used for distributing power throughout the IC. The two poly layers allow the user to create high density double poly capacitors ($0.86\frac{fF}{\mu m^2}$). The second poly layer also can be used to form two types of resistors: one (RPOLY2) with a sheet resistance of 50 Ω per square and the other (RPOLYH) with a sheet resistance of 1200 Ω per square. The supply voltage for this process is 3.3 V - 3.6 V. In this and in the next two chapters, transistor process parameters will be needed by the reader in order to understand the design details. Therefore, process information is shared with the reader here. Table 2.1 shows the device parameters related to the NFET (N-type Field Effect Transistor) and device parameters for the PFET (P-type Field Effect Transistor) are given in Table 2.2.

A charge amplifier consists of a charge-sensitive amplifier which converts charge into voltage. A charge-sensitive amplifier is created by using an operational transconductance amplifier (OTA) with a capacitor in the feedback path. Charge can be slowly bled off the feedback capacitor using a large-valued resistance. The output voltage from the charge-sensitive amplifier can then be converted back into a charge by connecting the output of the charge sensitive amplifier to the summing node of an op-amp. The charge gain is a function of the ratio of the capacitor value at the output of the charge sensitive amplifier to the value of the capacitor in the feedback path. In this application we need

two different charge gains: 1 and 4. Therefore, the charge amplifier described in this chapter has two outputs and therefore we have two output capacitors where one is 4 times larger than the other.

Table 2.1: NFET Parameters

Threshold Voltage	V_{TN}	0.5 V
Transconductance Parameter	K_{PN}	170 $\frac{\mu A}{V^2}$
Bulk Modulation Factor	γ_N	0.6 $V^{\frac{1}{2}}$
Early Voltage per Unit Length	V_{EN}	21.1 $\frac{V}{\mu m}$
Gate Oxide Thickness	t_{ox}	7.6 nm
Gate Oxide Capacitance per Unit Area	C_{ox}	4.5 $\frac{fF}{\mu m^2}$
Threshold Voltage Matching Coefficient	A_{VTN}	9.4 mV $\cdot$ μm
Transconductance Matching Coefficient	A_{KPN}	0.7 % $\cdot$ μm

Table 2.2: PFET Parameters

Threshold Voltage	V_{TP}	-0.7 V
Transconductance Parameter	K_{PP}	60 $\frac{\mu A}{V^2}$
Bulk Modulation Factor	γ_P	0.4 $V^{\frac{1}{2}}$
Early Voltage per Unit Length	V_{EP}	17.7 $\frac{V}{\mu m}$
Gate Oxide Thickness	t_{ox}	7.6 nm
Gate Oxide Capacitance per Unit Area	C_{ox}	4.5 $\frac{fF}{\mu m^2}$
Threshold Voltage Matching Coefficient	A_{VTP}	14.5 mV $\cdot$ μm
Transconductance Matching Coefficient	A_{KPP}	1.0 % $\cdot$ μm

2.1 Design Specifications

The design specifications of the charge amplifier are based on both external factors such as detector capacitance and internal factors, for example, the gain-bandwidth product of the core amplifier. The specifications for our charge amplifier were the following;

- Must have two charge outputs (charge gain of 1 and charge gain of 4).
- It should support detector capacitances between 25 pF and 300 pF.
- It must possess a very high dynamic range (at least 86 dB)
- The rise time of the charge-sensitive amplifier should be less than 75 ns for detector capacitances less than 200 pF
- The Gain Bandwith Product (GBW) of the core amplifier should be at least 130 MHz with a low-frequency open loop gain of at least 80 dB
- The charge sensitive amplifier should posses a decay time constant of $\approx$20 μs.
- The phase margin should be at least 45 degrees for detector capacitance of 25 pF to assure stability.
- Low total integrated noise ($\approx$20 keV).
- Wide voltage swing for core amplifier (as close to rail-to-rail as possible).
- Utilization of fully compensated continuous reset system.

In the simulation section, the results will be provided to demonstrate all of the specifications listed above were satisfied. In the following section, the charge amplifier architecture will be discussed in detail and the blocks which have influence over the charge amplifier performance will be characterized.

2.2 Design

In HINP5, we must be able to support energy levels up to 400 MeV. Therefore, this specification sets the feedback capacitor value. One can calculate the maximum charge packet corresponding to 400 MeV using Equation 2.1.

$$Q_{max} = Q_e \cdot \left[\frac{E_{max}}{3.6eV}\right] \tag{2.1}$$

In Equation 2.1, E_{max} is the energy level of the particle (maximum of 400 MeV). 3.6 eV is the energy required to form an electron-hole pair in silicon. Q_e is defined as the charge of an electron ($1.602 \cdot 10^{-19}$). As a result, Q_{max} is calculated as 17.8 pC for the maximum energy level.

A continuous reset system using pseudo-resistors (implemented using small FETs) allows the charge sensitive amplifier to idle at a voltage, V_{DD} - $|V_{TP}|$ when we are collecting holes. When a charge packet (holes) corresponding to an energy level of 400 MeV strikes the detector the output of the charge sensitive amplifier will plunge to the negative rail. It can be seen from the Table 2.2 that $|V_{TP}|$ is 0.7 V for this process. Hence, V_{max} is 2.6 V. The design of the pseudo-resistors will be discussed in detail in Subsection 2.2.2.

Since Q_{max} and V_{max} are now known, the feedback capacitor, C_f, can be calculated using Equation 2.2.

$$C_f = \frac{Q_{max}}{V_{max}} \tag{2.2}$$

2.2.1 Core amplifier

The result obtained from the Equation 2.2 is ≈7 pF. The charge amplifier needs to support detector capacitances, C_{DET}, in the range 25 pF to 300 pF. Therefore, the closed-loop gain range of the amplifier can be calculated using Equation 2.3.

$$Gain = \frac{C_{DET}}{C_f} \tag{2.3}$$

This results in closed-loop gains between 11 and 33 dB. The higher the closed-loop gain, the smaller the bandwidth (BW). The product of the closed-loop bandwidth and closed-loop gain must equal the GBW of the core amplifier (130 MHz). The bandwidth in turn determines the rise time, t_r, of the signal at the output of the amplifier.

From the Equation 2.4, to ensure rise times shorter than 75 ns for the detector capacitances up to 200 pF, a GBW of 130 MHz was calculated for the core amplifier. A two-stage OTA design was selected for the core amplifier to meet the high GBW requirement. The first stage was designed to have 71 dB of gain and another 35 dB of gain was obtained from the second stage which corresponds to 106 dB total low-frequency open loop gain.

$$t_r = \frac{0.35}{BW} \tag{2.4}$$

In a properly designed amplifier, the dominant noise source should be the input transistor. Other noise contributors such as cascode transistors and load transistors should be made negligible. Also, the white noise and 1/f noise terms are minimized for $C_G = C_S$ (capacitive matching) where C_G is the input capacitance of the input transistor and C_S is the total external capacitance at the input [De Geronimo and O'Connor, 2005]. Thus, the input transistor was designed to have a large shape factor with a minimum length while operating in a moderate inversion region. This not only helps the capacitive matching but also increases the g_m value of the input transistor. A moderately inverted FET has an equivalent noise resistance given by Equation 2.5.

$$R = \frac{2}{3} \cdot \frac{1}{g_m} \tag{2.5}$$

A PFET with a gate length of L = 0.35 μm and gate width of W = 1 mm (16 μm

x 64 fingers) was selected for the input transistor and was biased at a drain current of 630 μA. Therefore, g_m is 9.25 $m\mho$. We shall now be able to calculate the equivalent noise resistance of the input transistor. It is $\approx$70 Ω. The use of a single-ended input structure significantly relaxes the noise requirements by a factor of $\sqrt{2}$ compared to differential input structures.

The use of cascode structure in the input stage of our OTA helps us to achieve high open loop gain and wide bandwidth. There are three cascode structures which have been recently adopted by designers for applications that require high gain, wide bandwidth, low noise and high dynamic range: single cascode (SCS), amplified cascode (ACS) and dual cascode (DCS) [De Geronimo et al., 2008], see Figure 2.1. The ACS and DCS were designed to solve SCS's issues which limit the amplifier's performance. The three main problems related to SCS design are (1) its high input impedance limits the DC gain (2) its high input impedance adds a pole (at a low freqeuncy) at the drain of M_0 which decreases phase margin and (3) it affects the pole-zero cancellation due to the contribution from the gate-to-drain capacitance of the input FET which is amplified by the voltage gain resulting in integrating a significant amount of the incoming charge [De Geronimo et al., 2008].

In terms of the impedance at the drain of M_0, DC voltage gain and noise, ACS and DCS configurations improve the system performance. Both ACS and DCS decrease cascode impedance through extra transistors, namely M_A and M_2. However, a DCS offers slightly better improvement in regards to GBW and power dissipation. Both of the structures add two extra poles to the amplifier's transfer function, both of which are at high frequencies. However, ACS's extra poles can be complex conjugates, and as a result these might cause difficulties within the stabilization process of the amplifier. On the other hand, a DCS adds real poles that have fewer engineering challenges. These two structures have their main difference in terms of power dissipation. The M_A transistor in the ACS configuration requires an extra bias current which increases the dissipated power

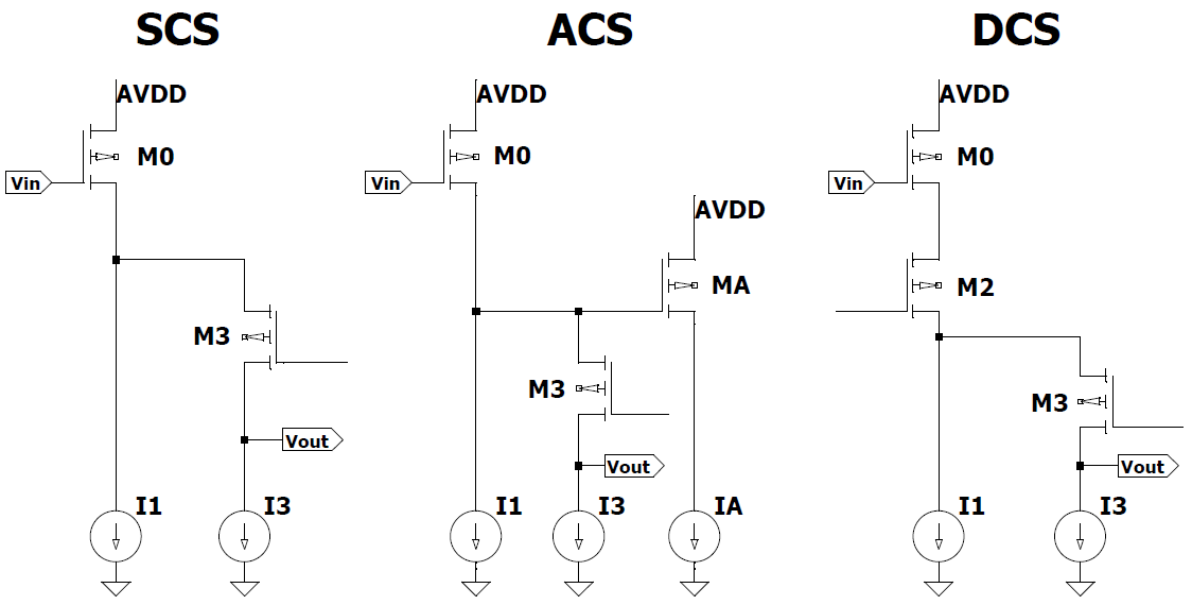

Figure 2.1: Cascode Comparison

which is important in keeping the power dissipated in the HINP5 IC as low as possible. After careful consideration, a DCS configuration was implemented for the core amplifier's input stage.

In our amplifier design, see Figure 2.2, it can be easily observed that the M_0 is the input device, M_2 is the first cascode device and M_3 is the second cascode device. The bias current of M_3 is controlled by a loop which involves M_3, M_6, M_7 and M_8, given in Equation 2.6. It is very important to match M_3-M_6 and also M_7-M_8. It can be seen that two conditions need to be satisfied for the loop to work properly. The effective voltage terminology, V_{eff} used to describe saturation voltage of the FET, in other terms, $V_{DS,SAT}$.

$$V_{DD} - (V_{eff7} + |V_{TP}|) - (V_{eff6} + |V_{TP}|) + (V_{eff3} + |V_{TP}|) + (V_{eff8} + |V_{TP}|) = V_{DD} \quad (2.6)$$

$$V_{eff3} < V_A - V_B = [V_{DD} - (V_{eff8} + |V_{TP}|)] - [(V_{eff4} + V_{TN})] \quad (2.7)$$

Equation 2.7 makes sure that second cascode device M_3 is saturated. The gain of the

first stage obtained by the transistors M_8 and M_9 form a push and pull output stage, referred to as a complementary common source amplifier. The combination of these two transistors provides an output resistance of ≈100kΩ with a bias current of 100 μA. The result is 71 dB of gain at the output of the first stage. The schematic of the core amplifier is presented in Figure 2.2, and the devices sizes can be found in Table 2.3.

A 10 pF compensation capacitor, C_c was used. Lead-lag compensation (addition of resistor in series with C_c) was used to cancel one of the lower frequency poles, thereby further increasing the GBW. The resistor was implemented with a PFET operating in the resistive region to save silicon area and to ensure tracking across process corners. At the output of the charge amplifier a 42 pF capacitive load was expected, therefore the compensation capacitor's value was selected to be relatively high in order to assure stability with the expected load.

The second stage implemented a common source amplifier with a current source load structure. To satisfy the risetime of 75 ns specification, the slew rate (SR) of the amplifier needed to be significantly high. In order to achieve high slew rate, a high bias current at the output node was required. The bias current was choosen as 1.1 mA also significantly increases the g_m value of the input transistor M_{10} to $7m℧$. This resulted in a second-stage gain of 35 dB. A gain contribution of the second stage drove the total gain of the amplifier to 106 dB. A slew rate of 110 V/μs was calculated using Equation 2.8.

$$SR = \frac{I_{M10}}{C_c} \tag{2.8}$$

One of the other important parameters of an amplifier is the frequency response. In our design, there are 5 important nodes that significantly impact the frequency response and phase margin of the OTA. As shown in Table 2.4, Node D is the dominant pole. The high load capacitance of 42 pF makes the output node the second lowest pole frequency at 27 MHz. Thus, lead-lag compensation was used to cancel this pole's impact.

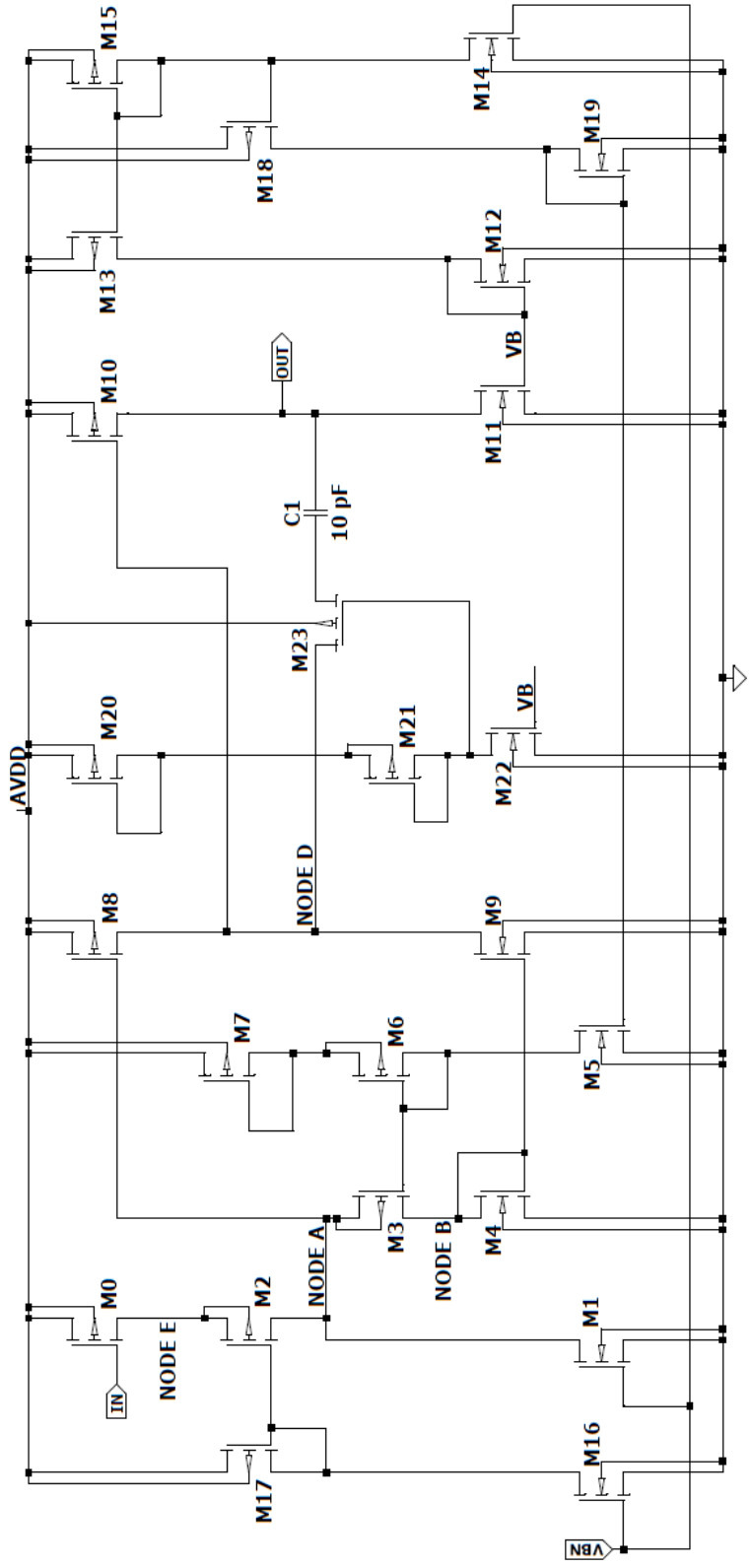

Figure 2.2: Core Amplifier Schematic

Table 2.3: Device Sizes for Core Amplifier

	W (μm)	L (μm)	Gates	I_D (μA)
M0	32	0.35	32	650
M1	16.8	16	10	550
M2	32	0.7	2	650
M3	4.6	0.7	2	110
M4	4.7	2	2	110
M5	9.4	2	2	110
M6	4.6	0.7	2	110
M7	4.6	0.7	2	110
M8	4.6	0.7	2	110
M9	4.7	2	2	110
M10	93.3	0.7	4	1100
M11	37.7	2	10	1100
M12	37.7	2	1	110
M13	13.3	2	2	110
M14	16.8	16	2	110
M15	13.3	2	2	110
M16	16.8	16	2	110
M17	6.2	3	2	110
M18	13.3	2	1	55
M19	9.4	2	1	55
M20	7.7	0.7	1	110
M21	7.7	0.7	1	110
M22	37.7	2	1	110
M23	36.2	0.7	1	

Table 2.4: Parasitic and Dominant Pole Locations

	Pole Location (Hz)
Node A	$248{\cdot}10^6$ (Parasitic)
Node B	$318{\cdot}10^6$ (Parasitic)
Node D	$2.5{\cdot}10^3$ (Dominant)
Node E	$183{\cdot}10^6$ (Parasitic)
Output	$27{\cdot}10^6$ (Cancelled)

2.2.2 Continuous reset circuit and pole-zero cancellation

The feedback capacitor of the amplifier integrates the current released by the detector. The high repetition rate charge pulses coming from the detector stored in the feedback capacitor may cause the amplifier to saturate. Thus, a continuous reset circuit needs to be implemented to discharge the feedback capacitor [De Geronimo and O'Connor, 2000]. A continuous reset circuit makes use of a feedback resistance in parallel with a feedback capacitor (see Figure 2.3). The value of the resistor is determined by the decay time specification of the charge sensitive amplifier which is at ≈20 μs in this application. One can calculate the value offeedback resistance using Equation 2.9.

$$R_f = \frac{t_f}{C_f} \tag{2.9}$$

The value of R_f was found to be ≈2.8 MΩ, but a resistor with such high value occupies a very large area. Although a large valued resistor will have a high thermal noise voltage associated with it, this is not a problem in our circuit because R_f and C_f form a low-pass filter (with a low corner frequency), and low-frequency noise is rejected by the shaper.

When holes are collected by the charge amplifier, the core amplifier input idles at $V_{DD} - |V_{TP}| - V_{eff0} \approx 2.6V$ which forces amplifier output to idle at same value (2.6 V) in

DC operation and it can go as low as ground level. However, when electrons are collected, using a real resistor does not work because the amplifier would have a range of 2.6 V to 3.3 V. Rather, the amplifier output should idle at V_{TN} and be able to make excursions to V_{DD} when electrons are being collected, which will allow the maximum dynamic range to be achieved. Therefore, the feedback resistance was implemented as a pseudo-resistor (implemented using a FET) to greatly reduce the silicon area and to provide correct operation for both polarities.

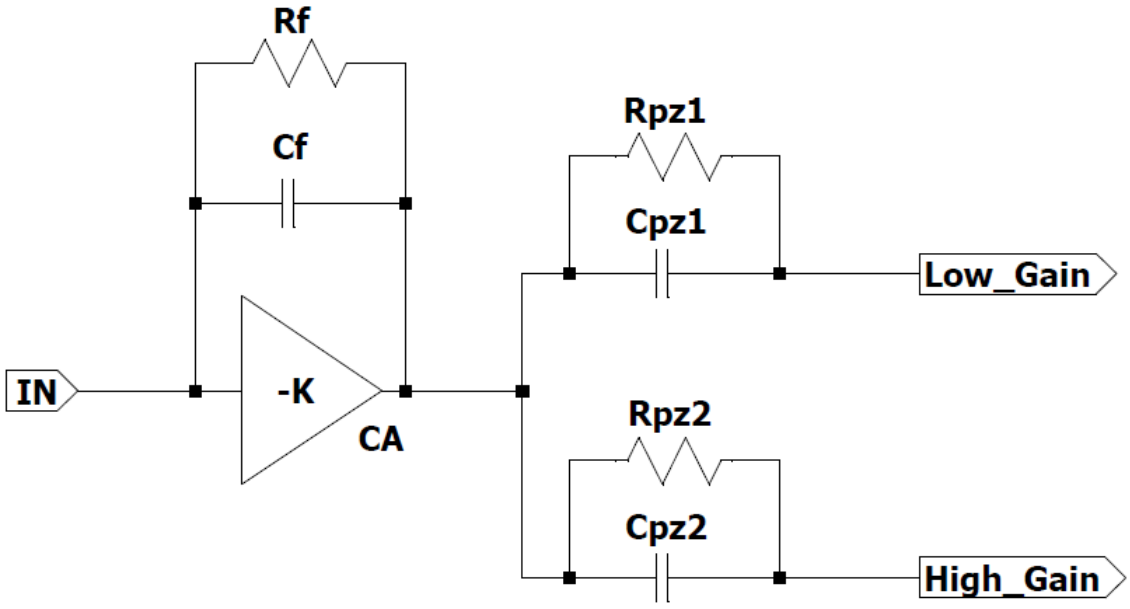

Figure 2.3: Pole Zero Cancellation

R_f along with the C_f in the charge sensitive amplifier introduce a low-frequency pole. This extra pole results in an undershoot at the output of the shaper and spoils the semi-Gaussian shaped pulse which is desired at the output of the shaper[Grybos et al., 2007]. In order to handle high pulse repetition rates, it is necessary that we return to the baseline in a very short period of time (a few μs). The introduction of the low-frequency pole causes the return to the baseline to be unacceptably long. A zero must be introduced to cancel this unwanted pole.

Table 2.5: PZC Circuit Component Values

	R_f, C_f	R_{pz1}, C_{pz1}	R_{pz2}, C_{pz2}
R	2.8 MΩ	2.8 MΩ	0.7 MΩ
C	7 pF	7pF	28 pF
ω	50 kHz	50 kHz	50 kHz

As described earlier, C_{pz1} and C_{pz2} are needed in order to convert the voltage at the output of the charge sensitive amplifier back into a current. The shaper input is a current impulse with the output being a semi-Gaussian shape voltage. The PZC (pole-zero cancelation) circuit adds a resistor in parallel with the capacitor and introduces a zero to cancel the pole due to R_f and C_f. It can be seen from Figure 2.3 that, R_{pz1} - C_{pz1} form the PZC circuit for the low gain sub-channel and R_{pz2} - C_{pz2} for the high gain sub-channel. The pole and the zero have to be located at approximately the same frequency to cancel each other [Grybos and Szczygiel, 2008], see Table 2.5. Therefore, Equation 2.10 needs to be satisfied.

$$R_f \cdot C_f = R_{pz1} \cdot C_{pz1} = R_{pz2} \cdot C_{pz2} \tag{2.10}$$

The transfer function at the output of the PZC circuit is given in Equation 2.11. It can be observed from the transfer function that the pole introduced by the feedback path is being canceled by the zero introduced in PZC circuit. The Q_{in} is the charge packet sensed at the input of the amplifier and Q_{out} is the charge injected into the input of the shaper circuit which will be discussed in Chapter 3.

$$TF(s) = \frac{Q_{out}}{Q_{in}} = \frac{R_f}{s \cdot C_f \cdot R_f + 1} \cdot \frac{s \cdot C_{pz} \cdot R_{pz} + 1}{R_{pz}} \tag{2.11}$$

Because of the reasons mentioned previously in this section, an effective resistance is needed to discharge C_f. Pseudo-resistors are employed [De Geronimo and O'Connor, 2000].

Since the amplifier output needs to swing between V_{TN} and V_{DD} for electron collection and between $(V_{DD} - V_{TP})$ and ground for hole collection, two different circuits were designed. A configuration bit defining polarity is used to select the appropriate circuit. The switches also make sure that FETs are not floating when a circuit is not being used.

When electrons are being collected, the charge amplifier makes use of the circuit depicted in Figure 2.4. The generated V_{TN} (0.5 V) voltage is applied to the gate of M_0 which forces the amplifier output to idle at V_{TN}. The feedback capacitance, C_f is located between the drain of the M_1 and the drain of the M_2 which are the pseudo (PMOS) resistors. They must be matched. The charge stored in C_f results in current flow through M_2. The PFETs M_4 and M_5 are the pseudo PMOS resistors which were used in the PZC circuit. They are also matched with the M_1 and M_2. However, M_5 is made 4 times as wide (4 parallel FETs) in order to satisfy Equation 2.10, as it can be seen in Table 2.6.

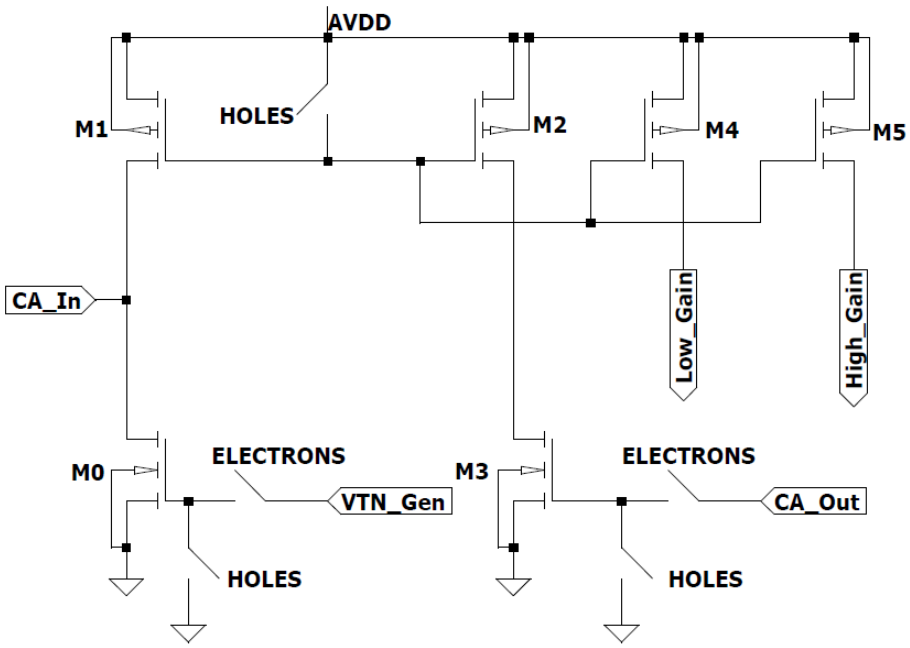

Figure 2.4: Continuous Reset Circuit - Electron Collection

For hole collection we use the circuit illustrated in Figure 2.5. The generated $V_{DD} - |V_{TP}|$ (2.6 V) voltage is applied to the gate of the M_6 that forces the amplifier output to

Table 2.6: Device Sizes for Continuous Reset Circuit - Electron Collection

	W (μm)	L (μm)	ng
M0	1	60	1
M1	2	20	1
M2	2	20	1
M3	1	60	1
M4	2	20	1
M5	8	20	4

idle at $V_{DD} - |V_{TP}|$. The transistors M_7 and M_8 are the pseudo (NMOS) resistors and M_7 takes the feedback capacitor's charge off. Similar to the circuit in Figure 2.4, M_{10} and M_{11} were used for the PZC. As before, M_{11} is made 4 times wider (one-fourth the resistance), see Table 2.7.

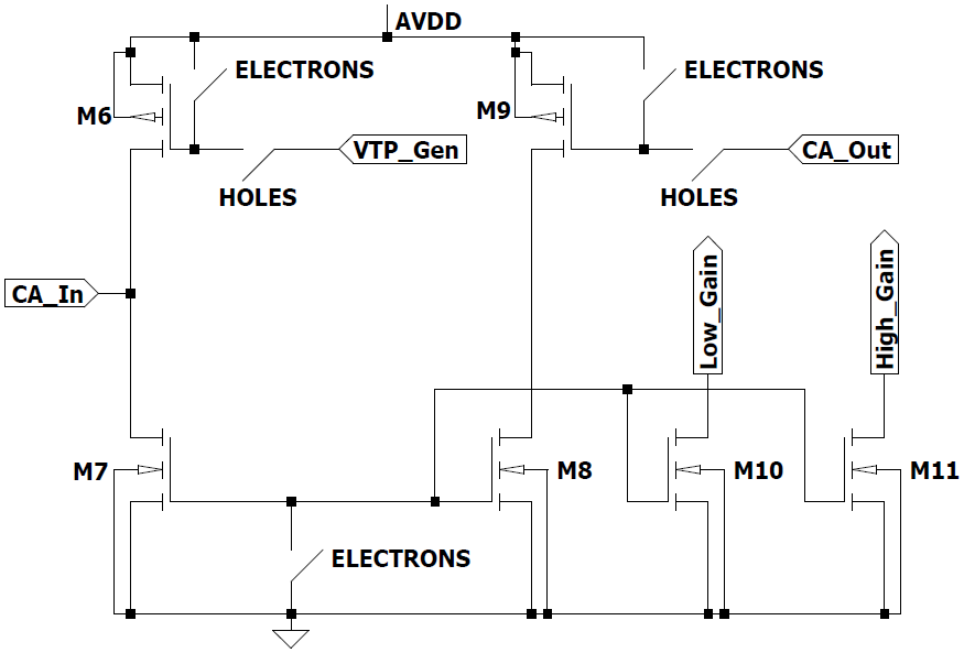

Figure 2.5: Continuous Reset Circuit - Hole Collection

Table 2.7: Device Sizes for Continuous Reset Circuit - Hole Collection

	W (μm)	L (μm)	ng
M6	1	4	1
M7	2	40	1
M8	2	40	1
M9	1	4	1
M10	2	40	1
M11	8	40	4

2.2.3 Threshold voltage generator

As discussed earlier in this chapter, the charge amplifier output is required to idle at a voltage, (V_{TN}, above ground for electron collection and $|V_{TP}|$ below V_{DD} for hole collection. This not only assures the maximum dynamic range but also prevents the pseudo-resistors from entering the cut-off region. Therefore, the Threshold Voltage Generator (TVG) circuit was designed to generate the VTN_Gen and VTP_Gen constant voltages, which correspond to 0.5 V and 2.6 V, respectively.

Equation 2.12 and Equation 2.13 were used to generate V_{TN} and similar expressions were used to generate (V_{DD}-$|V_{TP}|$). Although M_1 and M_3 have elevated threshold voltages, their effects cancel each other. It can be seen from the Equation 2.13, if a conditon of $2 \cdot V_{eff2} = 2 \cdot V_{eff1} = V_{eff3}$ is satisfied, V_{TN} can be obtained at the VTN_Gen output. Devices sizes are given in Table 2.8.

$$V_{GS2} + V_{GS1} - V_{GS3} = VTN\_Gen \tag{2.12}$$

$$V_{TN} + V_{eff2} + V_{eff1} - V_{eff3} = VTN\_Gen \tag{2.13}$$

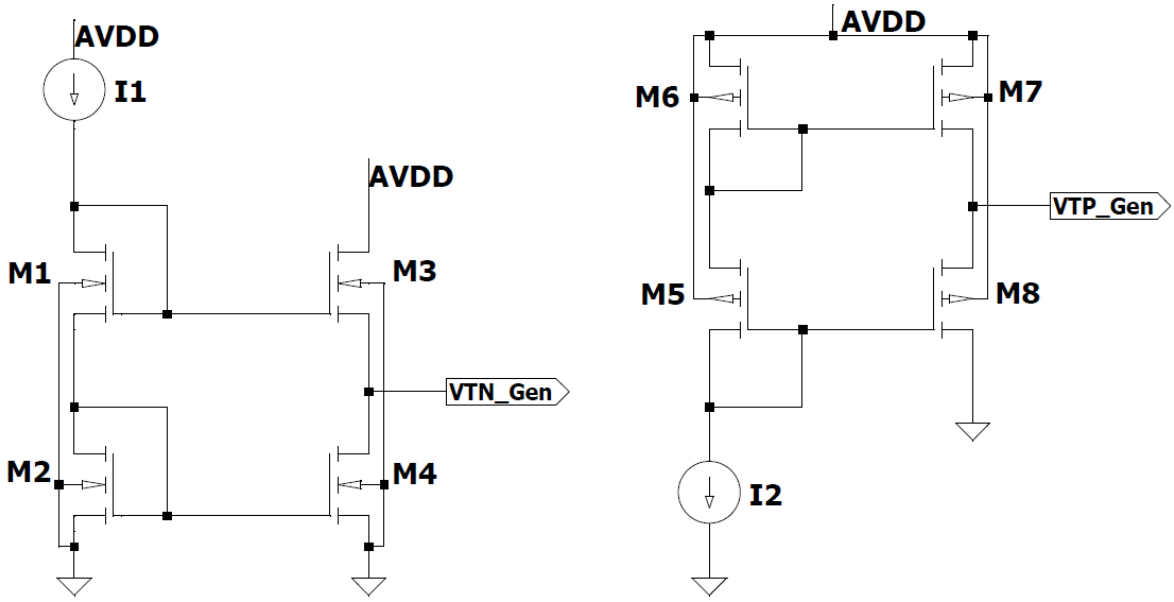

Figure 2.6: Schematic of Threshold Voltage Generator

Table 2.8: Device Sizes for Threshold Voltage Generator

	W (μm)	L (μm)	ng	I_D (μA)
M1	4.5	4	4	46
M2	4.5	4	4	46
M3	4.5	4	1	46
M4	4.5	4	4	46
M5	6	2	4	23
M6	6	2	4	23
M7	6	2	4	23
M8	6	2	1	23

2.2.4 Pulser

It is often inconvenient when working with the HINP5 IC to have to connect the chip to Si-strip detectors. When verifying that the IC is functioning correctly or calibrating,

it is desirable to apply voltage pulses. The Si strip detector generates a current pulse. The current pulse can be simulated using a voltage pulse if one capacitively couples to the input node. Moreover, we have designed the IC so that even or odd channels can be independently pulsed, thereby allowing one to look at crosstalk issues arising between neighboring channels. Alternatively, all channels may also be pulsed if both even and odd pulsing is selected.

The main challenge of using voltage pulser is that charge of both polarities is injected. In order to minimize the amount of charge injected of the "wrong" polarity. In other words, to emulate the charge profile from a silicon strip detector, the rise time of the pulse signal should be very short and the fall time should be comparably long. This way, unwanted charge of the "wrong" polarity will be minimized.

Injecting charge of the "wrong" polarity results in the idle point of the amplifier to exceed (V_{DD}-$|V_{TP}|$) for hole collection for a short period of time. The amplifier output needs to reach its idle point before the next pulse arrives, therefore the pulse repetition rate is limited. The shape factors of the M_0 and M_6 transistors in Figures 2.4 and 2.5 were selected accordingly to help the amplifier output to attain its idle point as fast as possible. The researchers at WUSTL can use pulses with a repetition rate as high as 300 Hz with the HINP5 chip. This was deemed acceptable.

The pulser output is directly connected to the charge amplifier if selected configuration bit, see Figure 2.7. The amplitude of the voltage pulse determines how much charge will be injected into the charge amplifier. The pulser capacitor value was chosen as 7.5 pF. A Verilog-A model for the voltage pulser used by the WUSTL researchers was created in order to verify that our pulser circuit operates correctly. The model can be found in Appendix A.

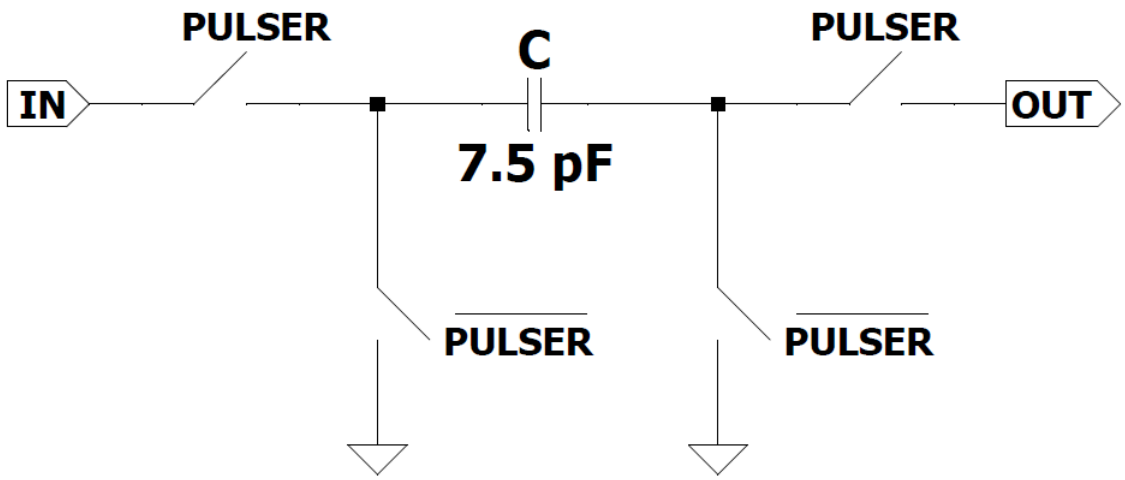

Figure 2.7: Schematic of Pulser

2.2.5 External pre-amplifier

Per the HINP5 specification, the IC must be able to be used with an external charge amplifier. When the external charge amplifier option is selected (via a configuration bit), the low-gain channel output should not be used. An analog multiplexer is used to select either the high-gain output of the internal charge amplifier or the output of the external charge amplifier. The appropriate output is then routed to the input of the high-gain shaper (to be discussed in the next chapter). See Figure 2.8.

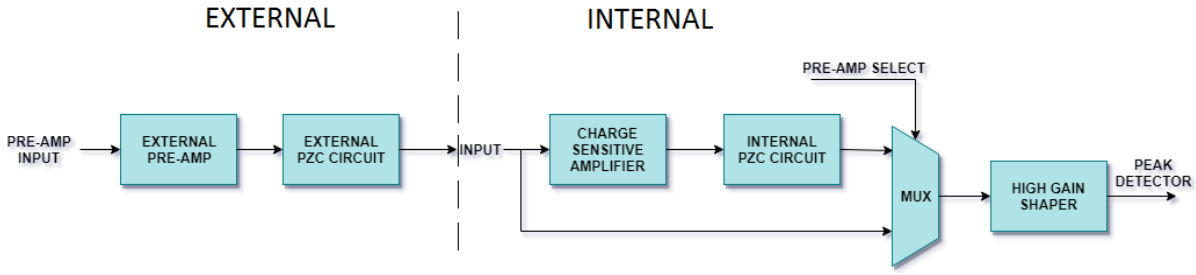

Figure 2.8: Block Diagram with the External Pre-Amplifier Option

2.3 Simulation Results

In this section, the simulation results of the charge amplifier will be discussed. The success of an amplifier can be measured by how well it meets the specification discussed in Section 2.1. It can be seen from the Figure 2.9 that the core amplifier has a unity gain frequency (GBW) at 130 MHz and a low-frequency gain of 98 dB. Table 2.9 shows the comparison between the calculated values in MathCAD and the measured values from the simulation.

Table 2.9: Comparison Between Calculation and Simulation

	Calculation	Simulation
Gain	106 dB	98 dB
GBW	160 MHz	130 MHz
Phase M. ($C_{DET} = 25pF$)	43°	46°
Corner Frequency	2.5 kHz	2.8 kHz
t_r ($C_{DET} = 200pF$)	60 ns	75 ns

From the transient analysis with a detector capacitance of 200 pF, t_r of the amplifier was measured to be 75 ns and t_f was measured to be 50 μs for an energy level of 10 MeV. It should be noted, since pseudo-resistors are used, the decay time constant actually is a function of the output level of the core amplifier (i.e. energy). For lower energy inputs, the decay time constant will be somewhat longer and for energy levels greater than 10 MeV, the decay time constant is somewhat shorter.

2.4 Layout

The charge amplifier core occupies an area of 180 μm x 120 μm (rail-to-rail) and can be seen in Figure 2.10. In the previous design, total area of charge amplifier was

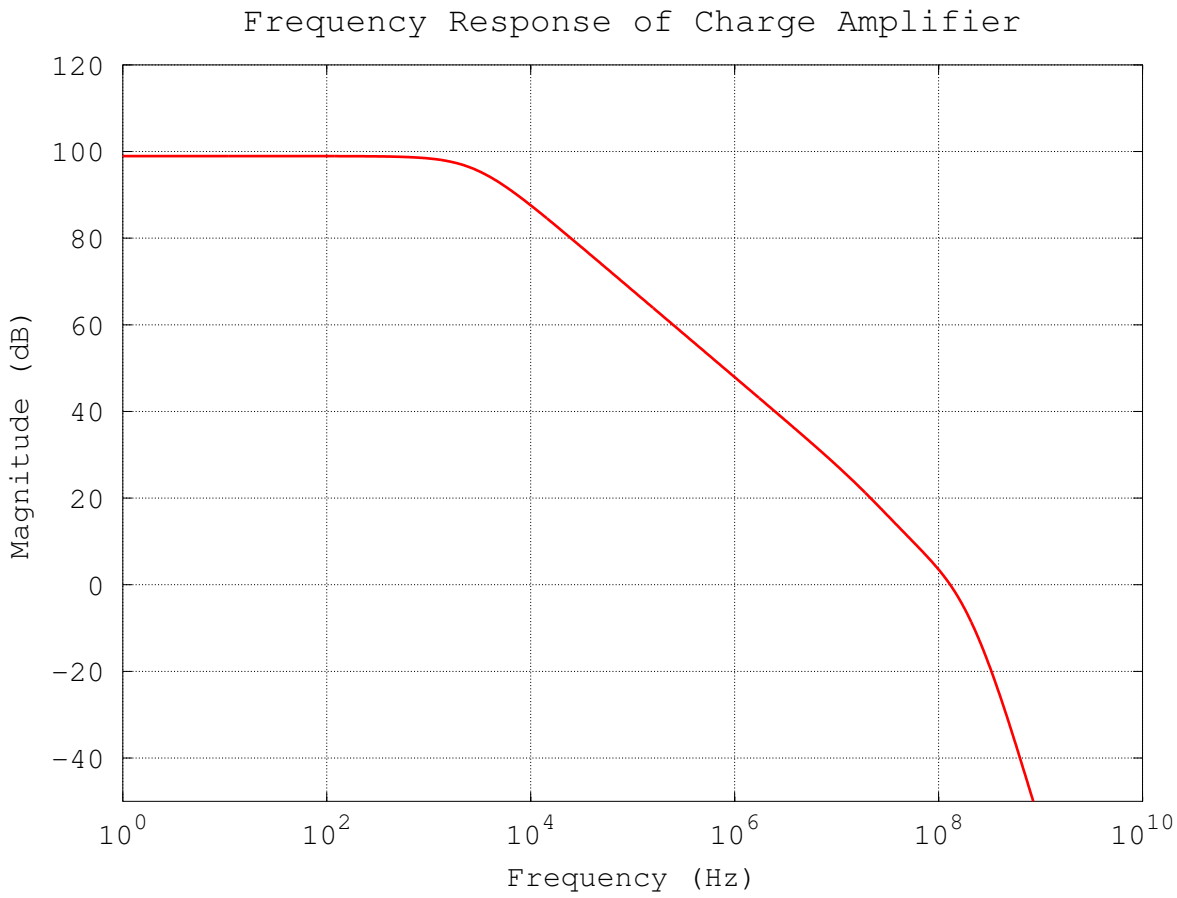

Figure 2.9: Frequency Response of Core Amplifier

occupying larger silicon area than shaper block. On the other hand, in this design, charge amplifier including continuous reset circuit, pole-zero cancellation circuit, threshold voltage generator, bias circuitry and pulser only uses 2/3 of the shaper area. Since new shaper layout has almost same dimensions with the previous design, usage of pseudo MOS resistors and small transistors helped us to reduce silicon area for the charge amplifier by the factor of 2.

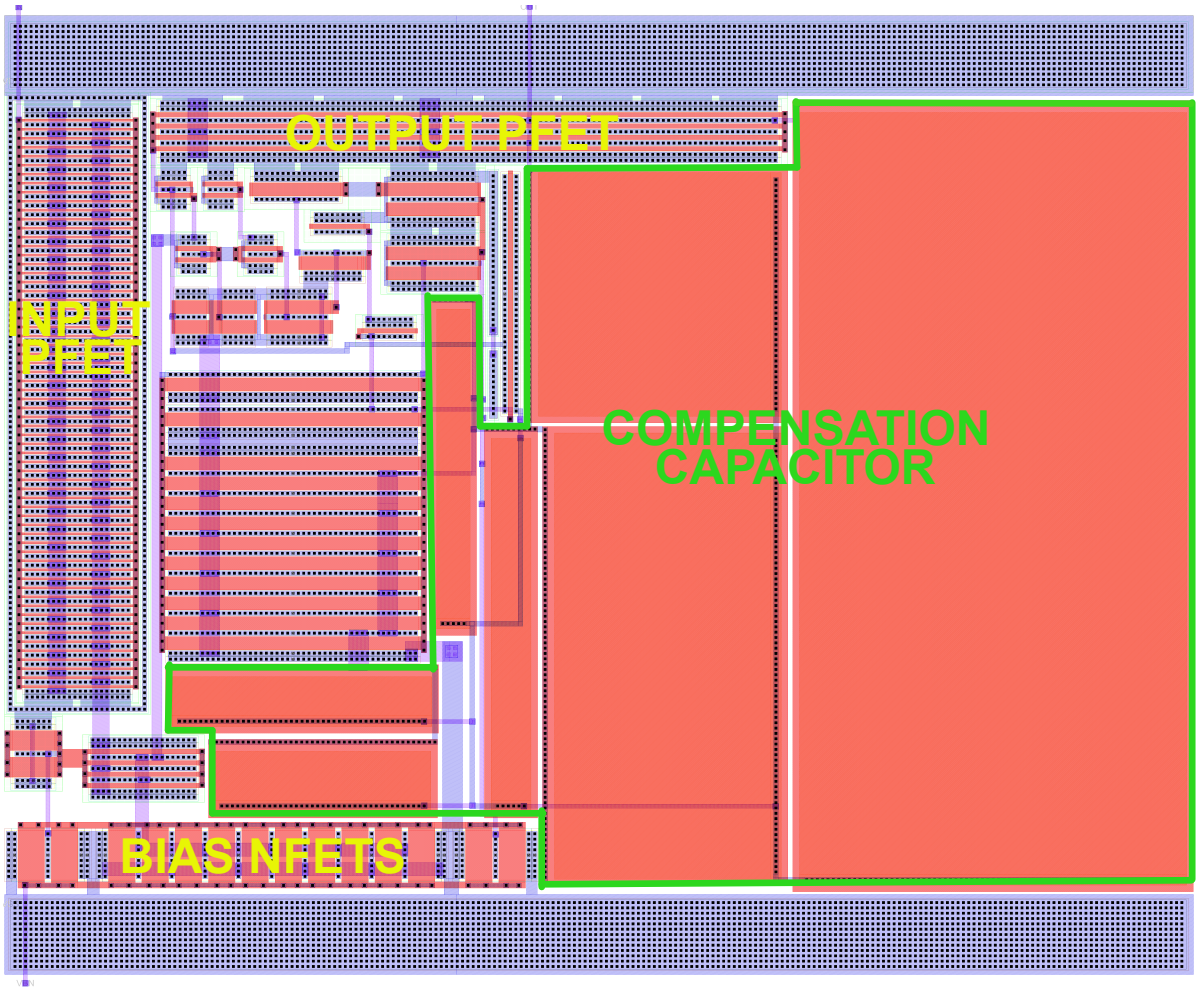

Figure 2.10: Layout of Core Amplifier (OTA)

CHAPTER 3

GAUSSIAN SHAPER

The output of the charge amplifier is a charge packet *i.e.* a current impulse. The shaper is a low-pass filter which transforms the current impulse at the input into a semi-Gaussian shaped voltage at the output. A semi-Gaussian shaped output is desirable because it is very easy to find the peak voltage of gaussian shaped waveform. Also, the signal-to-noise ratio (SNR) is maximized by using a semi-Gaussian shaped signal [De Geronimo and Li, 2011]. The shaper produces a Gaussian shaped pulse whose amplitude is directly proportional to the energy level of the particle which struck the detector. In Figure 2.3, C_{pz1} and C_{pz2} differentiates the step-like signal at the output of the charge amplifier. This results in a narrow current pulse for the input of the shaper.

The shaper properly limits the signal bandwidth to achieve maximum SNR. The voltage transfer function from the output of the charge sensitive amplifier to the output of the shaper is bandpass in nature (center frequency around 300 kHz). Due to the need for the PZC circuit (a resistor shunts the capacitor), the attenuation is not infinite at DC. Rather, a maximum attenuation of approximately 32 dB is achieved for low frequencies (*i.e.* frequencies less than 8 kHz) for an input energy level of 10 MeV. Since the resistance of the pseudo-resistor increases in value as output level decreases, the corner moves to a lower frequency and some additional attenuation is obtained. For higher energy levels, somewhat less attenuation is achieved because of the decrease in resistance of the pseudo-resistors. The bandpass response is quite helpful in rejecting the low-frequency 1/f noise emanating from MOSFETs in the core amplifier. It also helps reduce the low-frequency components of the white noise originating from the Si-strip detector and its associated bias circuits.

While we will discuss the design of the shaper in this section, the reader must recall

that the linear branch (please refer Figure 1.5 actually contains two copies of the shaper circuit, one to service the low-gain (x 1) output from the charge amplifier and a second one to service the high-gain (x 4) output.

3.1 Design Specifications

The design specifications for the shaper are the following;

- Peaking time should be between 1 μs and 1.5 μs.
- Total noise at the output of the high-gain shaper should be less than 25 keV.
- Very high dynamic range (at least 72 dB).
- Shaper must return to baseline (better than 1 percent) within 5 μs.
- Very high linearity (Residuals less than a 5 percent over the range deemed "linear")

3.2 Design

One way to construct a semi-Gaussian shaper (see Figure 3.1) is to cascade a single differentiator and n integrators [Spieler, 2005]. The n integrators and one differentiator each add one pole, thus determining the order of the filter (n+1). The classical shaper configurations, however, have limitations on the maximum achievable dynamic range. Therefore, De Geronimo offered a topology called Delayed Dissipative Feedback (DDF) based on delaying the resistive feedback from the furthest available nodes in a signal path [De Geronimo and Li, 2011]. A third-order shaper employing DDF is shown in Figure 3.2. His claim is that a factor of two higher dynamic range can be obtained due to the use of this very low noise configuration.

In this process, a single supply voltage of 3.3 V was used. Thus, an analog ground (AGND) of 1.65 V was generated to provide a baseline for the shaper. Higher-order filters generate Gaussian shapes closer to the optimum shape with lower noise properties; however,

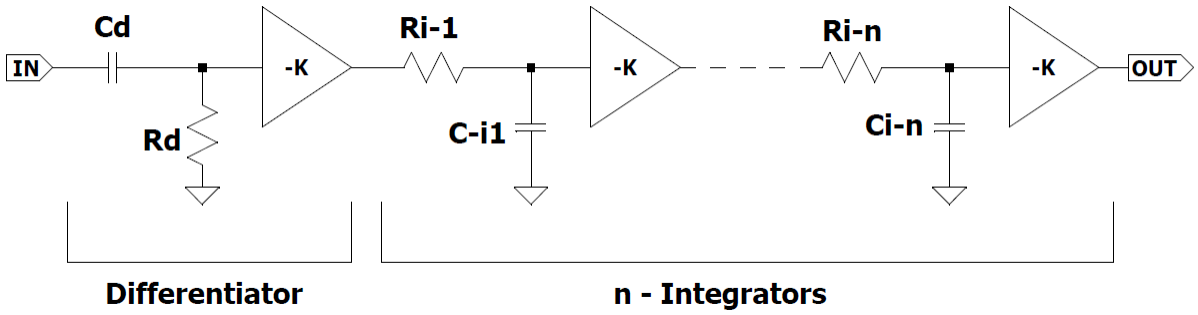

Figure 3.1: Classical Configuration for a Shaper

the filter becomes more complex to design and enlarges the silicon area. After careful consideration, a third-order shaper was implemented in order to obtain the semi-Gaussian signal shape. The third-order shaper contributes three poles to the transfer function, one of them is a real pole and other two are complex conjugates [De Geronimo and Li, 2011]. The performance of the shaper is optimized if all of the amplifiers are operating rail-to-rail.

To assure rail-to-rail operation for all amplifiers and to achieve maximum signal-to-noise ratio, the equations below must be satisfied for the third order shaper.

$$A_{v2} = A_{v3} = 1.08 \tag{3.1}$$

$$\epsilon_p = \frac{\tau_p}{\omega_0} = 0.57, \tag{3.2}$$

$$\alpha_x \geq 0.35 \tag{3.3}$$

$$C_x \approx C_2/3 \tag{3.4}$$

The transfer function of the third-order shaper with DDF configuration is given in Equation 3.5 [De Geronimo and Li, 2011].

$$\frac{V_{out}}{I_{in}} = \frac{R_1}{s^3 \cdot \frac{\tau_1 \cdot \tau_2 \cdot \tau_3}{A_{v2} \cdot A_{v3}} + s^2 \cdot \frac{\tau_1 \cdot [\tau_2 \cdot (1 - a_x) + \tau_3]}{A_{v2} \cdot A_{v3}} + s \cdot \frac{\tau_1}{A_{v2} \cdot A_{v3}} + 1} \tag{3.5}$$

Design coefficients for the different orders of shapers with complex-conjugate poles are given in the Table 3.1, where CU-n implies the order of the filter and τ_p corresponds

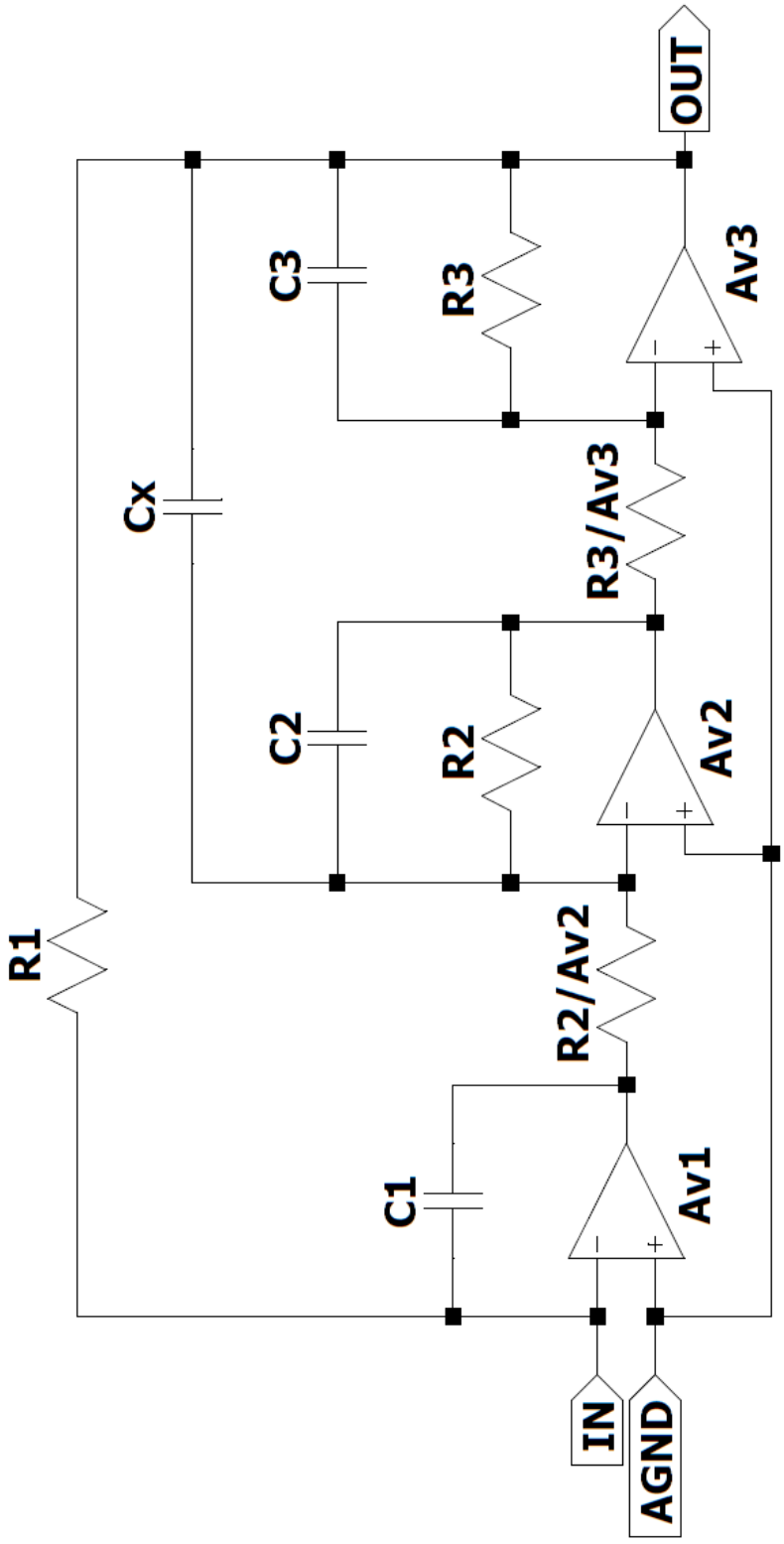

Figure 3.2: Schematic of Third-Order Shaper with DDF Configuration

to peaking time. Resistor and capacitor values can be easily calculated with the given Equations 3.5 and the Table 3.5. The resulting component values can be found in Table 3.2.

Table 3.1: Design Coefficients for the Different Order of Shapers

	$\omega_0\tau_p$	$\omega_1\tau_p$	Q_1	$\omega_2\tau_p$	Q_2	$\omega_3\tau_p$	Q_3
CU-2	-	1.031	0.541	-	-	-	-
→ CU-3	1.793	1.976	0.606	-	-	-	-
CU-4	-	2.471	0.514	2.812	0.672	-	-
CU-5	2.945	3.066	0.543	3.532	0.736	-	-
CU-6	-	3.400	0.507	3.612	0.576	4.178	0.797
CU-7	3.758	3.842	0.523	4.128	0.61	4.775	0.855

The op amps used in the shaper design must be designed correctly in order to achieve rail-to-rail operation. Therefore, a Verilog-A model was written in order to obtain specifications for the op amps used in the shaper. As a result, the need for high GBW ($>$ 40 MHz), modest slew rate (2.3 $\frac{V}{\mu s}$) and intermediate gain ($>$ 60 dB) emerged. An op amp from the AMS analog standard cell library which meets design specifications was used in the shaper circuit. The schematic of the op amp can be seen in Figure 3.3 and device sizes are provided in Table 3.3.

In the previous design, two different peak samplers were used for two different polarities; namely, hole collection and electron collection. As we shall see in the next chapter of this thesis, the design of a peak sampler is extremely challenging. Rather than using a different peak sampler for each polarity, an inverting gain amplifier was added to the output of the shaper as shown in Figure 1.5. A configuration bit is used to select either inverted or non-inverted shaper output. The inverted output is needed for hole collection. The same op amp used in the shaper is used in the inverting gain amplifier. The noise of the inverting gain amplifier only degrades the noise performance by a few keV (noise analysis provided in next section of this thesis).

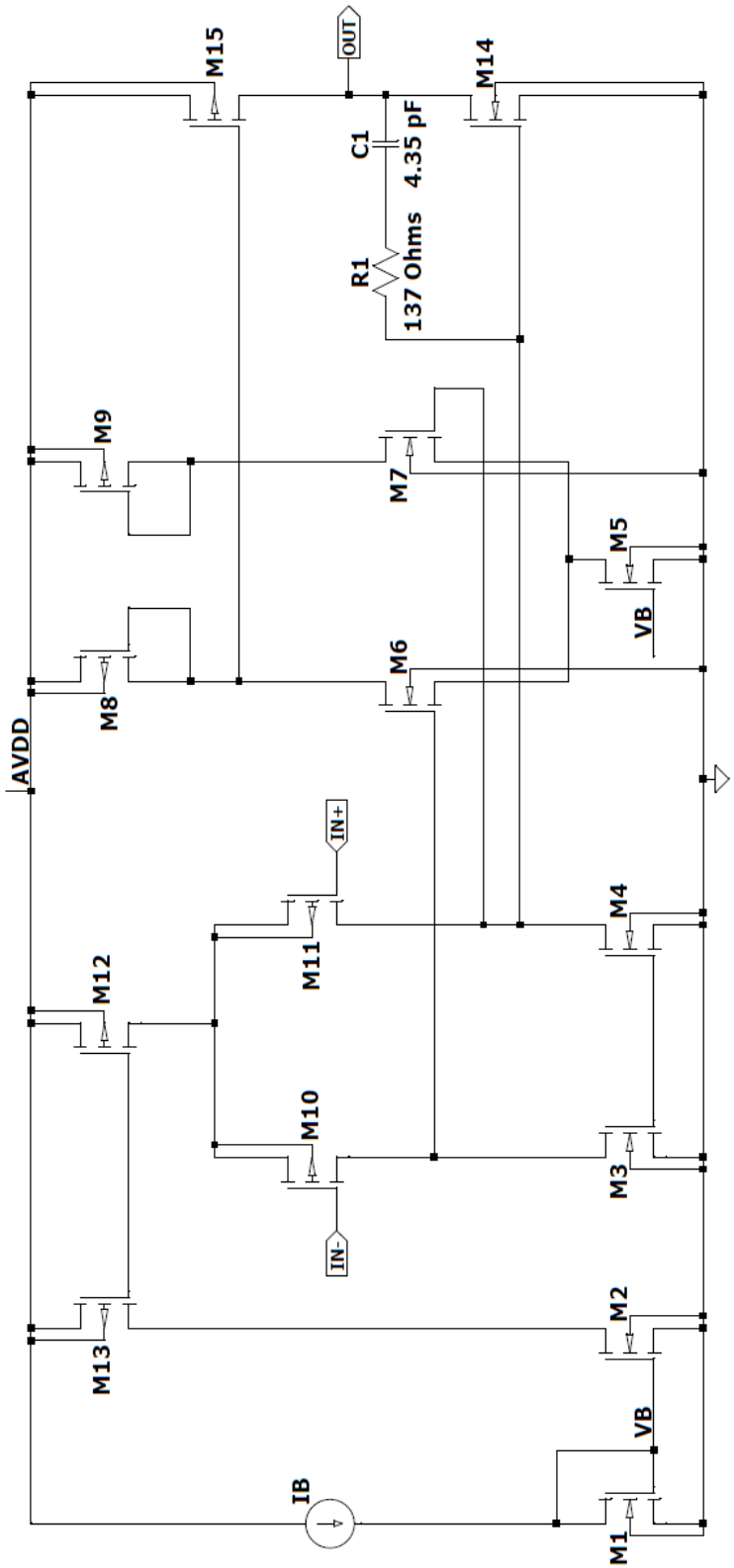

Figure 3.3: Schematic of Op-Amp Used in Shaper

Table 3.2: Component Values of Gaussian Shaper

Component	Value
R1	186 kΩ
R2	82 kΩ
R3	32 kΩ
R2/A_{v2}	76 kΩ
R3/A_{v3}	30 kΩ
C1	10.5 pF
C2	7.5 pF
C3	7.5 pF
C_x	3.5 pF

3.3 Simulation Results

First, the op amp which was chosen from the standard cell library was simulated. The simulation results of the op amp used in shaper design can be found in Table 3.4. In order to reduce the power dissipation, a decision was made to operate the op amp with a bias current of 5.75 μA which is one-half the recommended bias. When operated at full bias, the op amp had a GBW which was larger than needed.

A transient analysis was also performed. An accurate semi-Gaussian shape was obtained at the output of the shaper with peaking time of approximately 1 μs. The pole-zero cancellation discussed in Section 2.2.2, as expected, allows for a quick return to baseline. It can be seen from Figure 3.5 the high-gain shaper has four times more gain than the low-gain shaper. Finally, we measured the maximum slope of the semi-Gaussian shaped output. With a full-scale output, the maximum slope was 2.3 $\frac{V}{\mu s}$. This is important because it sets the slew rate specification for both the op amp in the shaper and for the peak detector.

Table 3.3: Device Sizes for Shaper Op Amp (with recommended bias currents)

	W (μm)	L (μm)	Gates	I_D (μA)
M1	20	1.25	1	10
M2	20	1.25	2	20
M3	12	1	1	
M4	12	1	1	
M5	20	1.25	30	300
M6	80	0.5	1	150
M7	80	0.5	1	150
M8	30	0.5	1	150
M9	30	0.5	1	150
M10	250	1	1	
M11	250	1	1	
M12	120	1	8	160
M13	120	1	1	20
M14	200	1	1	1200
M15	210	0.5	1	1200

Table 3.4: Characterization of Shaper Op Amp

Component	Simulation ($I_B = 11.5\ \mu A$)	Simulation ($I_B = 5.75\ \mu A$)
GBW	100 MHz	45 MHz
Low Fr. Gain	86 dB	89 dB
SR	300 V/μs	160 V/μs
Phase M.	74°	90°

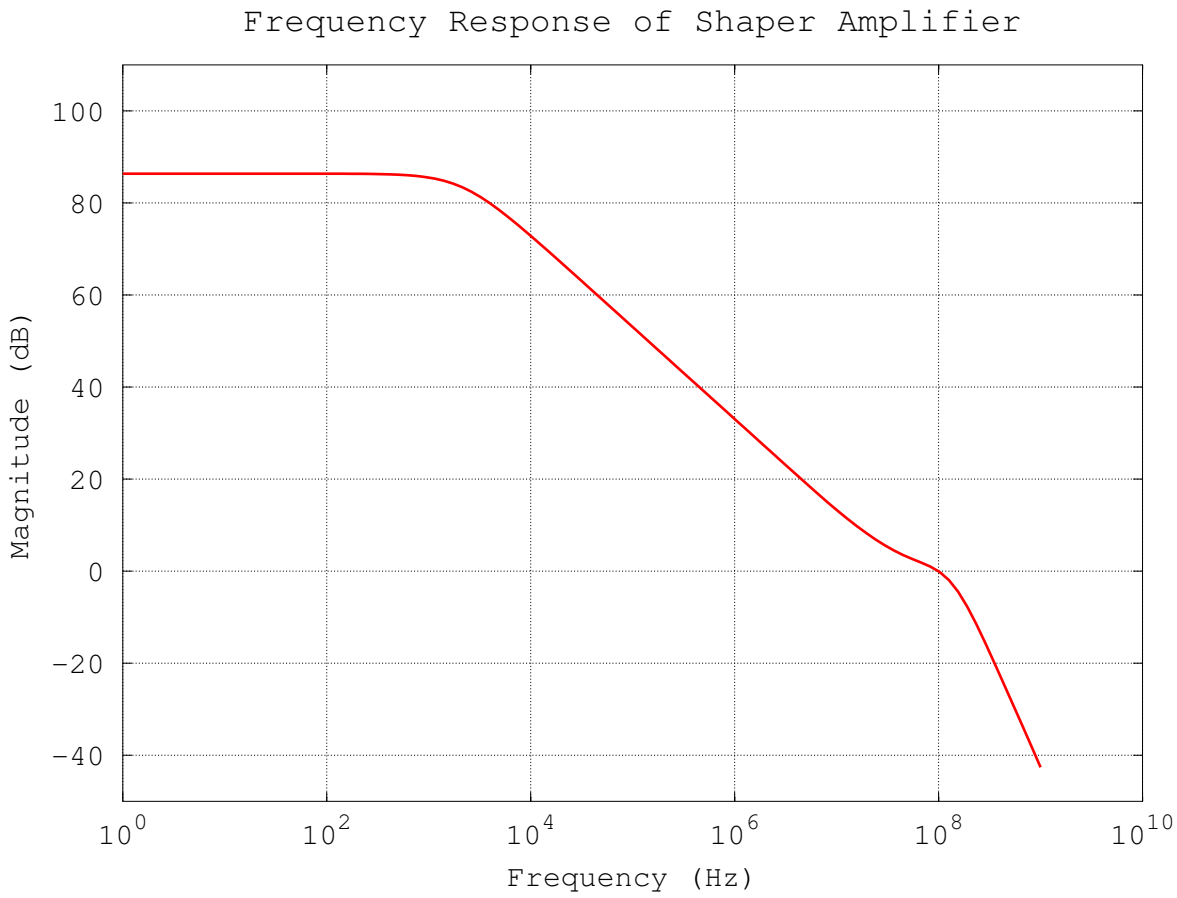

Figure 3.4: Frequency Response of Shaper Op Amp

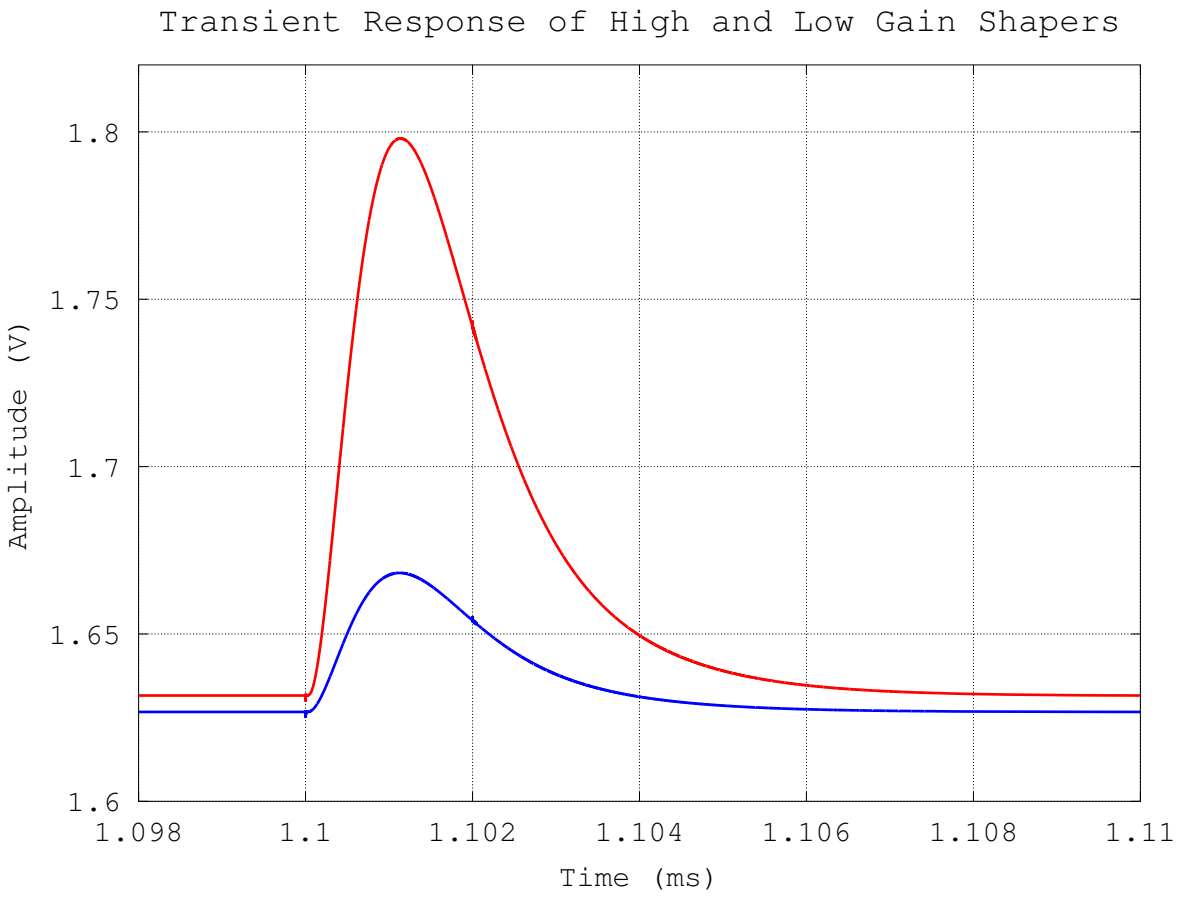

Figure 3.5: Transient Response of Shaper

Table 3.5: Top 5 Noise Contributors at the Output of the High Gain Shaper

Device	Noise Type	Noise % of Total
Detector	Shot	42.51
Detector	Thermal	21.99
CA/M_0	Thermal	11.29
CA/M_8	Thermal	3.40
CA/M_6	Thermal	3.36

The other important parameter for the shaper is the total integrated noise at the output of the shaper. Our design objective was to have an energy resolution of better than 25 keV with the high-gain shaper and better than 100 keV with the low-gain shaper. It can be observed from the Table 3.5 that the silicon strip detector is the largest noise contributor due to its leakage current and bias resistance. Moreover, input transistor M_0 is the dominant source of the noise after the detector, which is an another indicator of a properly designed charge amplifier.

An energy resolution of 18 keV (electron collection) and 20 keV (hole collection) was achieved with a detector capacitance of 100 pF. Thus, the noise specification was met. However, the peak detector and the off-chip driver circuits will degrade this to some extent. Simulations, however, indicate that even with these additional contributions to the noise a resolution of better than 25 keV is expected.

Energy resolution (for both gain modes) as a function of detector capacitance (for both hole and electron collection) is plotted in Figure 3.6. Moreover, the noise slope is excellent. The noise slope is 67 $\frac{eV}{pF}$ in high-gain mode and 20 $\frac{eV}{pF}$ in low-gain mode. The resolution is significantly better than that obtained in previous HINP designs.

It is very important that the response be linear. Therefore, both shapers' linearity properties were investigated and plotted to determine the dynamic range that they can

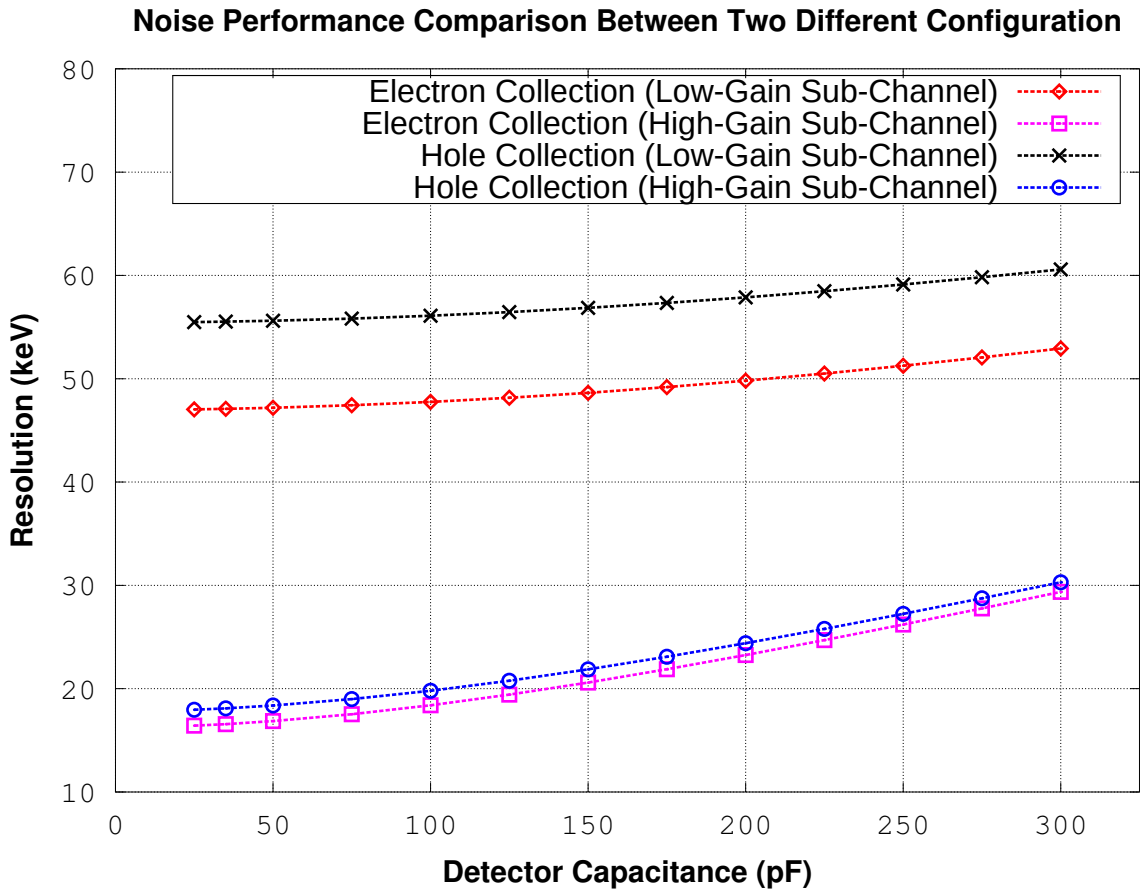

Figure 3.6: Energy Resolution of the Linear Branch

support. A Verilog-A model for a Si-trip detector was created to characterize the response to energy input from 10keV to 500 MeV. An ideal peak detector was modeled using Verilog-A. This was created to characterize the linear branch up until peak detector block. Both of the models can be found in Appendix A. The Octave scripts to create linearity and noise plots can be found in Appendix B. A Tcl (Tool Command Language) script was written to separate 40 Monte Carlo runs from each other which are located in the same file, see Appendix C.

Forty Monte Carlo simulations were performed for both high gain and low gain shapers to observe spread under mismatch and process variations. Figures 3.7 and 3.8 show the typical run without the variations. In the top plots, the blue line (best-fit line) demonstrates that the channel is linear. In the bottom plot, residuals were shown for the whole energy range. The spread can be found in Figures 3.9 and 3.10. The full-scale range only changes by roughly $\pm$ 10 % over all process corners and expected mismatch.

3.4 Layout

The shaper occupies an area of 1 mm x 120 μm (rail-to-rail) in Figure 3.11. When it is compared to the previous design (HINP4), shaper layout was shrinked by $\approx$40%, even with the addition of an extra inverting gain amplifier. Figure 3.11 is annotated based on shaper schematic given in Figure 3.2

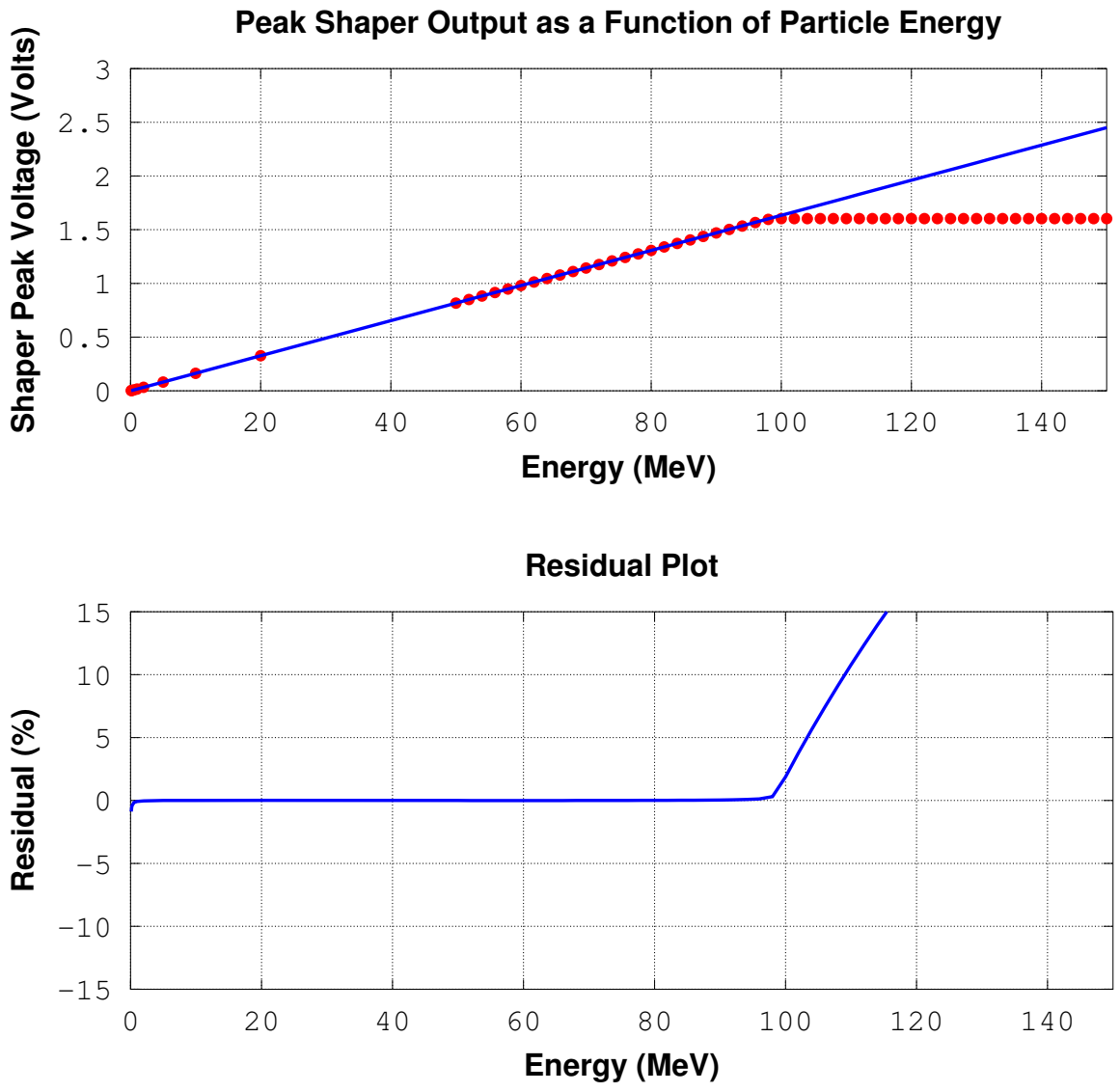

Figure 3.7: Typical Linearity Run - High Gain Shaper

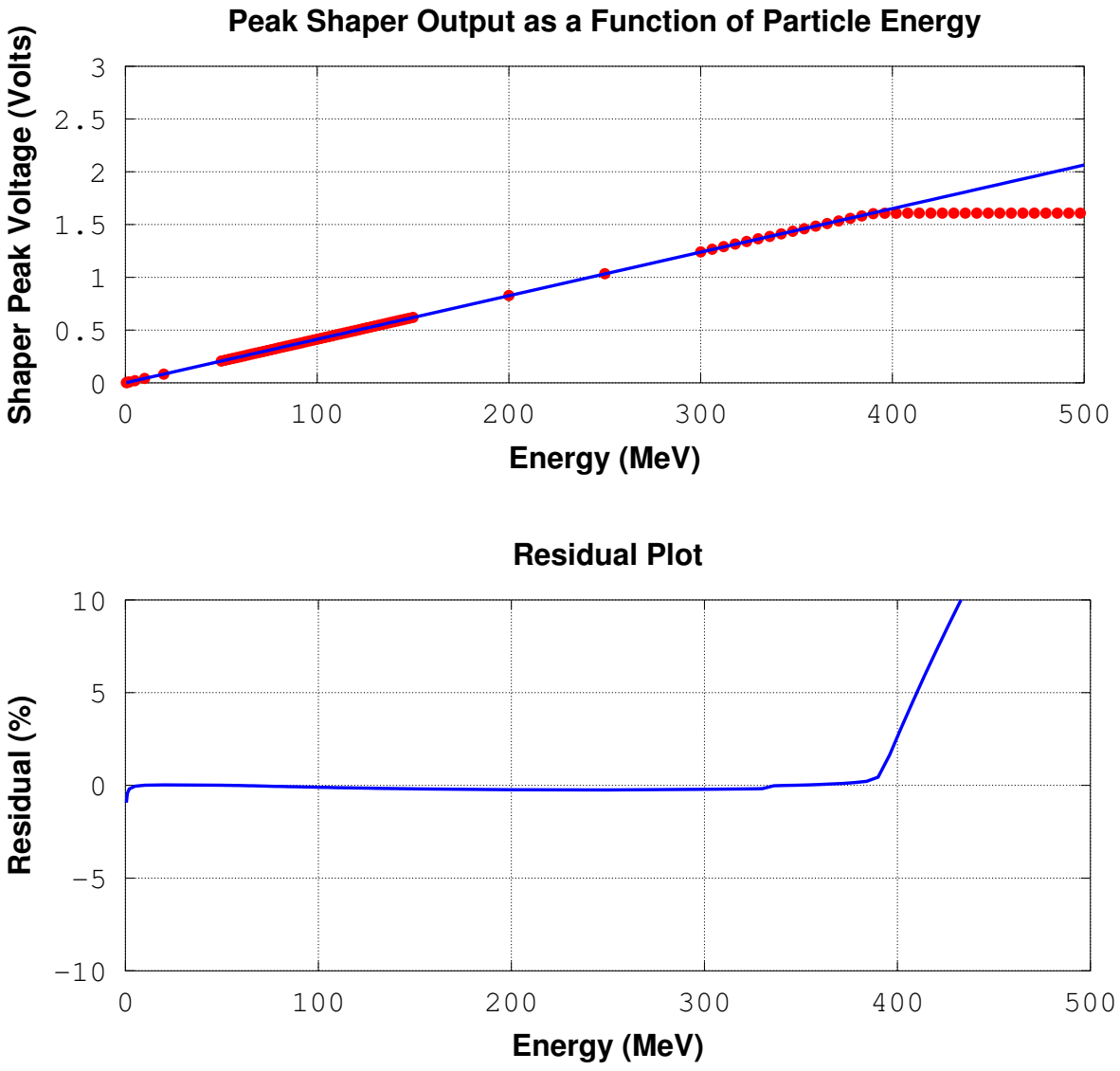

Figure 3.8: Typical Linearity Run - Low Gain Shaper

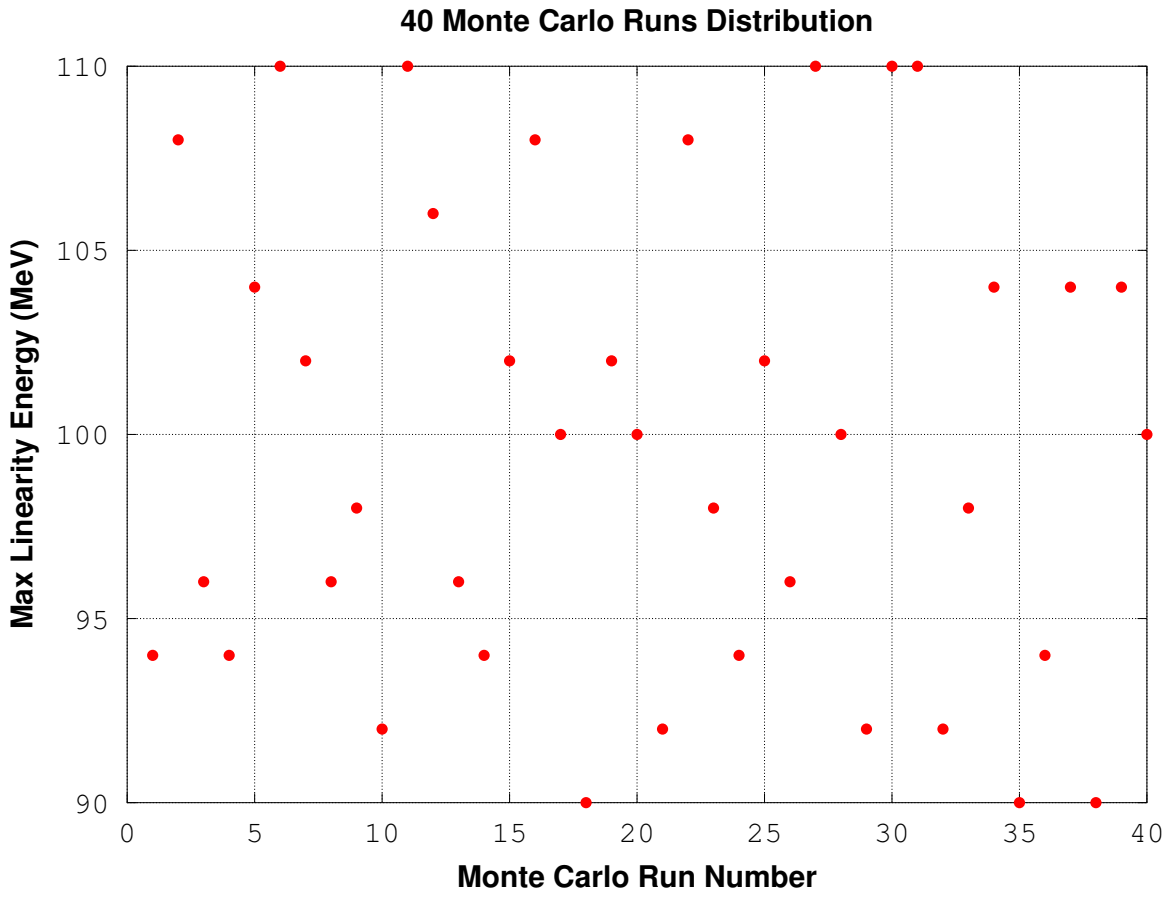

Figure 3.9: 40 Monte Carlo Linearity Runs - High Gain Shaper

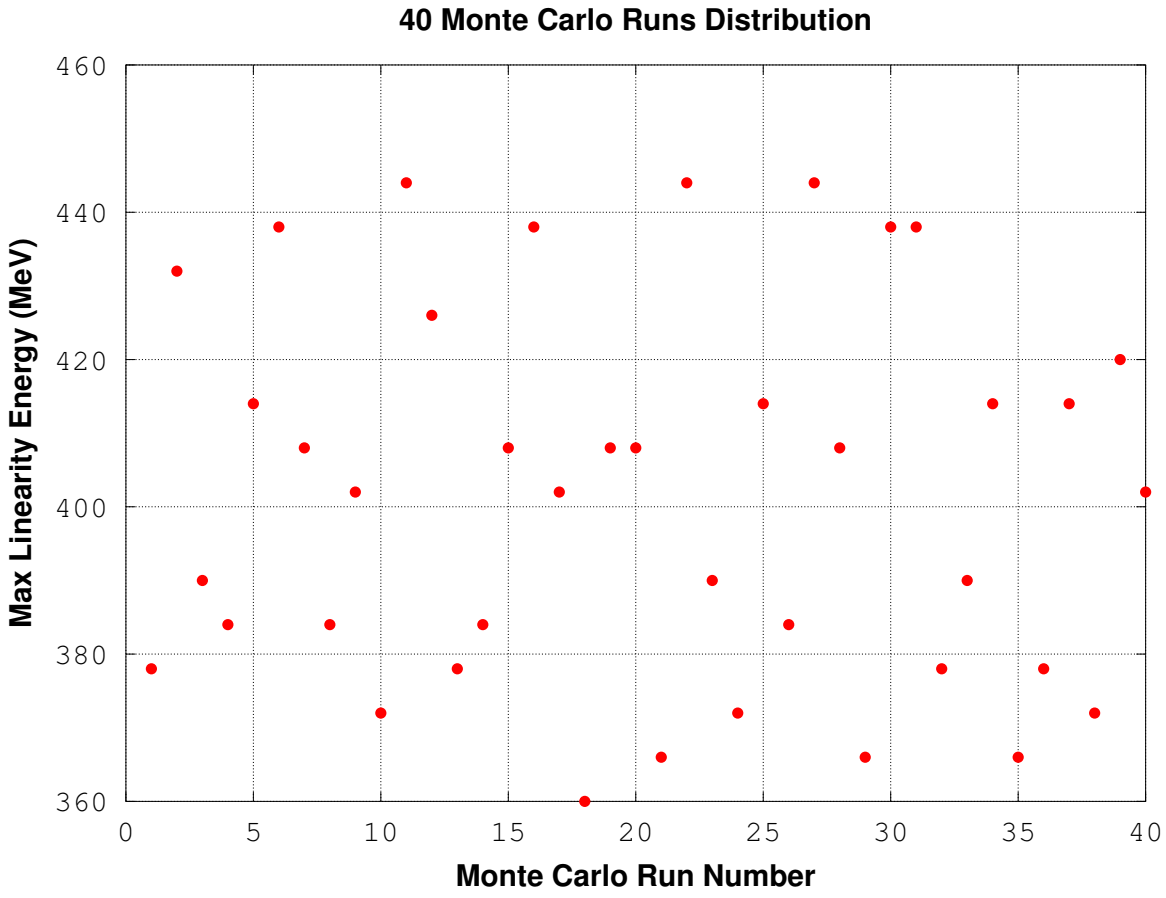

Figure 3.10: 40 Monte Carlo Linearity Runs - Low Gain Shaper

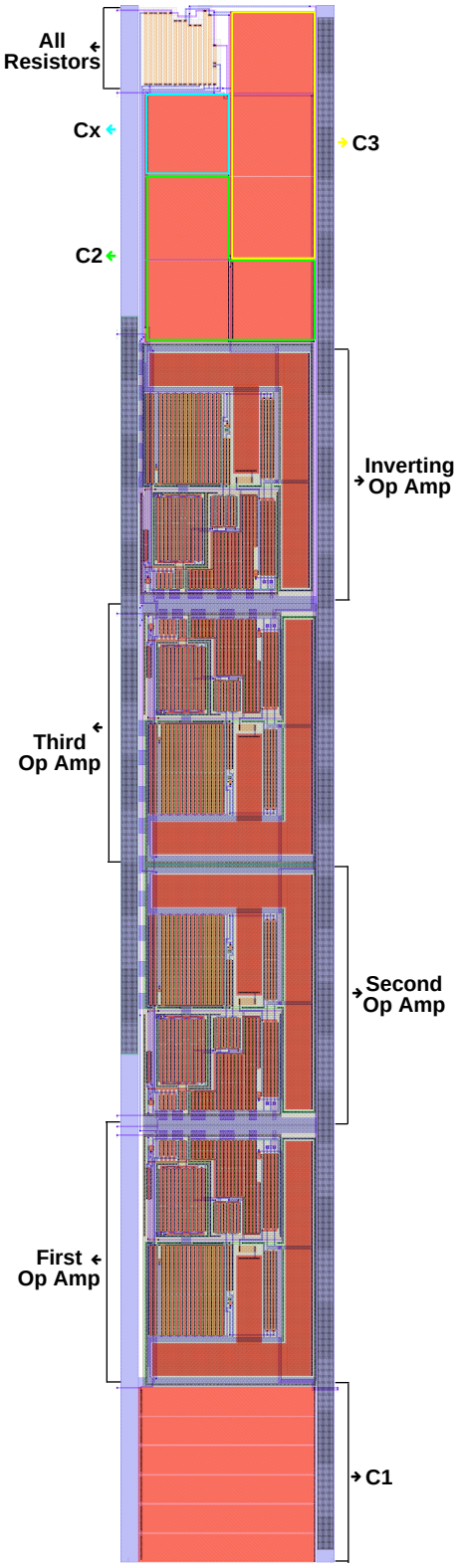

Figure 3.11: Shaper Layout

CHAPTER 4

PEAK DETECTOR

The peak detection circuits are very common in nuclear signal processing applications. The semi-Gaussian shape generated at the output of the shaper block has an amplitude directly proportional to the particle's energy. Therefore, amplitude of the peak point needs to be measured to obtain energy levels of the particles. To do that, generally, peak-detect-and-hold (PDH) circuits are implemented. PDH systems are made of an amplifier, a MOS current source as the rectifying component, and a hold capacitor.

In this thesis work, a two-phase PDH structure, also known as correlated double sampling, was implemented due to limitations of the classical PDH configuration on accuracy. The classical PDH configuration is vulnerable to static and dynamic errors such as offset, finite gain, common-mode rejection (CMRR), parasitic capacitive coupling and slew rate[De Geronimo et al., 2002a]. In two-phase PDH structures, peak amplitude is stored into a capacitor during the *write* phase and the value stored in capacitor is read out during the *read* phase. The two biggest advantages of the two-phase PDH configuration are: (1) it is offset and common-mode errors free and (2) it minimizes the impact of the parasitic capacitances[De Geronimo et al., 2002b].

4.1 Design Specifications

The design specifications for the peak detector are the following:

- High accuracy, less than $\approx 5\%$ error.
- Very high dynamic range.
- Adequate phase margin in both *write* and *read* modes.
- Analog multiplexer to select between polarities.

- Must possess a slew rate of at least 2.3 $\frac{V}{\mu s}$ (per the discussion in previous section of this thesis)

4.2 Design

As we discussed in Chapter 3, the peak detector module receives two outputs, one directly comes from the shaper output and the other one comes from the inverting gain amplifier. A 2-to-1 analog multiplexer was implemented to select between these two outputs based on the polarity. A digital select bit for the analog multiplexer is provided by the configuration register which is located in the common channel. The negative peak detector schematic can be found in Figure 4.1.

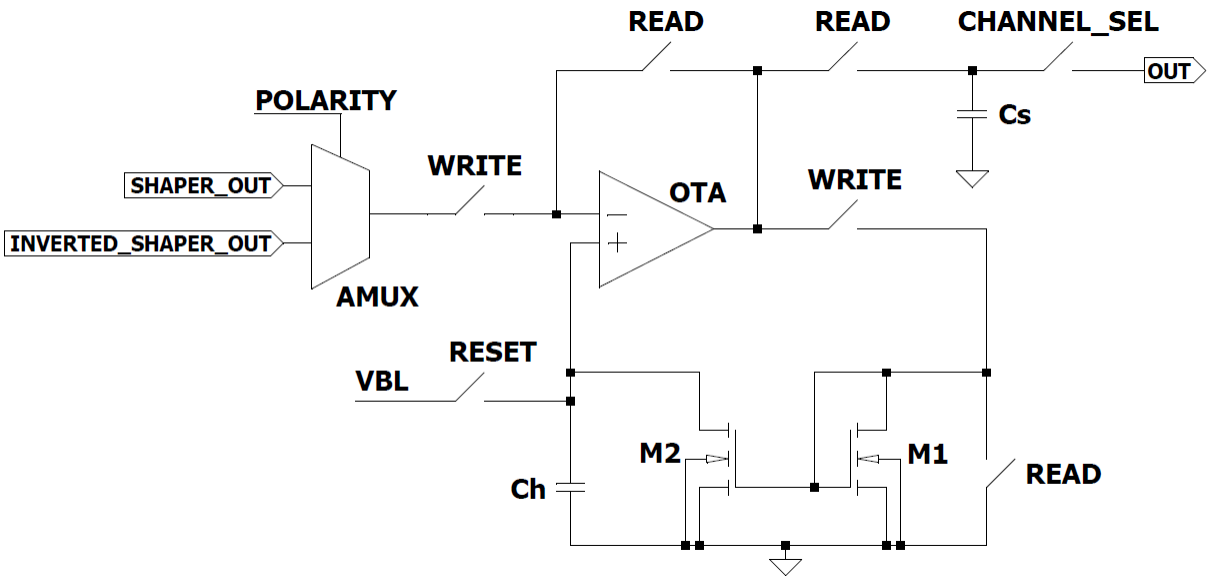

Figure 4.1: Negative Peak Detector

In two-phase peak detect-and-hold systems, three signals are necessary to control the peak detection loop, namely, **reset**, **write**, and **read**. The capacitor is pre-charged to 1.8 V (significantly greater than the 1.65 V AGND) when **reset** is asserted.

During the *write* mode (see Figure 4.2) the semi-Gaussian shaped pulse is being tracked and stored on capacitor, C_H. When the input voltage to the OTA is less than the

voltage across C_H, transistors M_1 and M_2 conduct. The OTA will adjust its output in order to make the voltage across the capacitor match the voltage at its input (negative feedback). However, if the input voltage is greater than the voltage across the capacitor, the loop opens and the capacitor voltage remains constant.

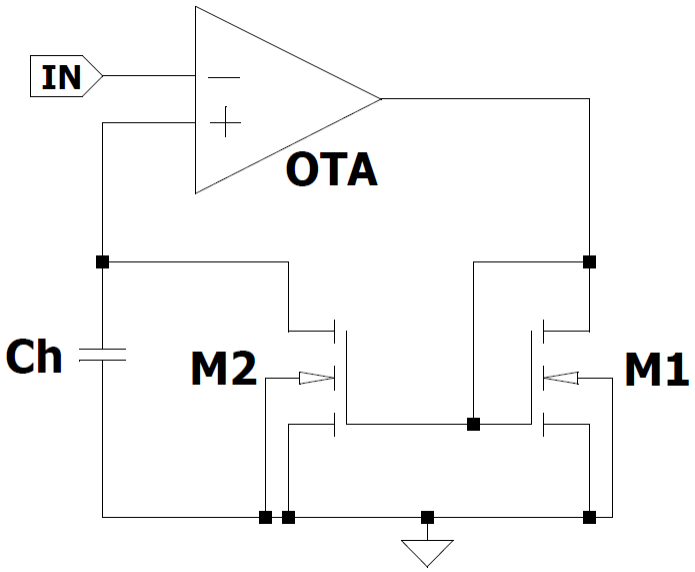

Figure 4.2: Write Mode

During *read* mode (see Figure 4.3), the OTA operates as a unity gain follower, and the value stored on the capacitor can be read out. However, the output is read out using a shared bus so one additional switch is needed to select the channel when it must drive the bus. The digital control bit (**chan_sel**) is generated by the digital readout electronics in the common channel of the chip. The stability capacitor, C_S, is needed to ensure that the OTA has an acceptable phase margin during readout. Also while in read mode, transistors M_1 and M_2 are tuned off.

When a particle strikes the detector, the CFD (Constant Fraction Discriminator) in the timing branch produces a signal that marks the arrival of the charge packet. The digital logic in the channel creates a narrow trigger pulse (**CFDnarrow**) approximately 5 ns wide. An inverted version of this signal drives the active low reset terminal of

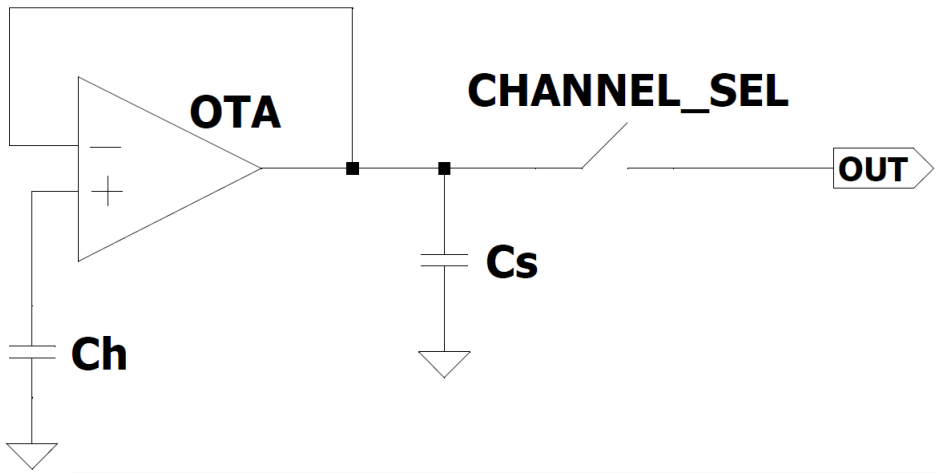

Figure 4.3: Read Mode

the D flip-flop (see Figure 4.4). This should force the peak detector into *write* mode. Simultaneously, the digital control will de-assert **reset**.

The read and write signals are generated by the control circuits which are illustrated in Figure 4.4. The **reset** is logically OR'ed with the output of the flip-flop because the peak detector must be placed in read mode when **reset** is asserted. When the input to the two-phase clock generator goes high, **read** will be high and **write** will be low. A two-phase clock ensures that all connections in the peak detector are broken before new connections are made.

Once the peak has been captured, it is desirable for the peak detector to return to *read* mode automatically. There are two reasons for this: (1) unwise to continue to search for peaks (2) the OTA would have an unacceptable phase margin. As described above, entering *read* mode connects a stabilizing capacitor to the OTA output.

This is accomplished by using a comparator from the analog standard cell library which compares the OTA output with a 250 mV threshold. When the shaper output transitions negative, significant current will flow in transistor M_1 and the gate-to-source voltage will go above a NFET threshold voltage causing the comparator to transition high. However, when the peak is reached, the current flowing in M_1 will tend toward

zero and the gate-to-source voltage of M_1 will drop below the 250 mV threshold thereby causing the comparator output to go back low. An inverter is added at the output of the comparator because the D flip-flop is positive edge-triggered. The peak detector stays in *write* mode for the peaking time of the shaper (≈1 μs).

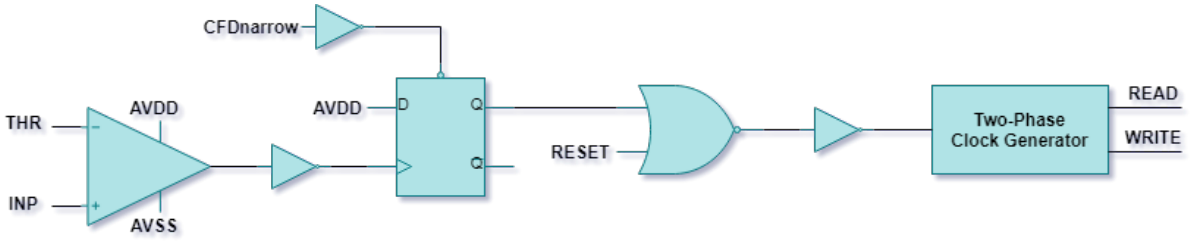

Figure 4.4: Control Circuit

A small-signal analysis was performed on the peak detector while in *write* mode. The small-signal equivalent circuit for the loop is presented in Figure 4.5. An expression for the DC loop gain is given in Equation 4.1.

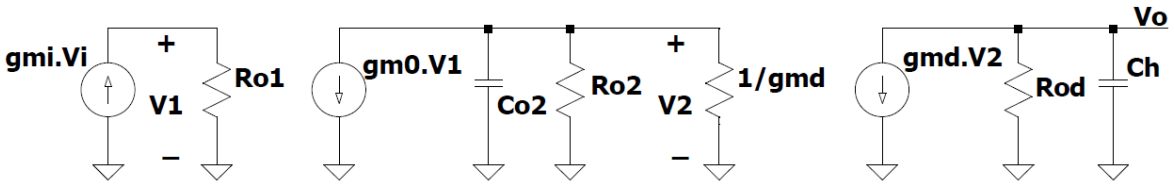

Figure 4.5: Small Signal Analysis of the Peak Detector

$$T(0) = g_{mi} \cdot R_{o1} \cdot g_{m0} \cdot \frac{1}{G_{o2} + g_{md}} \cdot g_{md} \cdot R_{od} \tag{4.1}$$

It is necessary to consider the loop gain for two cases: (1) large energy and on steep slope of Gaussian shape and (2) low energy and near peak of Gaussian. In other words, for case (1) the current flowing in M_1 is maximum while for case (2) the current is minimum.

For case (1) the DC loop gain is given by Equation 4.2. We need a DC loop gain of at least 60 dB to avoid finite gain errors. Care must be taken if this is to be achieved since

R_{od} (output resistance of M_2) will be small if near minimum length is chosen. Choosing M_2 to have minimum length is optimal from frequency response perspective.

$$T(0) = g_{mi} \cdot R_{o1} \cdot g_{m0} \cdot R_{od} \tag{4.2}$$

One wants the pole associated with the output of the OTA to always be a parasitic pole while the pole associated with the hold capacitor should always be the dominnt pole. The unity gain frequency, w_u, of the loop always should be less than or equal to the parasitic pole location, w_p, to provide at least 45° of phase margin. This condition is given in Equation 4.3. However, for case (1), the inequality is easily statisfied.

$$w_u = \frac{g_{mi} \cdot R_{o1} \cdot g_{m0}}{C_H} \leq \frac{g_{md}}{C_{o2}} = w_p \tag{4.3}$$

For case (2), the gain expression turns into a Equation 4.4. In this case, the loop gain is always high enough and it is not a concern.

$$T(0) = (g_{mi} \cdot R_{o1}) \cdot (g_{m0} \cdot R_{o2}) \cdot (g_{md} \cdot R_{od}) = A_0 \cdot (g_{md} \cdot R_{od}) \tag{4.4}$$

For case (2), the unity gain frequency needs careful consideration and it has to be significantly higher than the corner frequency of the shaper, which is 300 kHz.

$$w_u = A_0 \cdot \frac{g_{md}}{G_{o2}} \geq 2 \cdot \pi \cdot (300kHz) \tag{4.5}$$

The unity gain frequency expression, w_u, is given in Equation 4.6. In terms of stability, this value should be less than or equal to parasitic pole location, w_p, to provide at least 45° of phase margin.

$$w_u = A_0 \cdot \frac{g_{md}}{G_{o2}} \leq \frac{G_{o2}}{C_{o2}} = w_p \tag{4.6}$$

This is a very difficult pair of constraints to meet for high dynamic range applications such as ours. Making transistors M_1 and M_2 very wide helps one satisfy Equation 4.5 by increasing g_{md} but this increases C_{o2} and makes it difficult to satisfy Equation 4.6.

Finally, an OTA was designed to complete the peak detector module. Please refer to schematic shown in Figure 4.6. The first stage of the OTA consists of input PFETs and diode connected NFETs M_{15}, M_{17}. A gain (ratio of input to load transconductances) of 15 was desired. This ratio of transconductances can be increased by adding M_{14} and M_{16} to the circuit by decreasing the bias current of the diode-connected NFETs.

A high tail current of 92 μA was used to increase the NFET load transcontance, resulting in a very high parasitic pole frequency. Devices were sized relatively small to ensure none of parasitic poles have an impact on transfer function.

A source follower (M_7 and M_8) was used for DC level translation and defines the DC voltage on the gate of the output transistor. This helped us avoid having to use common mode feedback which makes the design simpler and uses less area. A second stage gain of 100 was desired. The overall low-frequency gain, A_0, of the OTA is 64 dB. The parasitic pole location for the second stage can be found in Equation 4.7. The schematic of the OTA and device sizes can be seen in Figure 4.6 and Table 4.1.

$$w_{p2} = \frac{g_{m8}}{C_{p2}} \tag{4.7}$$

4.3 Simulation Results

First, the OTA was simulated with the load capacitance of 1 pF. A low-freqeuncy gain of 62 dB, a GBW of 55 MHz and a phase margin of 50° was obtained. This ensures that the OTA will be stable, settle very quickly, and not suffer significantly from finite gain effects while in *read* mode. The Bode plot of the OTA is presented in Figure 4.7.

High linearity was desired for the linear branch as we discussed in nearly every chapter of this thesis. A linearity analysis was performed for the peak detector. For a "typical"

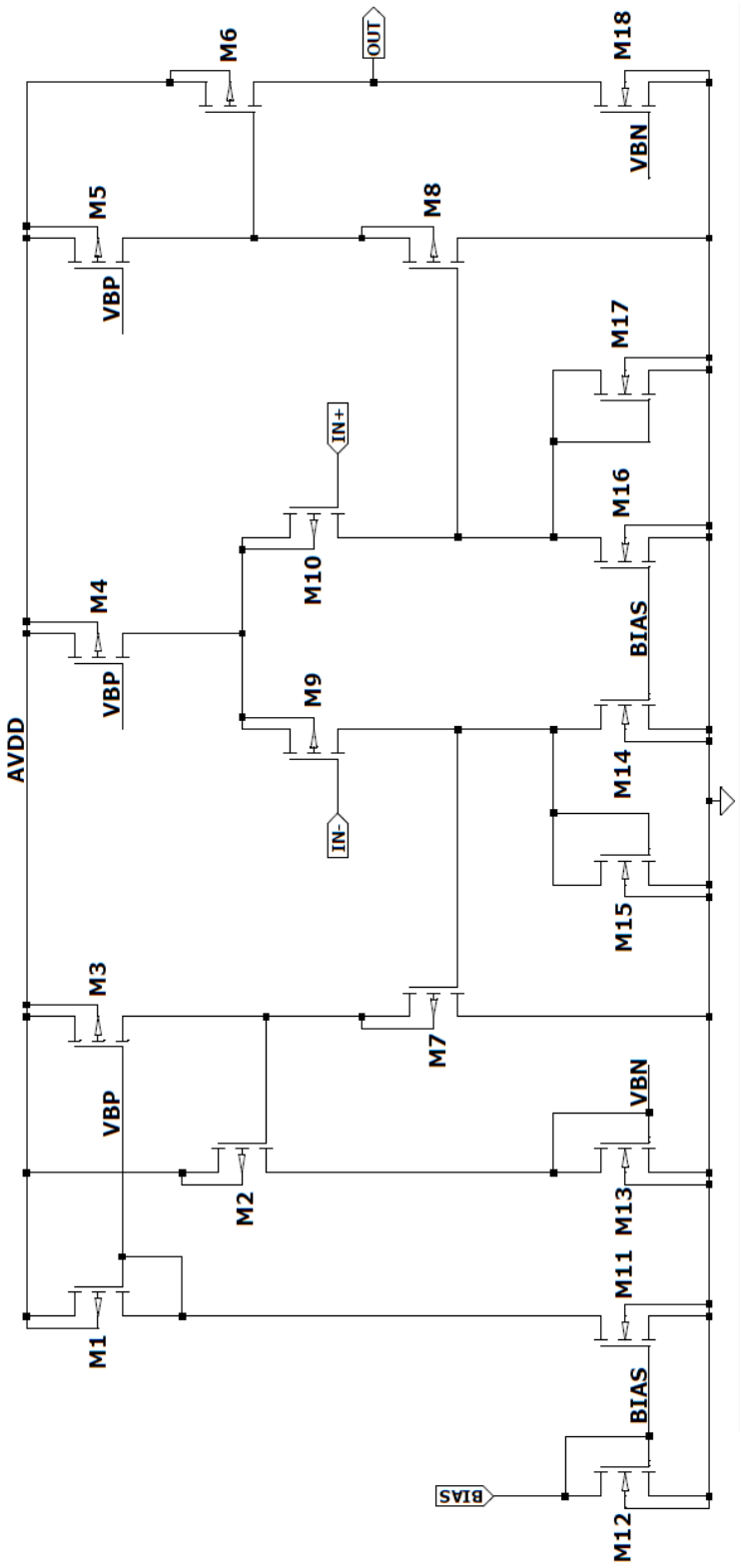

Figure 4.6: OTA Design for Negative Peak Detector

Table 4.1: Device Sizes for OTA

	W (μm)	L (μm)	Gates	I_D (μA)
M1	5	4	1	11.5
M2	8	5	1	11.5
M3	20	4	4	46
M4	40	4	8	92
M5	20	4	4	46
M6	8	5	1	11.5
M7	10	0.35	1	46
M8	10	0.35	1	46
M9	40	0.35	2	46
M10	40	0.35	2	46
M11	1.4	4	1	11.5
M12	1.4	4	1	11.5
M13	8.4	3	1	11.5
M14	4.2	4	3	34.5
M15	0.7	1	1	11.5
M16	4.2	4	3	34.5
M17	0.7	1	1	11.5
M18	8.4	3	1	11.5

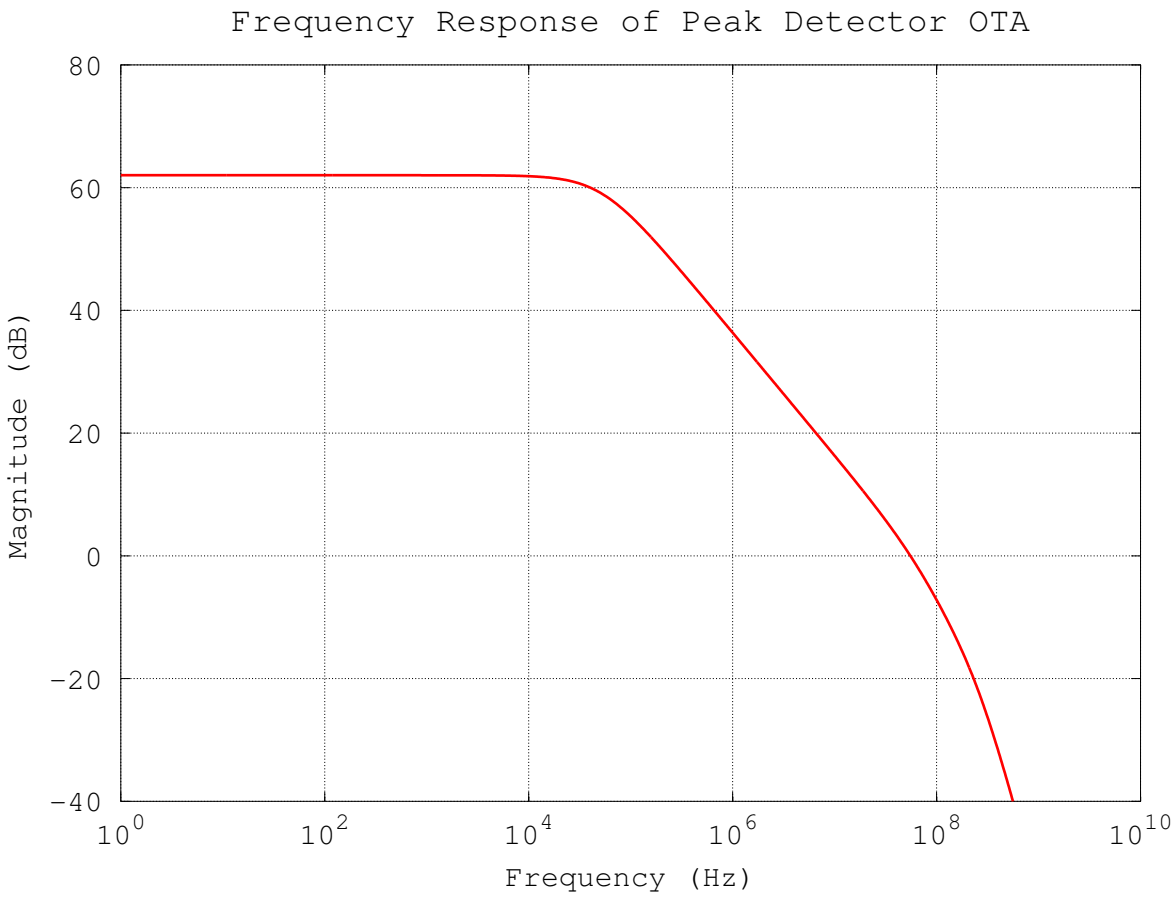

Figure 4.7: Frequency Response of OTA

process corner (no process or mismatch errors taken into account) is shown in Figures 4.8 and 4.9. One can easily see that our peak detector can detect peaks as low as 100 keV and as high as 90 MeV for the high gain mode and 360 MeV for the low gain mode with very high precision (less than 5% error). The peak detector can detect particle energies up to 100 MeV for the high gain mode and 400 MeV for the low gain mode with moderate precision ($\approx$10 % error).

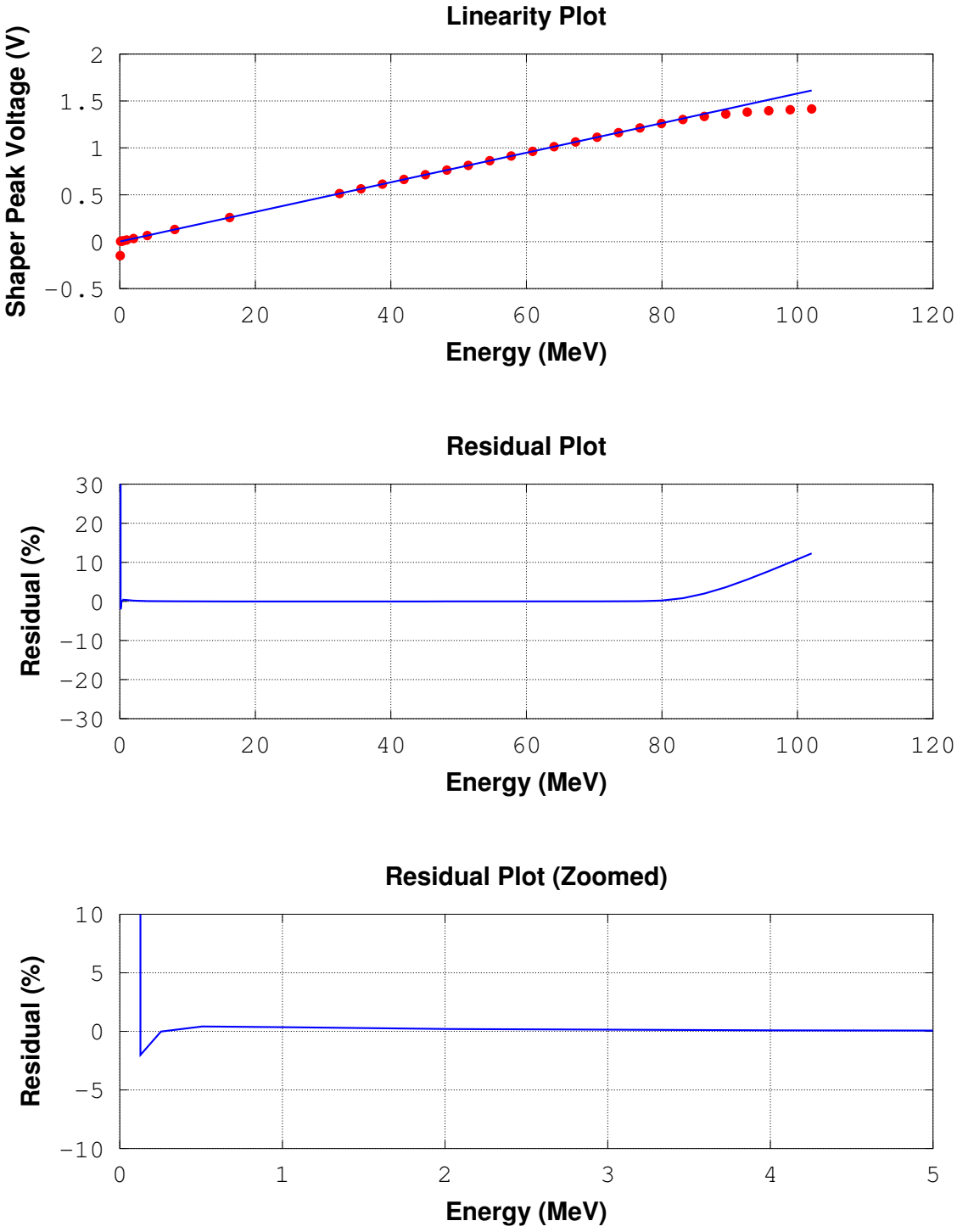

Figure 4.8: Typical Linearity Run - Negative Peak Detector - High Gain Sub-Channel

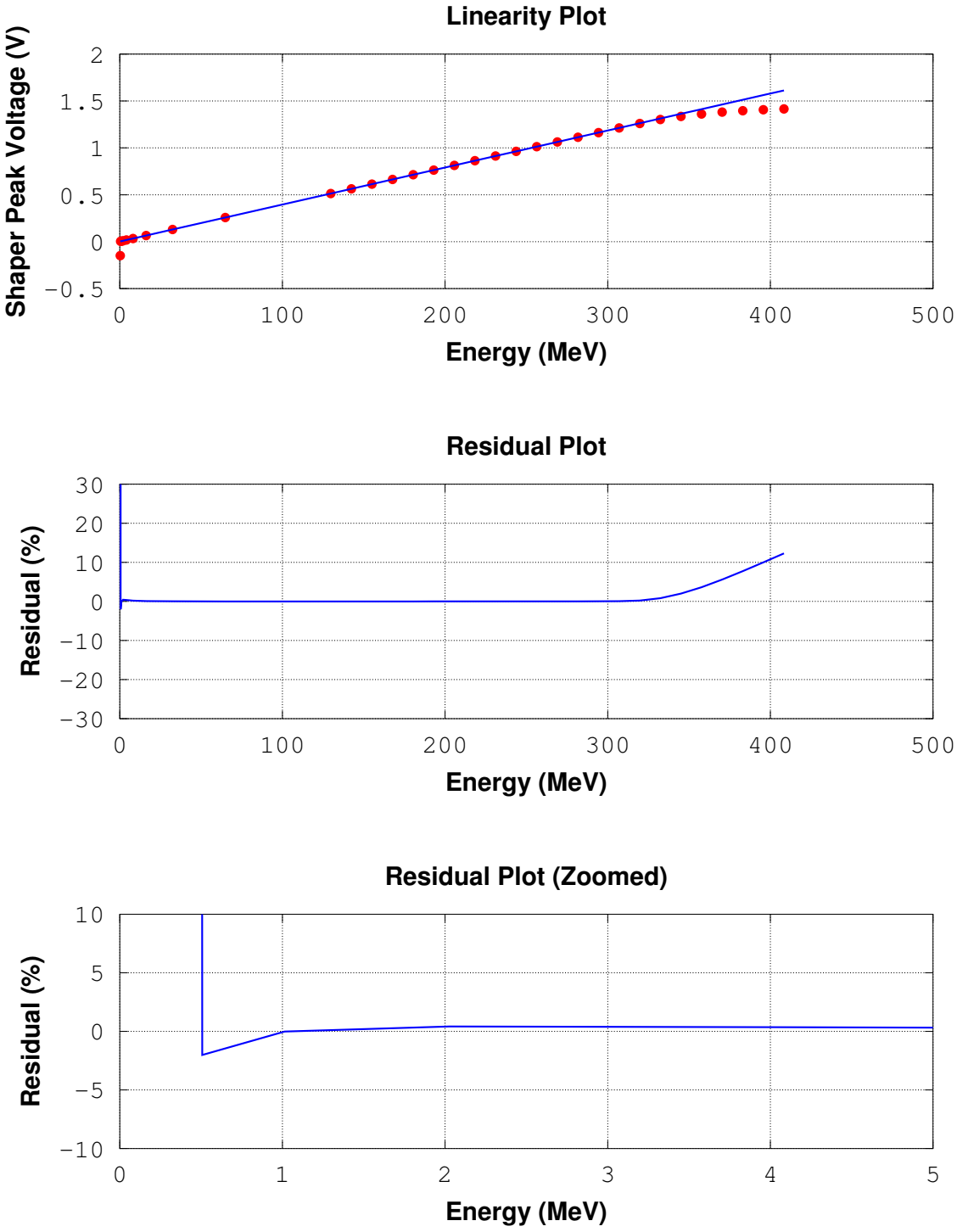

Figure 4.9: Typical Linearity Run - Negative Peak Detector - Low Gain Sub-Channel

CHAPTER 5

SUMMARY, CONCLUSIONS, AND FUTURE WORK

5.1 Summary

This thesis describes the design of the linear branch of a signal processing channel which will be part of a multi-channel integrated circuit for use in radiation monitoring. The thesis describes the design of a charge amplifier, a Gaussian filter, and a peak sampling circuit. The IC is expected to be fabricated through in Fall 2019. The IC has been named HINP5 (Heavy Ion Nuclear Physics IC - Version 5). The design presented here was implemented using a 0.35 μm AMS (Austrian Micro-Systems) CMOS process.

The charge amplifier consists of a very low-noise, high dynamic range two-stage OTA (GBW in excess of 130 MHz) and three double-poly capacitors, each shunted by a small pseudo-resistor (used for pole-zero cancellation) realized using just a few small FETs, thereby greatly reducing silicon area. The charge amplifier has dual outputs, each of which connect to the input of a Gaussian filter used for signal shaping.

The respective charge gain for the two sub-channels is x 1 (low-gain) and x 4 (high-gain). The use of dual outputs significantly relaxes the noise and dynamic range requirements of the shaper and peak sampling circuits which follow and allows us to achieve outstanding energy resolution (lower than 25 keV - FWHM) for the high-gain output while maintaining a highly linear response for energies as large as 400 MeV in the "low-gain" sub-channel. The outputs from both sub-channels is brought out of the chip differentially and then sampled by off-chip ADCs.

The peak sampler is composed of an OTA (Output Transconductance Amplifier) along with a diode-connected NFET and a sampling capacitor. The circuit makes use of correlated double sampling (CDS) to dramatically reduce the output 1/f noise and DC offset associated with the use of small transistors.

5.2 Conclusions

As we discussed at the beginning of every chapter, the linearity and the energy resolution are two most important specifications of this IC. The IC is highly linear (residuals less than ≈5%) up to 100 MeV at the output of the shapers (Figure 3.7) and linear up to 90 MeV at the output of the peak detectors (Figure 4.8). In terms of energy resolution, HINP5 is showing extremely satisfying performance and is significantly better than previous HINP designs (Figure 3.6). Energy resolution is a function of detector capacitance and the slope is excellent. The noise slope is 67 $\frac{eV}{pF}$ in high-gain mode and 20 $\frac{eV}{pF}$ in low-gain mode. An energy resolution of 18 keV (electron collection) and 20 keV (hole collection) was achieved at the output of the high-gain shaper with a detector capacitance of 100 pF. Even though the peak detector and the off-chip driver circuits will degrade this to some extent, simulations indicate that even with these additional contributions to the noise a resolution of better than 25 keV is expected.

In addition to linearity and energy resolution features, an extremely high dynamic range was obtained. The use of two shapers (x 1 and x 4) and pseudo-resistors extended the dynamic range up to 86 dB. Three new features were successfully added to linear branch: (1) utilization of external pre-amplifier (2) implementation of pseudo-resistors for both polarity (3) auto switching from *write* to *read* mode in peak detectors. The IC was simulated for the detector capacitances between 25 pF and 300 pF and correct operation demonstrated. The removal of real resistors, removal of one peak detector, change of design process from 0.5 μm to 0.35 μm reduced the silicon area compared to previous HINP versions.

5.3 Future Work

The charge amplifier and the Gaussian shaper parts of linear branch were carefully designed and evaluated. Layouts of these blocks are finished and ready to bring together

with the other branches of the IC. However, a further care needs to be taken for the peak detector. Twenty Monte Carlo simulations for the peak detector were performed. Even though spread was tight for the mismatch and process corners, Monte Carlo simulations needs to be repeated for higher number of runs, for example 40 or 60 runs. After the confirmation of a tight spread with at least 40 runs, peak detector layout needs to be done.

The AMS 0.35 μm process which is used in this design will be terminated by the manufacturer at the end of the 2019. Therefore, IC needs to be redesigned with another process if an improvement is necessary. The IC was simulated under variety of conditions (randomly distributed mismatch and process corners) and all essential circuits were added to prevent the need of any necessary future improvements.

REFERENCES

[Ball and Key, 2014] Ball, D. and Key, J. (2014). *Introductory Chemistry*. BCcampus, British Columbia.

[Carusone et al., 2011] Carusone, T., D.A., J., and K.W., M. (2011). *Analog Integrated Circuit Design*. John Wiley and Sons Ltd., Hoboken, New Jersey.

[Charity et al., 2007] Charity, R. J., Mercurio, K., Sobotka, L. G., Elson, J. M., Famiano, M., Banu, A., Fu, C., Trache, L., and Tribble, R. E. (2007). Decay of ^{10}C excited states above the $2p + 2\alpha$ threshold and the contribution from "democratic" two-proton emission. *Phys. Rev. C*, 75:051304.

[De Geronimo et al., 2008] De Geronimo, G., Fried, J., Frost, E., Phlips, B. F., Vernon, E., and Wulf, E. A. (2008). Front-end asic for a silicon compton telescope. *IEEE Transactions on Nuclear Science*, 55(4):2323–2328.

[De Geronimo and Li, 2011] De Geronimo, G. and Li, S. (2011). Shaper design in cmos for high dynamic range. *IEEE Transactions on Nuclear Science*, 58(5):2382–2390.

[De Geronimo and O'Connor, 2000] De Geronimo, G. and O'Connor, P. (2000). A cmos fully compensated continuous reset system. *IEEE Transactions on Nuclear Science*, 47(4):1458–1462.

[De Geronimo and O'Connor, 2005] De Geronimo, G. and O'Connor, P. (2005). Mosfet optimization in deep submicron technology for charge amplifiers. *IEEE Transactions on Nuclear Science*, 52(6):3223–3232.

[De Geronimo et al., 2000] De Geronimo, G., O'Connor, P., and Grosholz, J. (2000). A generation of cmos readout asics for czt detectors. *IEEE Transactions on Nuclear Science*, 47(6):1857–1867.

[De Geronimo et al., 2002a] De Geronimo, G., O'Connor, P., and Kandasamy, A. (2002a). Analog cmos peak detect and hold circuits. part 1. analysis of the classical configuration. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 484(1):533 – 543.

[De Geronimo et al., 2002b] De Geronimo, G., O'Connor, P., and Kandasamy, A. (2002b). Analog cmos peak detect and hold circuits. part 2. the two-phase offset-free and derandomizing configuration. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 484(1):544 – 556.

[Engel et al., 2007] Engel, G. L., Sadavisam, M., Nethi, M., Elson, J. M., Sabotka, L. G., and Charity, R. J. (2007). A multi-channel integrated circuit for use in low- and intermediate-energy nuclear physics—hinp16c. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 573(3):418 – 426.

[Ghosh, 2015] Ghosh, P. (2015). Characterization of silicon micro-strip sensors with a pulsed infra-red laser system for the CBM experiment at FAIR. *Journal of Instrumentation*, 10:C03029.

[Grybos et al., 2007] Grybos, P., Maj, P., and Szczygiel, R. (2007). Comparison of two pole-zero cancellation circuits for fast charge sensitive amplifier in cmos technology. In *2007 14th International Conference on Mixed Design of Integrated Circuits and Systems*, pages 243–246.

[Grybos and Szczygiel, 2008] Grybos, P. and Szczygiel, R. (2008). Pole-zero cancellation circuit with pulse pile-up tracking system for low noise charge-sensitive amplifiers. *IEEE Transactions on Nuclear Science*, 55(1):583–590.

[Knoll, 1989] Knoll, G. F. (1989). *Radiation Detection and Measurement*. Wiley, New York.

[Sadasivam, 2002] Sadasivam, M. (2002). A multi-channel integrated circuit for use with silicon strip detectors in experiments in low and intermediate physics. Master's thesis, Southern Illinois University Edwardsville.

[Sadrozinski, 2001] Sadrozinski, H. F. (2001). Applications of silicon detectors. *IEEE Transactions on Nuclear Science*, 48(4):933–940.

[Siegbahn, 1965] Siegbahn, K. (1965). *Alpha- beta- and gamma-ray spectroscopy*. North-Holland Pub. Co., Amsterdam.

[Spieler, 2005] Spieler, H. (2005). *Semiconductor Detector Systems*. Oxford University Press, New York.

[Wallace et al., 2007] Wallace, M., Famiano, M., van Goethem, M., Rogers, A., Lynch, W., Clifford, J., Delaunay, F., Lee, J., Labostov, S., Mocko, M., Morris, L., Moroni, A., Nett, B., Oostdyk, D., Krishnasamy, R., Tsang, M., de Souza, R., Hudan, S., Sobotka, L., Charity, R., Elson, J., and Engel, G. (2007). The high resolution array (hira) for rare isotope beam experiments. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 583(2):302 – 312.

APPENDICES

APPENDIX A

Verilog-A Models

A.1 Silicon Strip Detector

```
// VerilogA for HINP_csa, Silicon_Strip_Detector_Linearity, veriloga
`include "constants.vams"
`include "disciplines.vams"
`define  QE  1.602e-19
module Silicon_Strip_Detector_Linearity_new2(LG_peak_in, HG_peak_in, outp, LG_sample_in,
     HG_sample_in);
      input    LG_peak_in;
      input    HG_peak_in;
      input    LG_sample_in;
      input    HG_sample_in;
      electrical  LG_peak_in, HG_peak_in, LG_sample_in, HG_sample_in;
      output      outp;
      electrical  outp;
      electrical  gnd;
      ground      gnd;
      electrical  bias_src;  // Voltage Source Node
      electrical  outp1;  //  Node before Blocking Cap
      parameter real C_det = 75p from [10p:500p]; // Detector Energy Range
      parameter real R_bias = 1M from [1k:100M]; // Bias Resistor
      parameter real V_bias = 50 from [10:500]; // Bias Voltage
      parameter real Is = 100n   from [1n:1u]; // Leakage Current
      parameter real PW = 15n    from [1n:50n]; // Current Pulse Width
      parameter real period = 1m from [100u:100m]; // Current Pulse Period
      parameter real time_tol = 10p; // Time tolerance for the timer
      parameter real trf = 50p; // Rise/Fall Time for the Current Pulse
      parameter real tpd = 100u from (0:200]; // Delay
      parameter real tpd_sample = 60u from (0:200]; // Start recording baseline sample
      parameter real sample_record = 10u from (0:200]; // Stop recording baseline sample
           after 10u
      parameter real tpd_record = 1.25m; // Delay for data record / 500u
      parameter real tpd_energy_change = 600u; // Delay for energy change
      parameter real C_block = 1u from [1u:100u]; // Blocking Capacitor
      parameter real Polarity = 1 from [-1:1]; // 1 for Holes, -1 for Electrons
      integer fid;
      integer n, k;
      real I_amp, charge_packet, I_det, time_flag, Energy, LG_in, HG_in, LG_sample,
          HG_sample;
      real EL[101:0];
      analog begin
         @(initial_step) begin
            // First create and open the file to record the data
            if(Polarity < 0)begin
               fid = $fopen("~/cds/results/data_recorder_electrons_%P.dat", "a");
               $fstrobe(fid, "Peak Shaper Output as a Function of Particle Energy");
            end
            else begin
               fid = $fopen("~/cds/results/data_recorder_holes_%P.dat", "a");
               $fstrobe(fid, "Peak Shaper Output as a Function of Particle Energy");
            end
```

```
    $fstrobe(fid, "Energy\tLG\tHG"); // Column Names
    I_det = 0.0; // Initial detector current amplitude
    time_flag = 0; // Time flag default value
    n = 0; // Start the counter from 0 to increase energy levels
    EL[0] = 10k;
    EL[1] = 10k;      EL[2] = 20k;      EL[3] = 50k;      EL[4] = 100k;     EL[5] =
        200k;     EL[6] = 500k;
    EL[7] = 1M;       EL[8] = 2M;       EL[9] = 5M;       EL[10] = 10M;     EL[11] =
         20M;     EL[12] = 50M;
    for (k = 12; k <= 61; k = k + 1) begin
          EL[k+1] = EL[k] + 2M;
    end
    EL[63] = 200M;    EL[64] = 250M;      EL[65] = 300M;
    for (k = 65; k <= 99; k = k + 1) begin
          EL[k+1] = EL[k] + 6M;
    end
    Energy = EL[0] * Polarity;
end
charge_packet = `QE * (Energy / 3.6); // Energy required to form a charge pair
    for Si
I_amp = charge_packet / PW; // Amplitude of the Current Pulse
// Gaussian shapes are read to obtain baseline accurately
@(timer(tpd_sample, period, time_tol)) begin
    LG_sample = V(LG_sample_in);
    HG_sample = V(HG_sample_in);
end
@(timer((tpd_sample + sample_record), period, time_tol)) begin
    LG_sample = LG_sample;
    HG_sample = HG_sample;
end
// Turn Current ON (Onset of Radiation)
@(timer(tpd, period, time_tol)) begin
    I_det = I_amp;
    time_flag = 1;     // Set time flag to specify bound_step time boundaries
end
// Turn Current OFF (Charge Packet has been deposited)
@(timer((tpd + PW), period, time_tol)) begin
    I_det = 0.0;
end
// Record the data (Energy level, LG peak, HG peak)
if(n > 1) begin // Ignore the first data bacuse it's unwanted due to Shaper
    startup
      @(timer(tpd_record, period, time_tol)) begin
         LG_in = V(LG_peak_in);
         HG_in = V(HG_peak_in);
         // We want Electrons and Holes plots look to be same
         $fstrobe(fid, "%g\t%.6f\t%.6f\t%.6f\t%.6f", abs(Energy/1e6) , abs(
             LG_in - LG_sample), abs(HG_in - HG_sample), LG_sample, HG_sample);
              // Divide Energy by 1e6 to get results as MeV, change 1.65 with
             AGND
      end
end
// Set step size(bound_step) back to default
@(timer((tpd + (500 * PW)), period, time_tol)) begin
    time_flag = 0;
end
// Increase and Calculate the energy level for the next measurement (10keV, 20
    keV, 50keV, 100keV, 200keV, 500keV...)
@(timer(tpd_energy_change, period, time_tol)) begin
      n = n + 1;
      Energy = EL[n] * Polarity;
end
// Model Silicon Strip Detector
```

```
        I(gnd,outp1) <+ transition(I_det, 0.0, trf, trf); // Radiation Induced Current
            Pulse
        I(gnd,outp1) <+ white_noise(2 * `QE * Is, "Shot Noise"); // Model of the Shot
            Noise of the Detector
        I(outp1) <+ C_det * ddt(V(outp1)); // Model for Detector Capacitance
        I(gnd,outp1) <+ Is * (limexp(V(gnd,outp1) / $vt) - 1.0); // Model Detector as
            Diode
        V(bias_src) <+ V_bias; // Bias Voltage Source Model
        V(bias_src,outp1) <+ I(bias_src,outp1) * R_bias; // Bias Resistor Model
        V(bias_src,outp1) <+ white_noise(4 * $vt * `QE * R_bias, "Johnson_noise"); //
            Thermal Noise
        I(outp1,outp) <+ C_block * ddt(V(outp1,outp)); // Blocking Capacitor
        // Change step size to precisely detect current pulse
        if(time_flag)begin
              $bound_step(PW / 10);
        end
        // Close the recorded data file
        @(final_step) begin
           $fclose(fid);
        end
      end
endmodule
```

A.2 Pulser

```
// VerilogA for caLib, Pulser_Generator, veriloga
`include "constants.vams"
`include "disciplines.vams"
module Pulser_Generator(HOLES, LG_peak_in, HG_peak_in, LG_sample_in, HG_sample_in, outp)
    ;
   input    HOLES, LG_peak_in, HG_peak_in, LG_sample_in, HG_sample_in; // Here for data
       recording purposes
   output      outp;
   electrical  LG_peak_in, HG_peak_in, LG_sample_in, HG_sample_in, HOLES, outp;
   parameter   period = 3m; // Pulse Period
   parameter   tpd = 100u; // Delay
   parameter   time_tol = 10p; // Time Tolerance
   parameter   tau_r = 5n; // Rise Time Constant
   parameter   tau_f = 0.3m; // Fall Time Constant
   parameter   tpd_record = 3.25m; // Start Recording Data After
   parameter   tpd_sample = 60u; // Sample Delay
   parameter   sample_record = 10u; // Sample Record After
   real     time_offset, vout, polarity, charge_packet, delta_V, time_flag, LG_in, HG_in
       , LG_sample, HG_sample;
   real     EL[65:0];
   integer  n,k,fid;
   analog begin
      @(initial_step) begin
         n = 0;
         time_flag = 0;
         vout = 0;
         polarity = V(HOLES);
            EL[0] = 0.0;
         for (k = 0; k <= 63; k = k + 1) begin
               EL[k+1] = EL[k] + 50m;
         end
         // First create and open the file to record the data
         if(polarity < 1.65)begin
            fid = $fopen("~/cds/results/pulser/data_recorder_electrons_%P.dat", "a");
            $fstrobe(fid, "Peak Shaper Output as a Function of Pulse Amplitude in Volts"
                );
```

```
            end
            else begin
               fid = $fopen("~/cds/results/pulser/data_recorder_holes_%P.dat", "a");
               $fstrobe(fid, "Peak Shaper Output as a Function of Pulse Amplitude in Volts"
                   );
            end
               $fstrobe(fid, "Voltage(V)\tLG\tHG"); // Column Names
         end
         delta_V = EL[n]; // Voltage pulse amplitude
         // Next pulse amplitude
         @(timer(tpd, period, time_tol)) begin
            n = n + 1;
         end
         // Mark the offset time
         @(timer(tpd, period, time_tol)) begin
            time_offset = $abstime;
         end
         // Gaussian shapes are read to obtain baseline accurately
         @(timer(tpd_sample, period, time_tol)) begin
               LG_sample = V(LG_sample_in);
               HG_sample = V(HG_sample_in);
         end
         @(timer((tpd_sample + sample_record), period, time_tol)) begin
               LG_sample = LG_sample;
               HG_sample = HG_sample;
         end
         if(n > 1) begin // Ignore the first data bacuse it's unwanted due to Shaper
             startup
                  @(timer(tpd_record, period, time_tol)) begin
                     LG_in = V(LG_peak_in);
                     HG_in = V(HG_peak_in);
                     // We want Electrons and Holes plots look to be same
                     $fstrobe(fid, "%g\t%.6f\t%.6f\t%.6f\t%.6f", abs(delta_V) , abs(LG_in -
                          LG_sample), abs(HG_in - HG_sample), LG_sample, HG_sample);
                  end
            end
         // Set the time flags to arrange bound_step
         @(timer((tpd-(tpd/1000)), period, time_tol)) begin
            time_flag = 1;
         end
         @(timer((tpd+(tpd/10)), period, time_tol)) begin
            time_flag = 0;
         end
         // Exponential pulse equations
         if(polarity > 1.65) begin
            vout = -(delta_V) * (exp(-($abstime-time_offset)/(tau_r)) - exp(-($abstime-
                time_offset)/(tau_f)));
         end
         else begin
            vout = 3.3 - (-(delta_V) * (exp(-($abstime-time_offset)/(tau_r)) - exp(-(
                $abstime-time_offset)/(tau_f))));
         end
         V(outp) <+ vout;
         // Set time step
         if(time_flag)begin
            $bound_step(2n);
         end
         // Close the file
         @(final_step) begin
            $fclose(fid);
         end
      end
endmodule
```

A.3 Ideal Peak Detector

```
// VerilogA for HINP_csa, Pos_Peak_Detector, veriloga
`include "constants.vams"
`include "disciplines.vams"
module Pos_Peak_Detector(IN, IB_OP_WB, IB_OTA, TRACK, READ, RESET, HOLES, AGND, IB_RST,
    AVDD, AVSS, OUT);
      // Needed to unify inputs and outputs of the transistor level model and veriloga
          model
      inout       IN, IB_OP_WB, IB_OTA, TRACK, READ, RESET, HOLES, AGND, IB_RST, AVDD,
          AVSS, OUT;
      electrical     IN, IB_OP_WB, IB_OTA, TRACK, READ, RESET, HOLES, AGND, IB_RST, AVDD
          , AVSS, OUT;
      real     vout;
      real  Vth;
      analog begin
            Vth = (V(AVDD) + V(AVSS)) / 2.0; // Set threshold
            @(initial_step) begin
                  vout = 1.0; // Start at 1V
            end
            if (V(RESET) > Vth) begin
                  vout =  1.0; // Reset to 1V
            end
            else if (V(TRACK) > Vth) begin // In Track Phase
                     if (V(IN) > vout) begin // Keep tracking
                           vout = V(IN);
                     end
                     else begin
                           vout = vout; // Stop tracking
                     end
                end
                else begin
                     vout = vout; // Out of Track Phase
                end
      V(OUT) <+ vout;
      end
endmodule
```

A.4 Ideal Gaussian Shape Generator

```
// VerilogA for peakLib, Gaussian_Shape_Generator, veriloga
`include "constants.vams"
`include "disciplines.vams"
module Gaussian_Shape_Generator(outp);
      output      outp;
      electrical  outp;
      parameter real tpd = 100u from (0:200]; // Delay
      parameter real period = 1m from [100u:100m];
      parameter real time_tol = 10p; // Time tolerance
      parameter real sigma = 0.45u; // Sigma for Gaussian
      parameter real BS = 15n; // Bound step
      parameter real tpd_bs = 90u; // Bound step start
      parameter real tpd_bf = 110u; // Bound step stop
      real     A[101:0];
      real     vout;
      real     offset;
      real     t0;
      real     time_flag;
      integer  n,k;
      analog begin
         @(initial_step) begin
```

```
            n = 0;
            A[0] = 0.0;
            // Increase amplitude by 0.02 Volts
            for (k = 0; k <= 100; k = k +1) begin
                  A[k+1] = A[k] + 0.02;
            end
            offset = 1.65;  // Baseline
            time_flag = 0;
         end
         // Next Gaussian shape amplitude
         @(timer(tpd, period, time_tol)) begin
            n = n + 1;
            t0 = $abstime + 1.5u;
         end
         // Set the time flags to arrange bound_step
         @(timer(tpd_bs, period, time_tol)) begin
            time_flag = 1;
         end
         @(timer(tpd_bf, period, time_tol)) begin
            time_flag = 0;
         end
         // Gaussian Shape equation
         vout = A[n] * exp(-pow(($abstime - t0), 2.0) / (2.0 * sigma * sigma)) + offset;
         V(outp) <+ vout;
         // Set time step
         if(time_flag)begin
               $bound_step(BS / 10);
         end
      end
endmodule
```

APPENDICES

APPENDIX B

Octave Scripts

B.1 Linearity Plot

```
#!/usr/bin/octave -qf

# MATLAB routine to plot peak voltage as function of energy

# Get name of data file

arg_list = argv () ;
rootname = arg_list{1} ;

# Get number of points to use in fit

m = str2num(arg_list{2}) ;

# Electrons or Holes, E or H

Polarity = arg_list{3};

#Low Gain or High Gain, type H or L

Gain_type = arg_list{4};

# Load in the data from file
# Use first line as plot title
# Get rid of \n at the end of the line

fid = fopen([rootname  '.dat'], 'rt') ;
tline = fgets(fid) ;
tline = tline(1:end-1) ;

# Second line has a time stamp so
# Start reading data from the 5th and 7th lines

if (Gain_type == 'H')
   data = dlmread([rootname '.dat'], '\t', 4, 0) ;
   x = data(:,1) ;
   y = data(:,3) ;
else
   data = dlmread([rootname '.dat'], '\t', 6, 0) ;
   x = data(:,1) ;
   y = data(:,2) ;
end

#  x-data in column 1 and y-data in column 2 or 3

n = length(x) ;

# Use the first m points to do the line fit (differs for HG or LG due to offset)

xfit = x(3:(m+2)) ;
```

```
yfit = y(3:(m+2)) ;

# Asumme x-data lines on a line whose slope is c2 and intercept is c1

# Create y = c1 + c2 * x
# Y = c * X

X = [ones(m, 1) xfit] ;

# Calculate coefficient vector (slope and intercept)

c = (pinv(X'*X))*X'*yfit ;
intercept = c(1)
slope = c(2)

# Plot the fitted equation we got from the regression
# X should now be all of the data

X = [ones(n, 1) x] ;

h = figure('name','Linearity Plot','numbertitle','off') ;

# Plot the original data

subplot(2,1,1) ;
plot(x, y, 'r.','MarkerSize',15);
if (Polarity == 'E')
   if (Gain_type == 'H')
   axis([0 150 0 3]) ;
   else
   axis([0 500 0 3]) ;
   end
else
   if (Gain_type == 'H')
   axis([0 150 0 3]) ;
   else
   axis([0 500 0 3]) ;
   end
end
grid on

xlabel('Energy (MeV)');
ylabel('Shaper Peak Voltage (Volts)');

hold on ;

# Plot the best fit line on the same plot!

plot(X(:,2), X*c, '-', "linewidth", 4) ;
title(tline) ;

% Compute the residuals

res =  (X*c) - y ;

# Convert the residual voltage to an energy

res = res ./ slope ;

# Convert the residual energy to a percentage based on energy level

res = (res ./ x) ;
```

```
# Plot the residuals

subplot(2,1,2) ;
plot(X(:,2), res*100, '-', "linewidth", 4) ;
if (Gain_type == 'H')
   axis([0 150 -15 +15]) ;
else
   axis([0 500 -10 +10]) ;
end
grid on

title('Residual Plot') ; % Set the Title
xlabel('Energy (MeV)'); % Set the x-axis label
ylabel('Residual (%)'); % Set the y-axis label

# Create a time_stamp

timestamp = strftime("_%Y-%m-%d_%H:%M", localtime( time() ) ) ;

warning("off")
print(h,'-dpdf','-color', [ './pdf/' rootname "_" Gain_type timestamp '.pdf']) ;

hold off
exit
```

B.2 Noise Plot

```
#!/usr/bin/octave -qf

# MATLAB routine to plot noise as function of Detector Capacitance and Comparison

# Get name of data files to plot

arg_list = argv () ;
rootname1 = arg_list{1} ;
rootname2 = arg_list{2} ;

# Load in the data from files

fid1 = fopen([rootname1  '.dat'], 'rt') ;
fid2 = fopen([rootname2  '.dat'], 'rt') ;

# First line has a description so start from 2nd line

data1 = dlmread([rootname1 '.dat'], '\t', 1, 0) ;
data1 = dlmread([rootname2 '.dat'], '\t', 1, 0) ;

#  x-data in column 1 and y-data in column 2

x1 = data1(:,1) ; # Cap Value
y1 = data1(:,2) ; # Resolution
n1 = length(x1) ;

x2 = data2(:,1) ; # Cap Value
y2 = data2(:,2) ; # Resolution
n2 = length(x2) ;

plot(x1, y1, 'r.', 'linewidth', 3);
grid on
xlabel('Cap Value (pF)'); %Multiply x with 10e12
ylabel('Resolution (keV)');
```

```
hold on ;

plot(x2, y2, 'b.', 'linewidth', 3);
title('Noise Performance Comparison Between Two Different Configuration') ;
legend({'One polarity peak detection','Two polarity peak detection'},'Location','
    northeast')

timestamp = strftime("_%Y-%m-%d_%H:%M", localtime( time() ) ) ;
warning("off")
print(h,'-dpdf','-color', [ './pdf/' rootname2 "_" Gain_type timestamp '.pdf']) ;

hold off
exit
```

APPENDICES

APPENDIX C

TCL Monte Carlo Run Split Script

```
#!/usr/bin/env tclsh

# Provide the arguments

set filename   [lindex $argv 0]
set num_points [lindex $argv 1]

# Find if it is electron or hole detection

if {[regexp "electron" $filename] == 1 } {
  set  polarity "E"
} else {
   if {[regexp "holes" $filename] == 1 } {
      set  polarity "H"
   } else {
      puts "You did something wrong"
      exit
   }
}

# Open the file and split each run

set fid [open "${filename}.dat" r]
set count 0
while { [gets $fid line] >= 0 } {
   if {[regexp "^Peak" $line] == 1} {
      if { $count == 0} {
         set count [expr {$count + 1}]
         set fidw [open "${filename}_${count}.dat" w]
         puts $fidw $line
      } else {
         close $fidw
         set count [expr {$count+1}]
         set fidw [open "${filename}_${count}.dat" w]
         puts $fidw $line
      }
   } else {
      puts $fidw $line
   }
}

close $fidw
close $fid

# Create another file to run linearity script for each MC simulation

if {[file exists "./run_linearity"] == 1} {
   file delete "./run_linearity"
}
set  fidA [open "run_linearity" w]
set  Entry1 "#!/bin/csh"
set  Entry2 "cd ~/cds/results"
puts $fidA $Entry1
```

```
puts $fidA $Entry2
for {set i 1} {$i <= $count} { incr i } {
   puts  $fidA "linearity ${filename}_${i} $num_points $polarity H"
   puts  $fidA "linearity ${filename}_${i} $num_points $polarity L"
}
close $fidA

set  cmd  "chmod u+x ./run_linearity"
eval exec $cmd
```

APPENDICES

APPENDIX D

Ocean Script - Energy Resolution (Electron Collection - High Gain output)

```
; Name of the testbench
;
name = "Noise_for_ocean_tb"
;
; Simulation temperature
;
temperature = 27
;
; Get the value of the PHOME variable
;
phome = getShellEnvVar("PHOME")

;
; Select spectre as our simulator
;
simulator( 'spectre )
;
; Point to the netlist for the design to be simulated
;

designVar = sprintf(nil "%s/Sim/%s/spectre/schematic/netlist/netlist" phome name)
design(designVar)

;
; Point to where results are located
;
resultsVar = sprintf(nil "%s/Sim/%s/spectre/schematic" phome name)
resultsDir(resultsVar)

;
; Tell simulator where the model files are located
;

modelFile(
    '("$AMS_DIR/spectre/s35/soac/processOption.scs" "")
    '("$AMS_DIR/spectre/s35/soac/cmos53.scs" "cmostm")
    '("$AMS_DIR/spectre/s35/soac/res.scs" "restm")
    '("$AMS_DIR/spectre/s35/soac/cap.scs" "captm")
    '("$AMS_DIR/spectre/s35/soac/vbic.scs" "biptm")
    '("$AMS_DIR/spectre/s35/soac/ind.scs" "indtm")
    '("$AMS_DIR/spectre/s35/soac/esddiode.scs" "esddiodetm")
)
definitionFile(
    "$AMS_DIRspectre/s35/soac/soac.scs"
)

; ######################################################
; Script somewhat unique after this point
; ######################################################

filename = sprintf(nil "%s/ocean/noise_electrons_hg/results.dat" phome)
fid = outfile(filename "w")
fprintf(fid "Cap\t Resolution(keV)\n")
```

```
drain(fid)

;  Resolution depends on capacitor value
;  Vary capacitor value

capList = list(25p 35p 50p 75p 100p 125p 150p 175p 200p 225p 250p 275p 300p )

; Supply Voltage

desVar( "AVDD" 3.3 )

; Polarity ( 0 for Electrons 3.3 for Holes)

desVar( "HOLES" 0 )

; Leakage Current

desVar( "Is" 100n )

; Particle Energy Level (Negative values for Electrons, Positive Values for Holes)

desVar( "Energy" -10M )

;
; Perform a series of simulations
;

foreach(capVal capList
    analysis('noise ?start "1m"  ?stop "1G"  ?dec "10"  ?p "/HG"  ?n "/gnd!"  ?oprobe ""
          ?iprobe ""  )
    desVar("C_det" capVal)
    envOption('analysisOrder  list("noise"))
    saveOption( ?outputParamInfo t )
    saveOption( ?elementInfo t )
    saveOption( ?modelParamInfo t )
    temp( temperature )
    run()
    sigma = rmsNoise( 1m 5M )
        ;Use this if you want high gain mode
        Resolution = 140972*sigma;

        ;Use this if you want low gain mode
   ;Resolution = 564904*sigma;
    fprintf(fid, "%e\t%f\n",  capVal, Resolution)
    drain(fid)
)

;
; Close up the file ... we are done
;

drain(fid)
close(fid)
```