MRI (# 1625499) : Design of Configuration and Readout Electronics for a Multi-Channel Integrated Circuit used in the Detection and Monitoring of Ionization Radiation

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Outline

- Introduction
- System Level Design
- Digital Design using EDI Tools
- Standard Cell Design Flow
- Common Channel
- Signal Channel
- Summary
- Future Work

Introduction

- ***Research Background:***
  - Alliance of IC Design Research Laboratory at SIUE with the Nuclear Reactions Group at Washington University St. Louis
  - Development of a class of multi-channel custom integrated circuits (ICs)
  - Need for these custom IC's ?
  - The Collaboration Achievements:
    - **HINP** – Heavy Ion Nuclear Physics with 16 Channels
    - **PSD** – Pulse Shape Discrimination with 8 Channels
    - Later many revised versions of PSD8C and HINP16C are developed

- HiRA – High Resolution Array Detector
  - An Array of Silicon Strip Detectors
  - 2 Silicon detectors of 65 µm & 1.5 mm

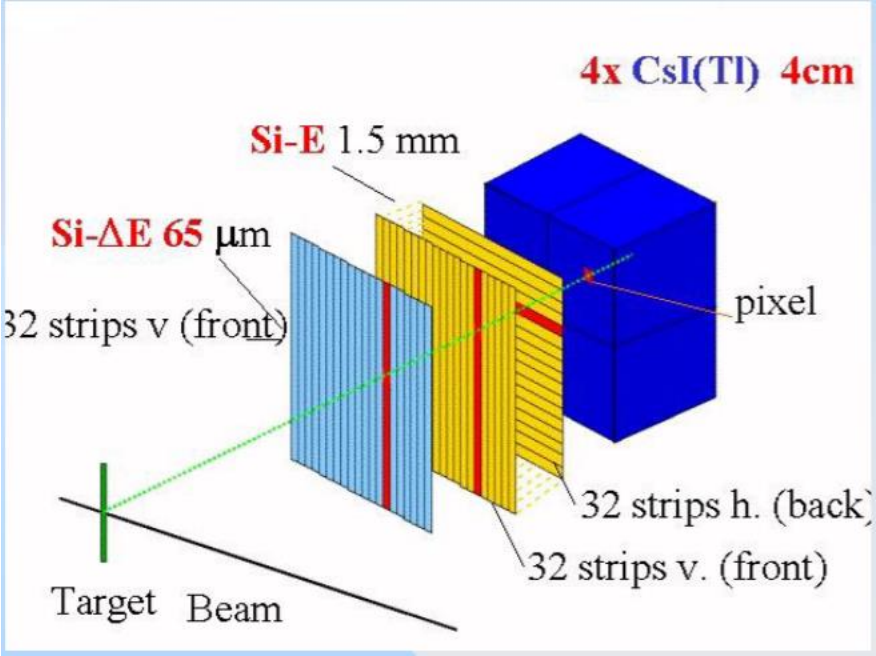


Fig.2 A look at Silicon Strip Detectors in HiRA © Stephanie_Simpson

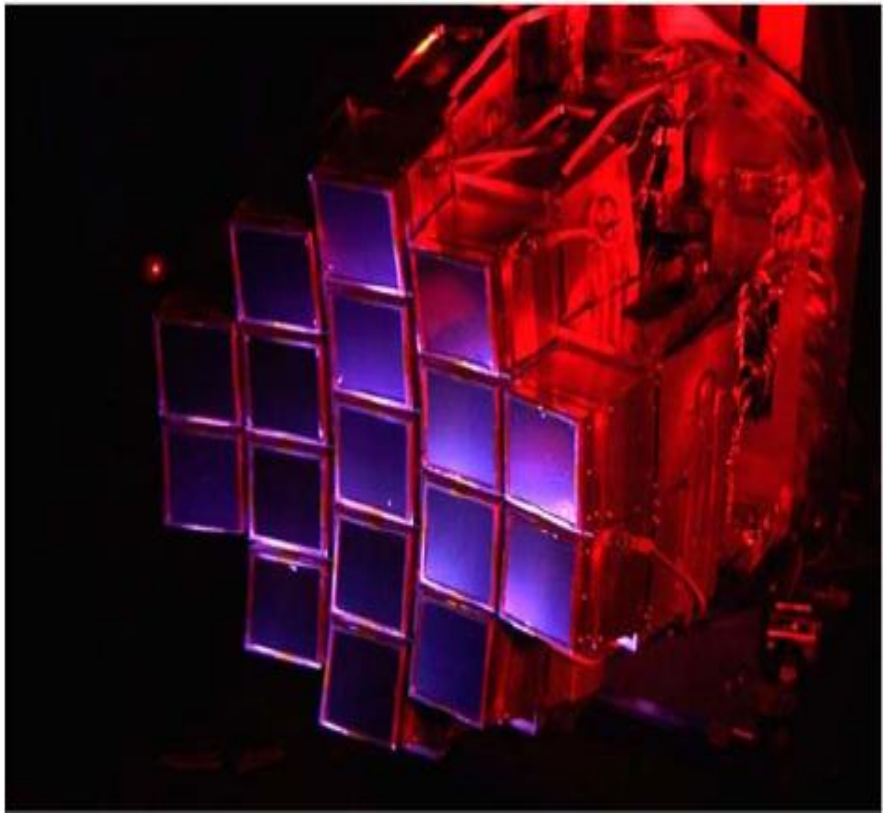


Fig.1 HiRA – High Resolution Array Detector

HINP5

- Linear Circuits
- Timing Circuits
- Configuration and Readout Circuits

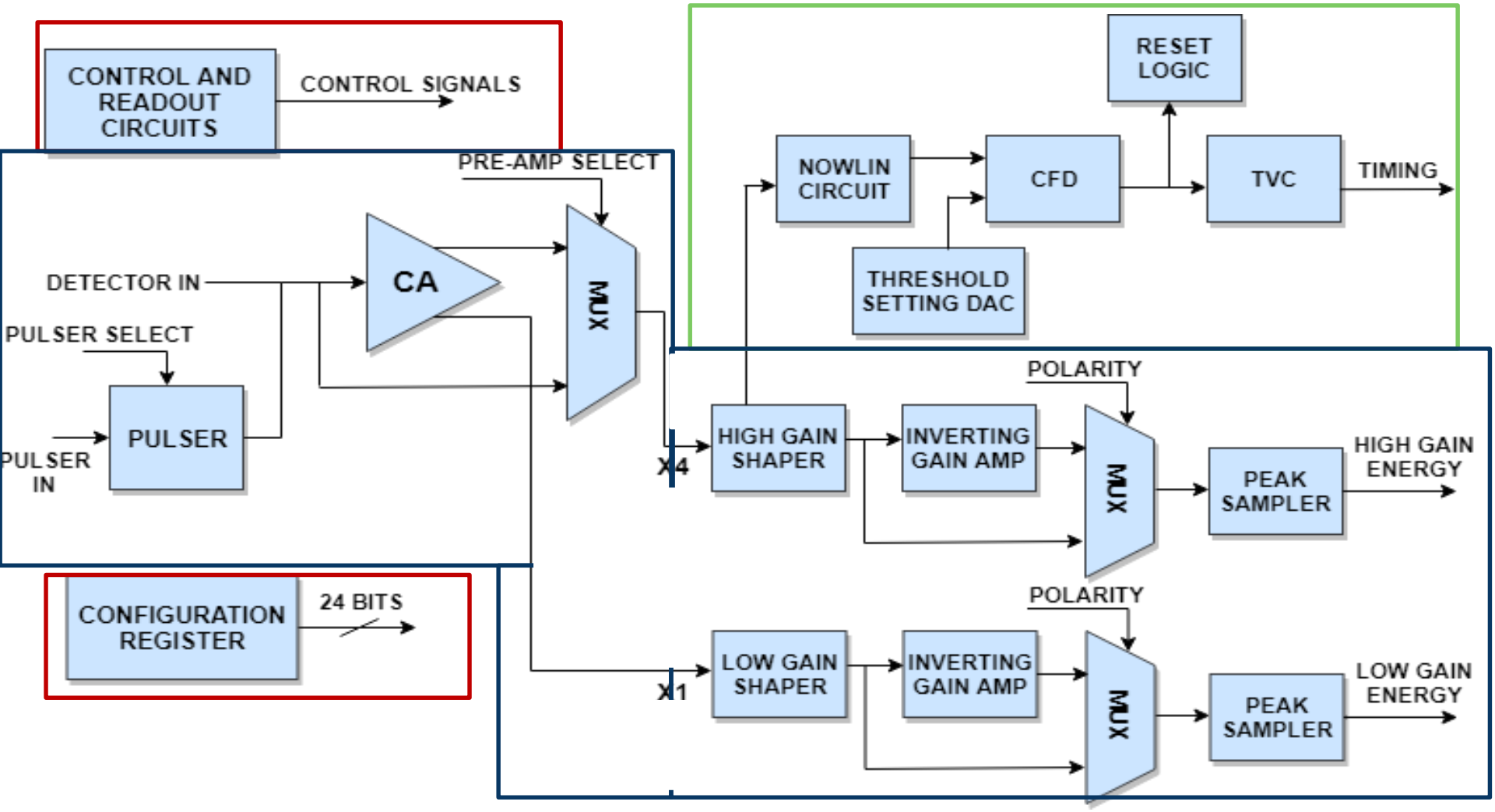
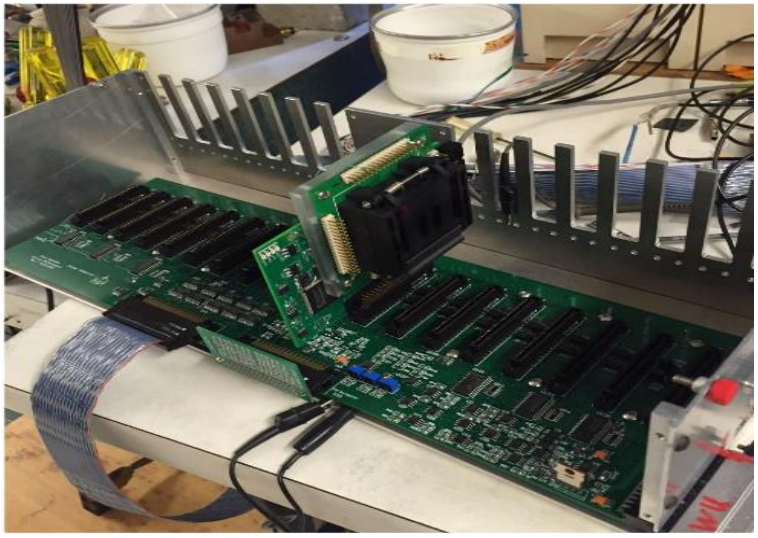


Fig.3 Block Diagram of a typical HINP5 channel © Korkmaz Anil

High Level System Design

- HINP5 chip generates analog pulse trains for both timing and energy of incident radiation.
- Need for digitization ?
- The Chipboards has
  - A simple Xilinx FPGA
  - 2 HINP5 chips
  - 3 ADC's for each HINP5 chip



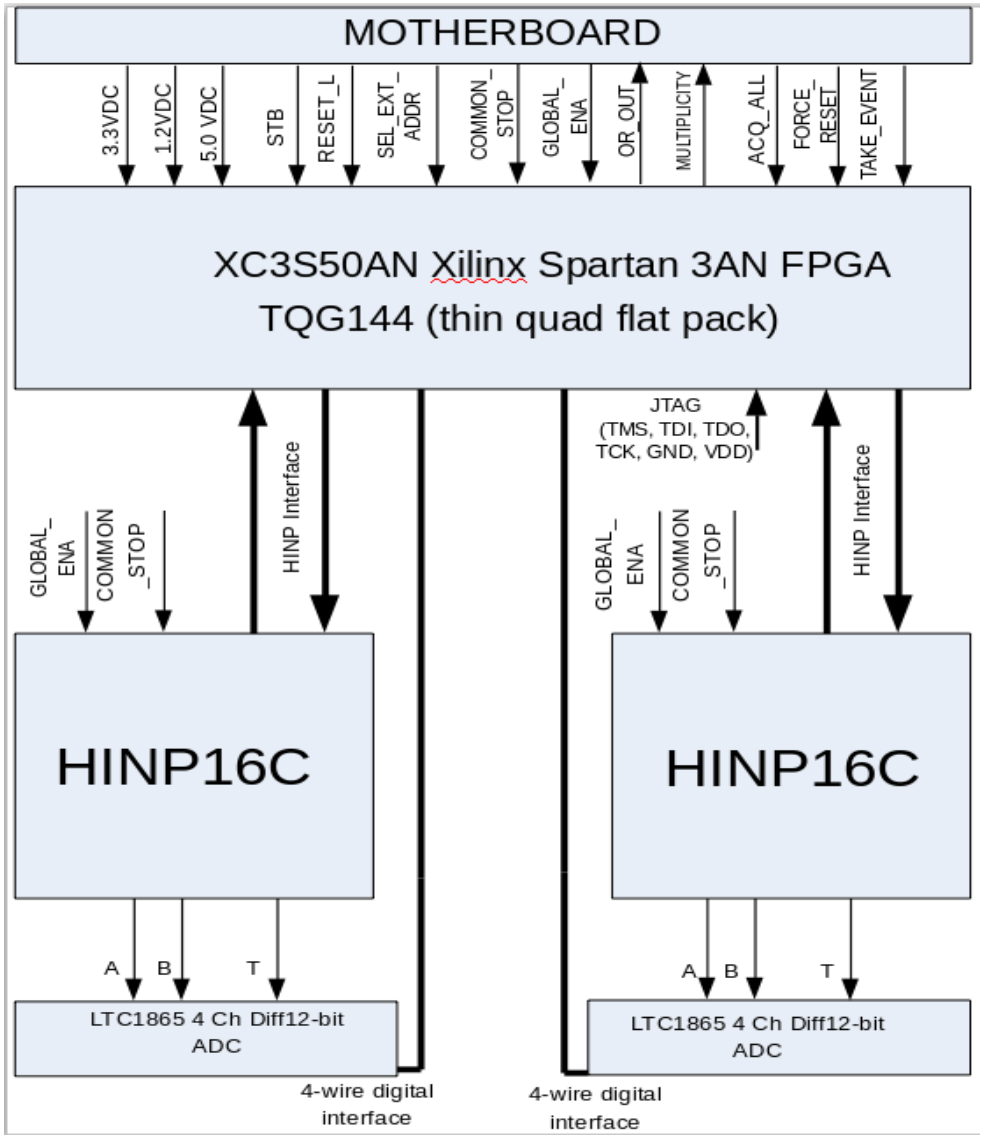


Fig.4 Block Diagram of the System

Digital Design using EDI Tools

- A Verilog driven digital design
- Cadence's EDI(Encounter Digital Implementation) computer aided design tools.
- Standard cell design approach
- Why Standard Cell Design ?
  - Building blocks: Logic cells from the digital standard cell library.
  - Less amount of design effort.
  - Speeds-up the design phase of the digital circuits[Eriksson et al., 2019].

Standard Cell Design Approach

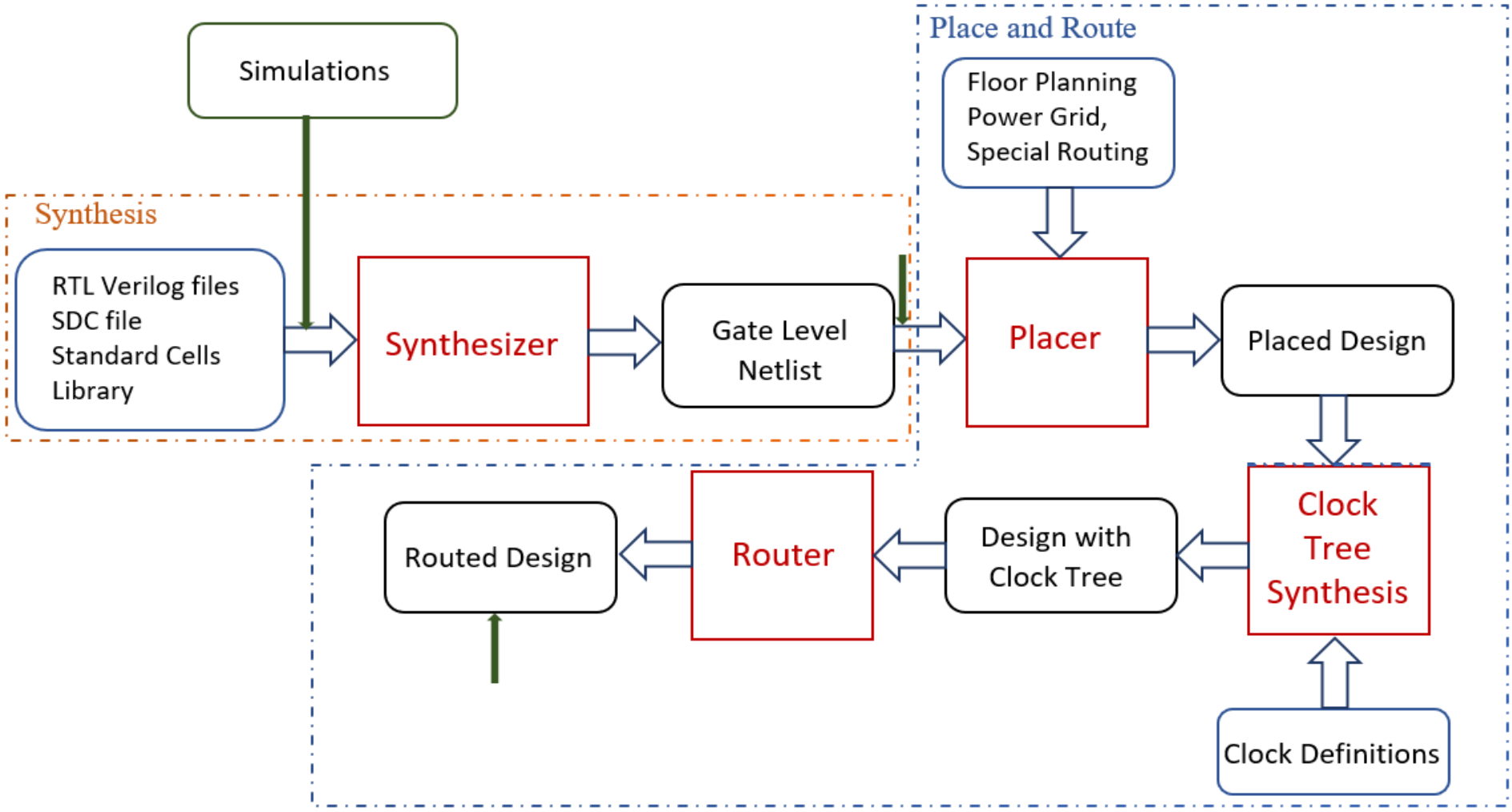


Fig.7 Standard Cell Design Flow

Fig.8 Exporting the design from cadence EDI tools to Cadence IC station

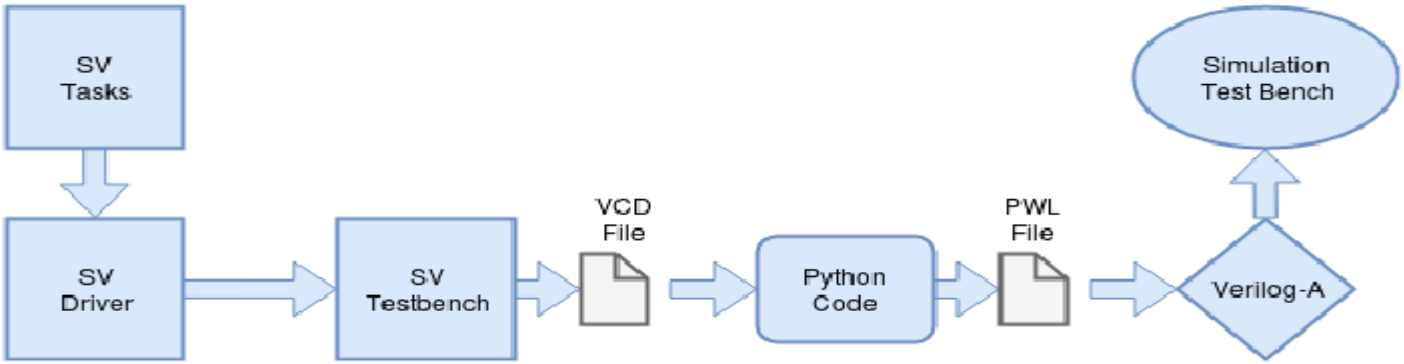
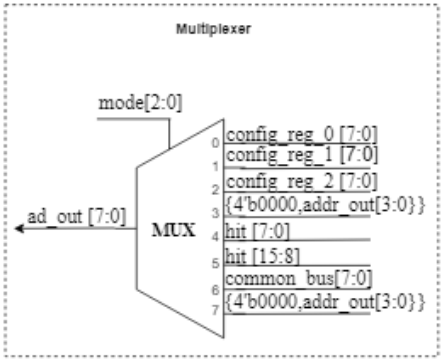
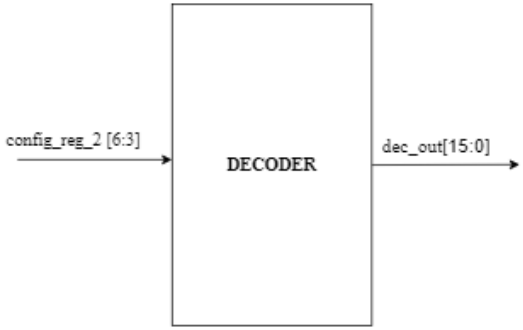


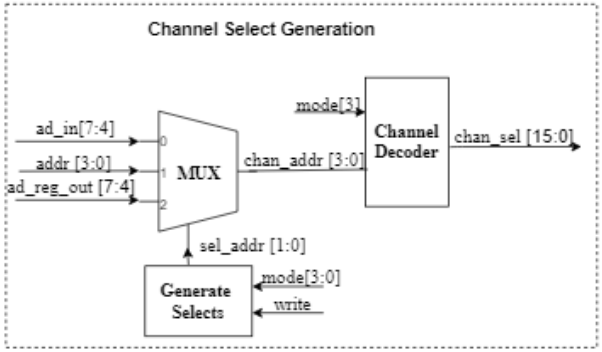
Fig.9 Electrical Simulation testing procedure © Bryan Orabutt

Common channel

HINP Digital

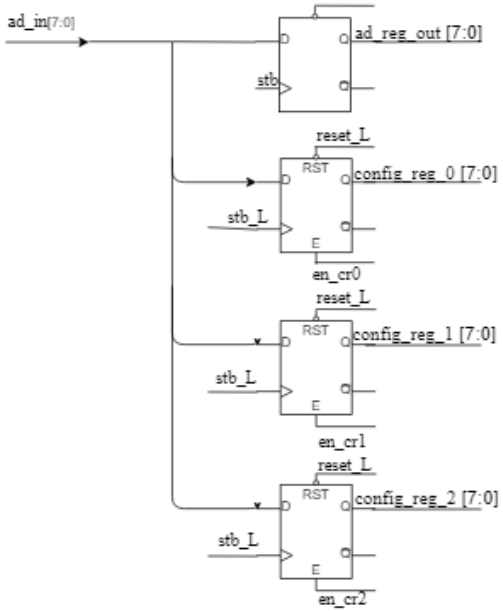


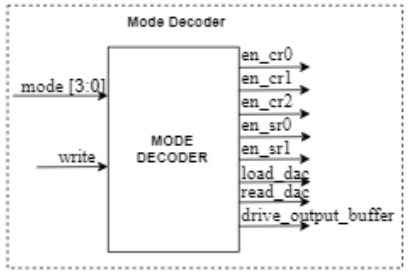


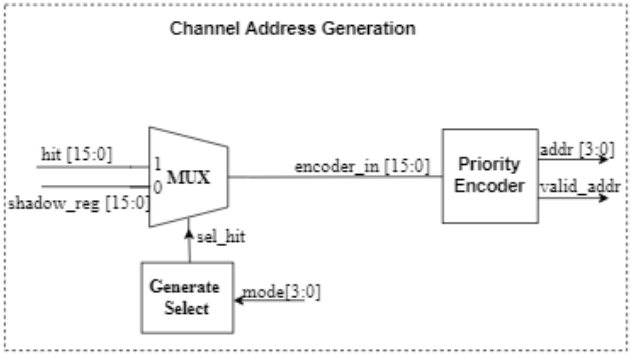


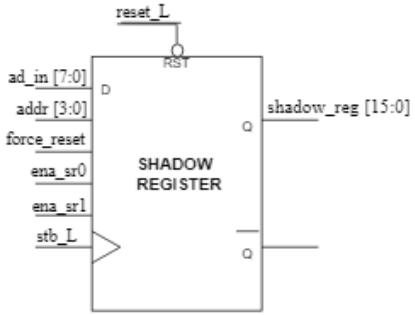
input ad_in [7:0]
input write
input stb
input hit [15:0]
input reset_L
input force_reset
input common_bus[7:0]

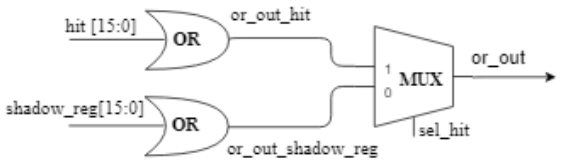
output ad_out [7:0]
output chan_sel [15:0]
output stb_L
output load_dac
output read_dac
output or_out
output drive_output_buffer
output config_reg_0 [7:0]
output config_reg_1 [7:0]
output config_reg_2 [7:0]
output dec_out [15:0]

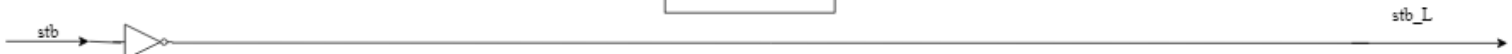












Configuration and Readout Electronics

- Provides proper control signals for all the sixteen signal channels and does readout.
  - 24 Configuration bits
  - Readout electronics

Configuration Register	BIT Position	Name	Function
config_reg_0	0	USE_EVEN_PULSER	0: Default 1: Pulsing EVEN channels
config_reg_0	1	USE_ODD_PULSER	0: Default 1: Pulsing ODD channels
config_reg_0	2	NOWLIN_CAP0	Selects one of the 16 capacitors to Set the NOWLIN delay (0.5pF to 8 pF)
config_reg_0	3	NOWLIN_CAP1	
config_reg_0	4	NOWLIN_CAP2	
config_reg_0	5	NOWLIN_CAP3	
config_reg_0	6	NOWLIN_MODE	0: Long Mode (Rise time constant: 12ns – 192ns) 1: Short Mode (Rise time constant: 1ns - 16ns)
config_reg_0	7	BUFFER_BIAS_HG	0: Bias is 50mv 1: Bias is 25mv

Table.1 Bit assignments of configuration register **cr_reg_0**

Configuration Register	BIT Position	Name	Function	Configuration Register	BIT Position	Name	Function
config_reg_1	0	BUFFER_BIAS_HG_POL	0: Positive Polarity 1: Negative Polarity	config_reg_2	0	TVC_2_USEC_MODE	1: TVC 2 usec full range 0: TVC 250 nsec range
config_reg_1	1	BUFFER_BIAS_LG	0: Bias is 50mv 1: Bias is 25mv	config_reg_2	1	EXT_CHARGE_AMP	0: Use internal charge amp 1: Use external charge amp
config_reg_1	2	BUFFER_BIAS_LG_POL	0: Positive Polarity 1: Negative Polarity	config_reg_2	2	HOLES	0: Electrons Collection 1: Holes Collection
config_reg_1	3	BUFFER_BIAS_TVC	0: Bias is 50mv 1: Bias is 25mv	config_reg_2	3	DLY_VC0	4-bit value that determines the 16 delay times by the auto reset block before the channels auto reset.
config_reg_1	4	BUFFER_BIAS_TVC_POL	0: Positive Polarity 1: Negative Polarity	config_reg_2	4	DLY_VC1	
config_reg_1	5	AGND_TR0	Allows to adjust AGND voltage (1.4 to 1.8v in 50mV step)	config_reg_2	5	DLY_VC2	
config_reg_1	6	AGND_TR1		config_reg_2	6	DLY_VC3	
config_reg_1	7	AGND_TR2		config_reg_2	7	DLY_VC4	1 bit that determines the width of the digital reset to be either 100nsec or 1usec

Table.2 Bit assignments of configuration registers **cr_reg_1** & **cr_reg_2**

Modes of Operation

write	mode[2:0]	Operation
0	"000"	ad_out <--- config_reg_0[7:0]
0	"001"	ad_out <--- config_reg_1[7:0]
0	"010"	ad_out <--- config_reg_2[7:0]
0	"011"	ad_out <--- {addr_out[3:0], 4'b000}
0	"100"	ad_out <--- hit_reg_lower[7:0]
0	"101"	ad_out <--- hit_reg_upper[7:0]
0	"110"	ad_out <--- 8'd0
0	"111"	ad_out <--- {addr_out[3:0] , 4'b0000}
1	"000"	config_reg_0 <--- ad_in[7:0]
1	"001"	config_reg_1 <--- ad_in[7:0]
1	"010"	config_reg_2 <--- ad_in[7:0]
1	"011"	addr_in <--- ad_in[7:4]
1	"100"	shadow_reg_lower <-- ad_in[7:0]
1	"101"	shadow_reg_upper <-- ad_in[7:0]
1	"110"	dac_reg(addr) <--- ad_in[7:0]
1	"111"	addr_in <--- ad_in[7:4]

Table 3. Modes of Operation

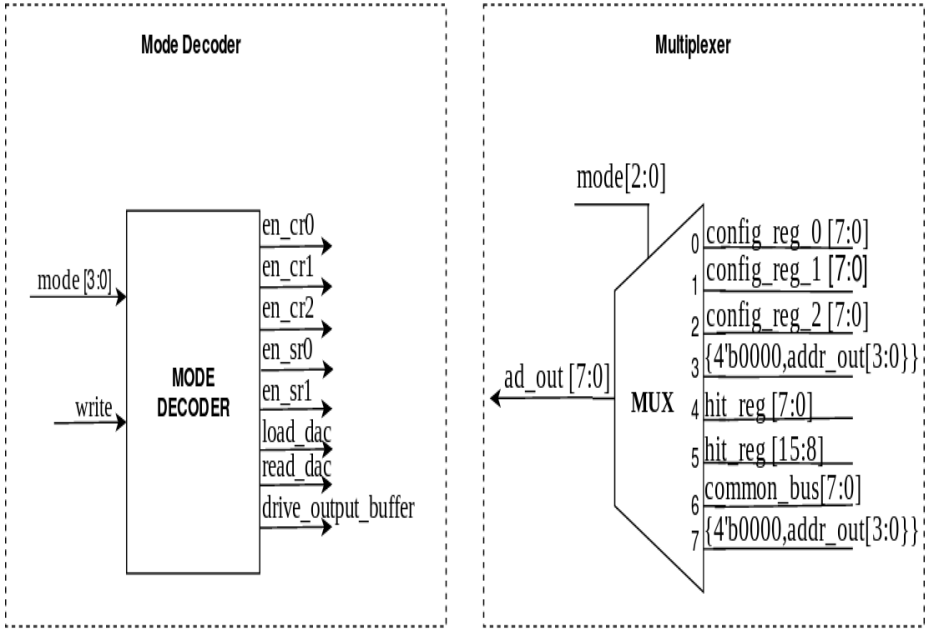


Fig.11 Mode Decoding Circuit in common channel

ad_reg [7:0] <--- {addr, mode}

addr: Upper nibble of ad_reg

mode: Lower nibble of ad_reg

Channel Address Generation

Verilog logic of channel address generation :

```
/**** Digital Logic for Channel Address Generation ****/

// MUX Logic for choosing either hit register or shadow register

reg [15:0] encoder_in;

always @(*) begin

        case (sel_hit)
                0: encoder_in = shadow_reg;
                1: encoder_in = hit;
        endcase
end

// Generate sel_hit bit for choosing either hit register or shadow register


assign sel_hit = (mode[2:0] == 3'd3 & ~write)? 1'b0 : 1'b1;

// Priority Encoder Block

integer j;

always @(*) begin
    if (|encoder_in) begin
        for (j=15; j>=0 ; j=j-1) begin
                if (encoder_in[j]) begin
                        addr = j;
                        valid_addr = 1'b1;
                end
        end
    end
    else begin
        addr = 4'd0;
        valid_addr = 1'b0;
    end
end
```

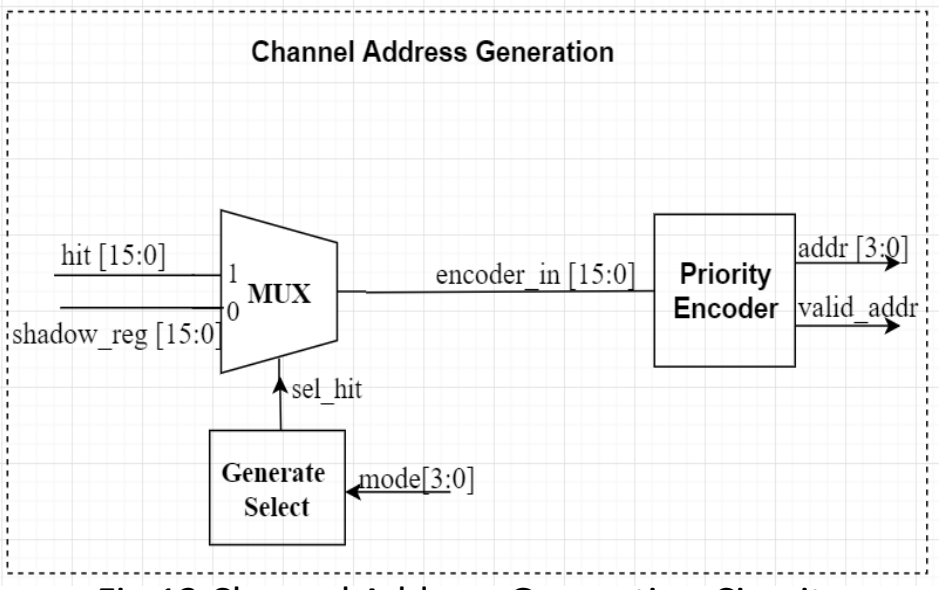


Fig.12 Channel Address Generation Circuit

Example:

If odd channels are hit;

hit[15:0] → encoder_in[15:0]	addr[3:0]	valid_addr
1010_1010_1010_1010	0001	1

readout;

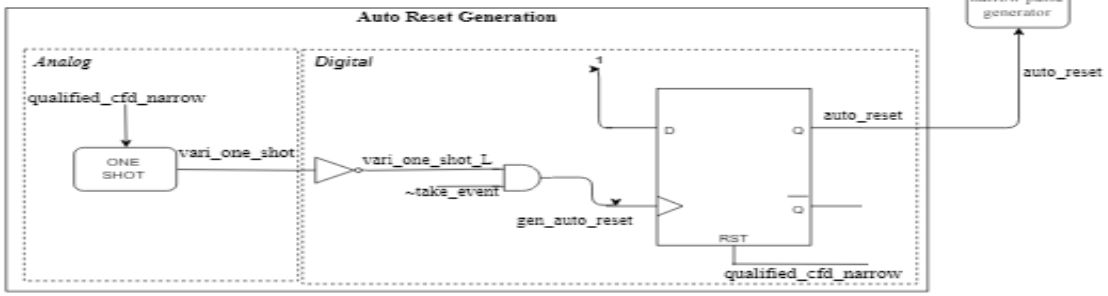
hit[15:0] → encoder_in[15:0]	addr[3:0]	valid_addr
1010_1010_1010_1000	0011	1

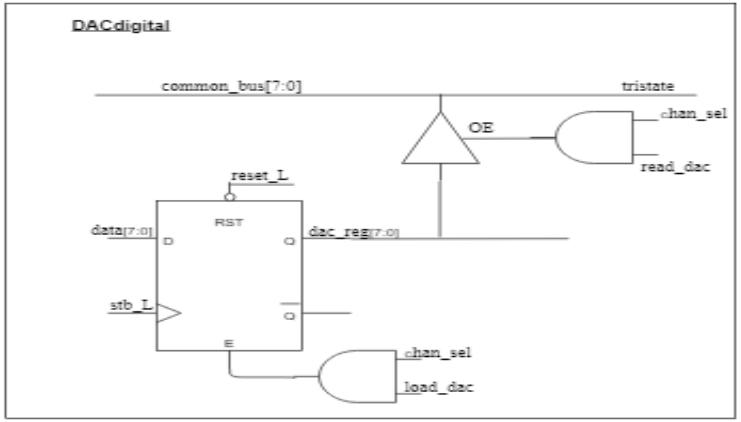
Signal Channel

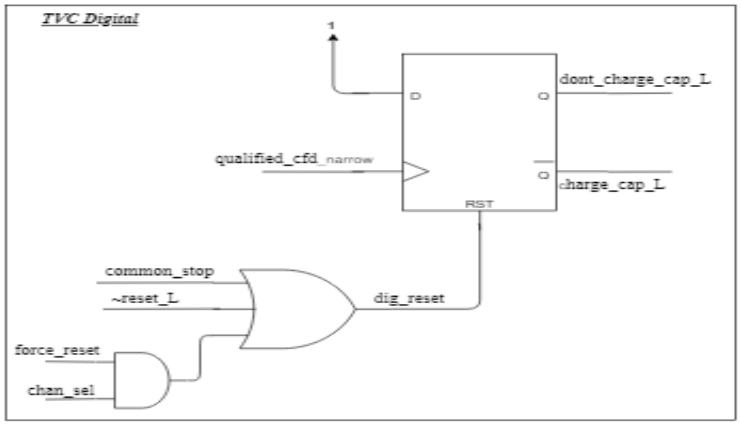
Channeldigital

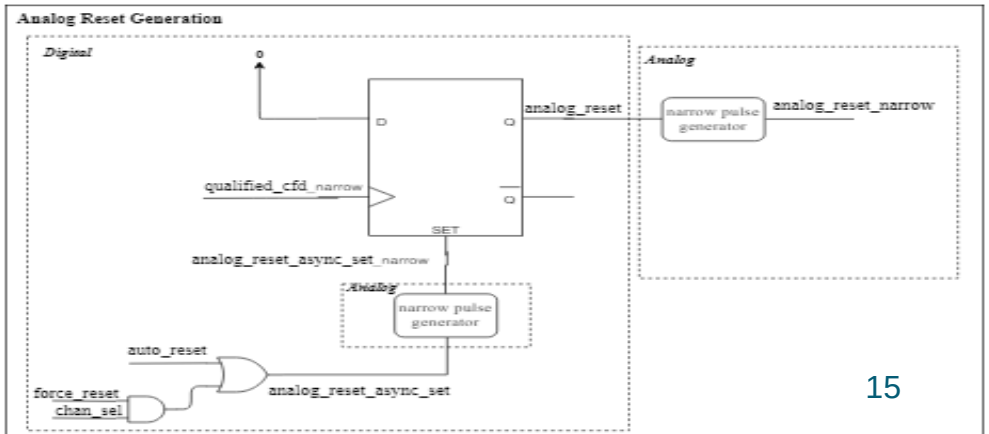

```
input reset_L
input force_reset
input stb_L
input take_event
input chan_sel
input common_stop
input leave_reset
input qualified_cfd
input vari_one_shot_L
input cfd_out
input load_dac
input read_dac
input spi_chan
input global_ena
input drive_output_buffer
input acq_all
input auto_reset_narrow
input analog_reset_async_set_narrow

output auto_reset
output analog_reset_async_set
output dont_charge_cap_L
output charge_cap_L
output analog_reset
output hit
output common_bus [7:0]
output read_chan
output dac_reg [7:0]
```









Layout of HINPdigital

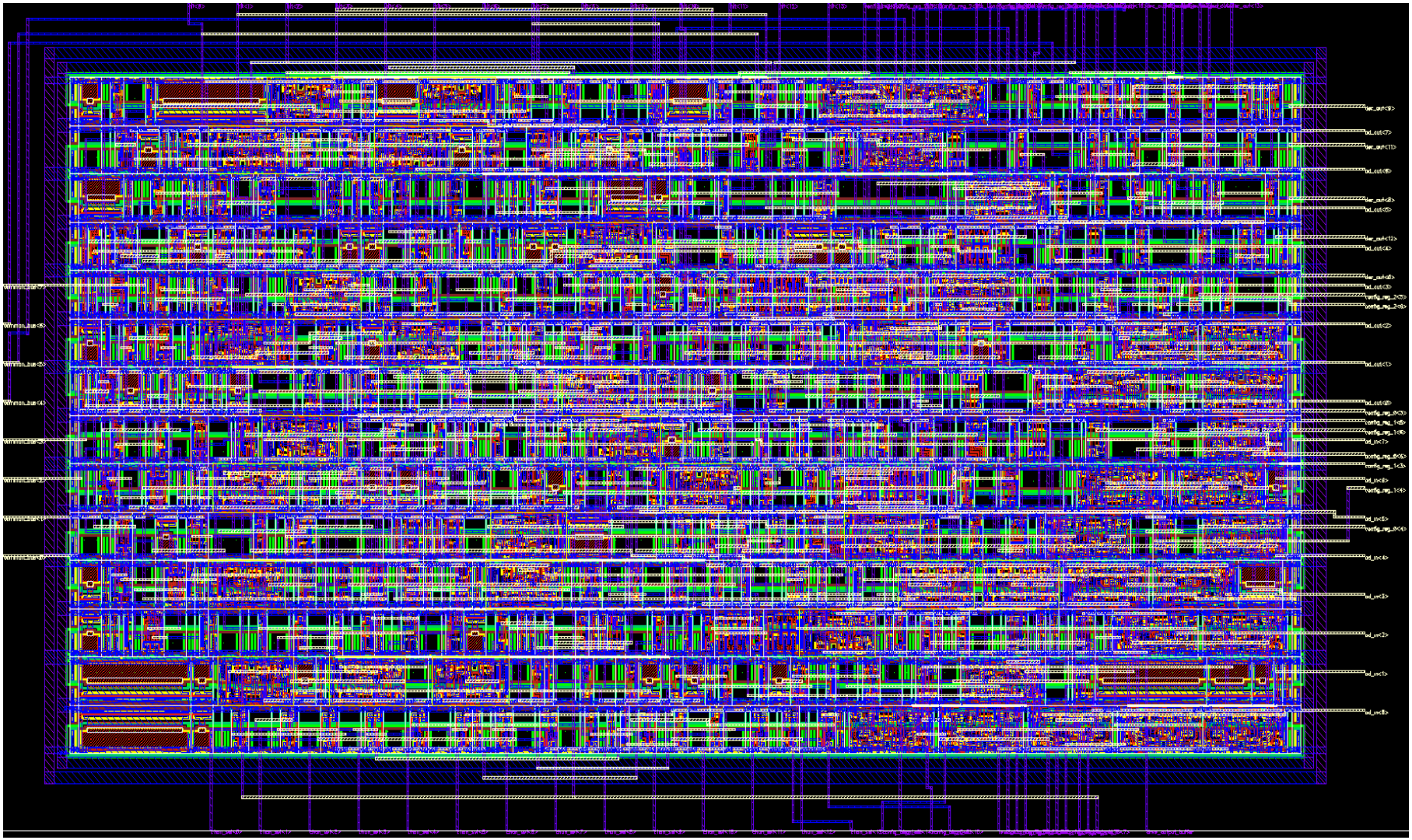


Fig.15 Layout of HINP common channel digital logic generated by place & route tool

Layout of Channeldigital

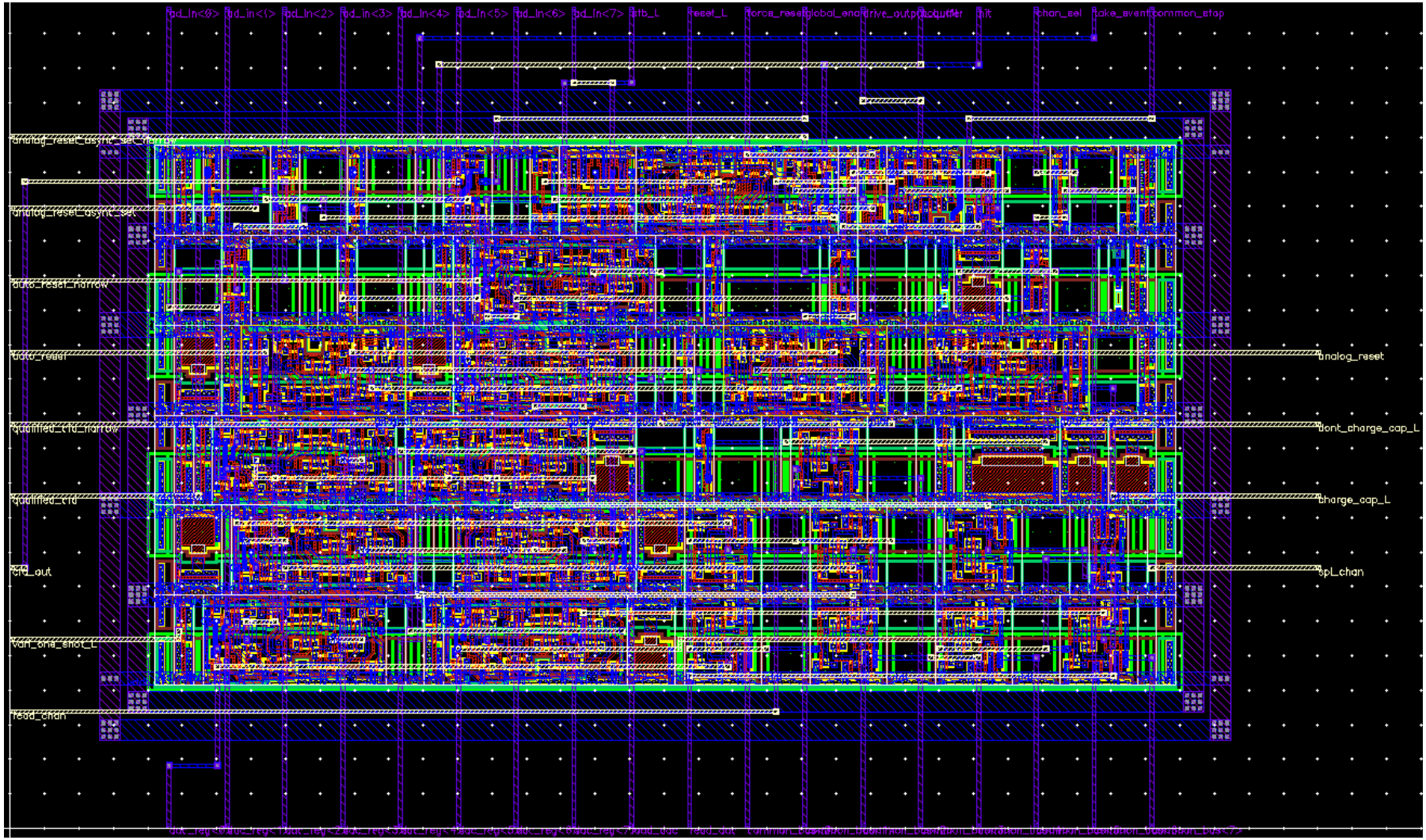


Fig.16 Layout of HINP signal channel digital logic generated by place & route tool

Summary

- Layout Dimensions:
  - HINP Digital: 427 µm X 223 µm
  - Channel Digital: 191 µm X 119 µm
- A Verilog driven design carried out using cadence EDI tools and digital standard cell library in 0.35-micron AMS design Kit.
- Electronic simulation performed using NC-Sim to verify the behavioral description of the digital logic implemented.
- Electrical simulations were also performed on the digital designs.
- The simulation results are as expected with out any issues.

Future Work

- Enhance the current SDC (Synopsys Design Constraints) file.
- The configuration and readout electronics digital design need to be binded with other analog circuits in the chip.
- Chip level simulations including the parasitic extraction still need to be done.
- Final Layouts of the HINP5 chip need to be finished.
- Expected to send for fabrication in late 2019 submissions to MOSIS.

Queries ?


Thank
you

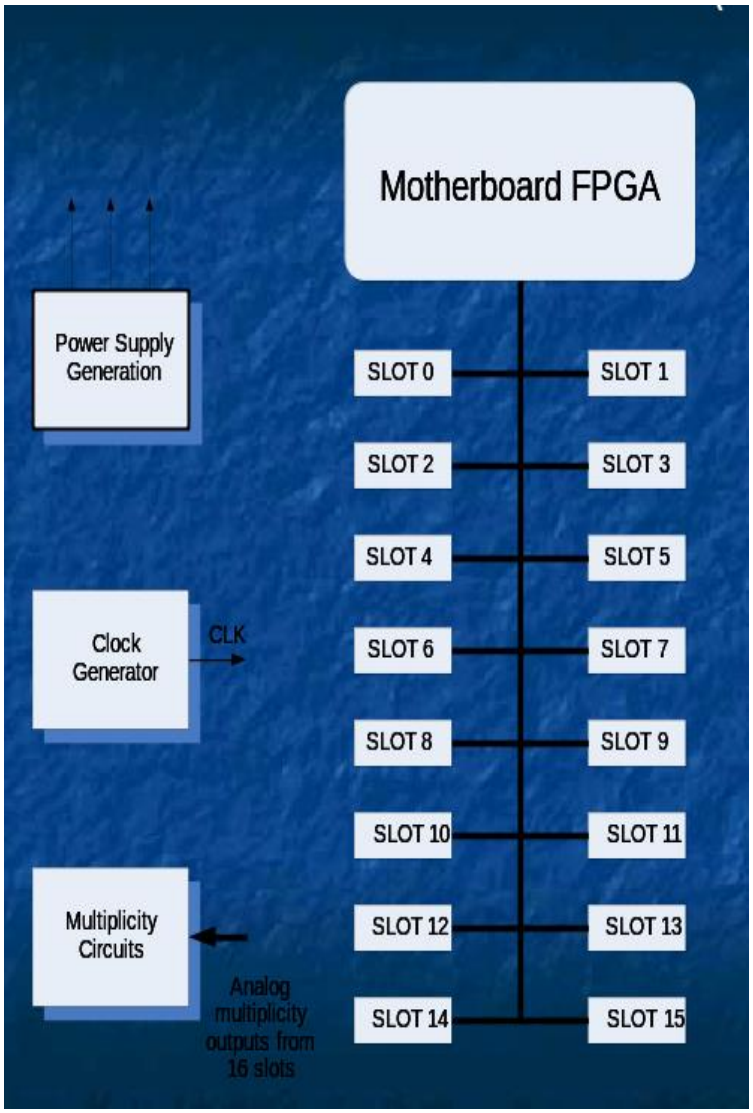


Fig.5 Block Diagram of the Motherboard

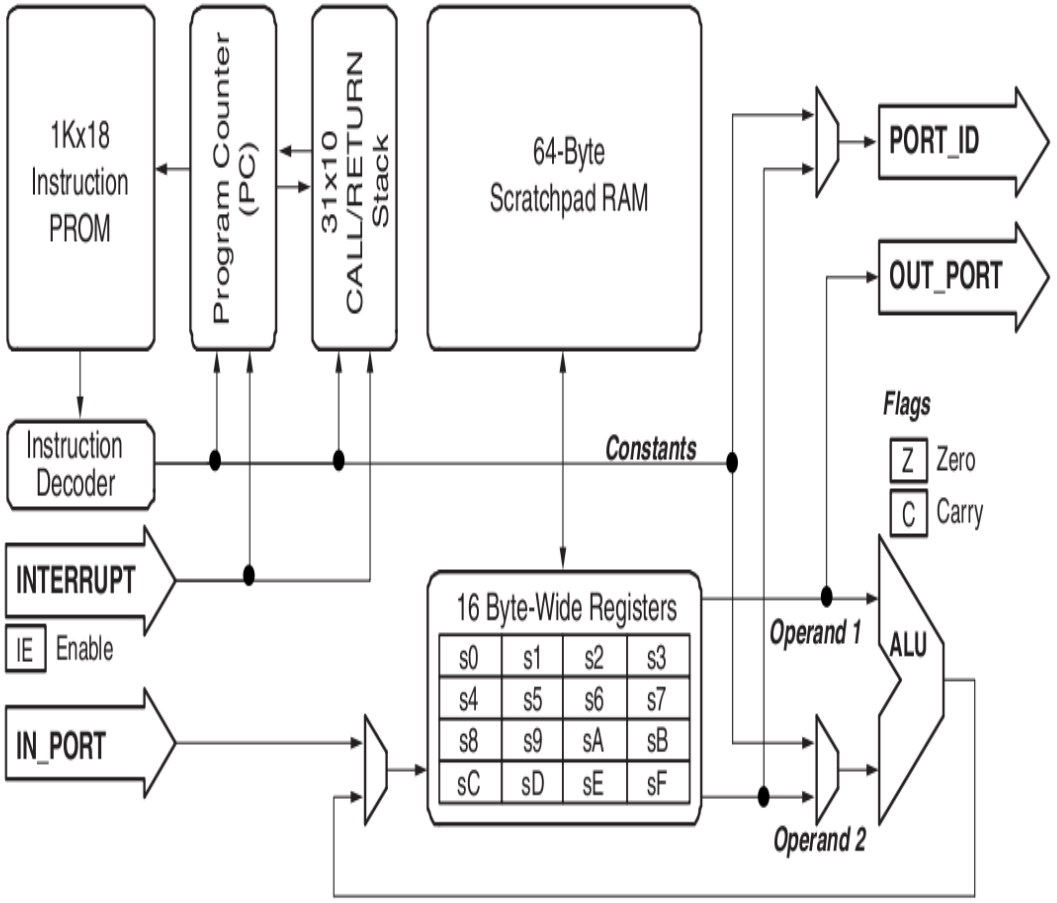


Fig.6 An 8-bit Pico blaze embedded microcontroller in FPGA.

Shadow Register

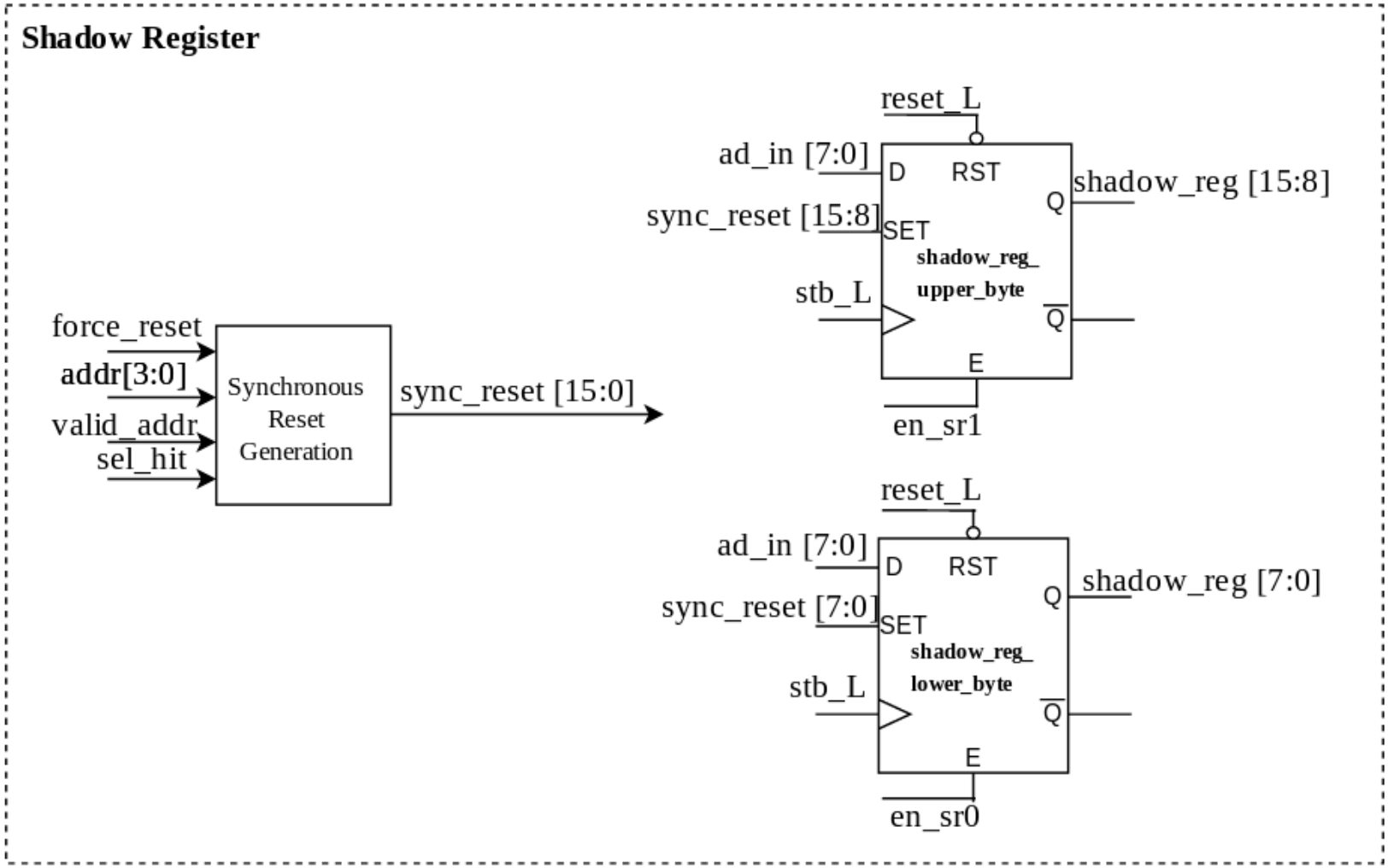


Fig.10 Shadow register in common channel

DAC Digital

Bit Position	Name	Function
0	DATA[0]	5-bit value that sets the threshold for the DAC at what level cfd fires
1	DATA[1]	
2	DATA[2]	
3	DATA[3]	
4	DATA[4]	
5	DATA[5]	This bit sets the polarity of the DAC 0: Positive Polarity 1: Negative Polarity
6	LOCAL_ENA	0: Disables the signal channel locally 1: Enables the signal channel locally
7	UNUSED	UNUSED

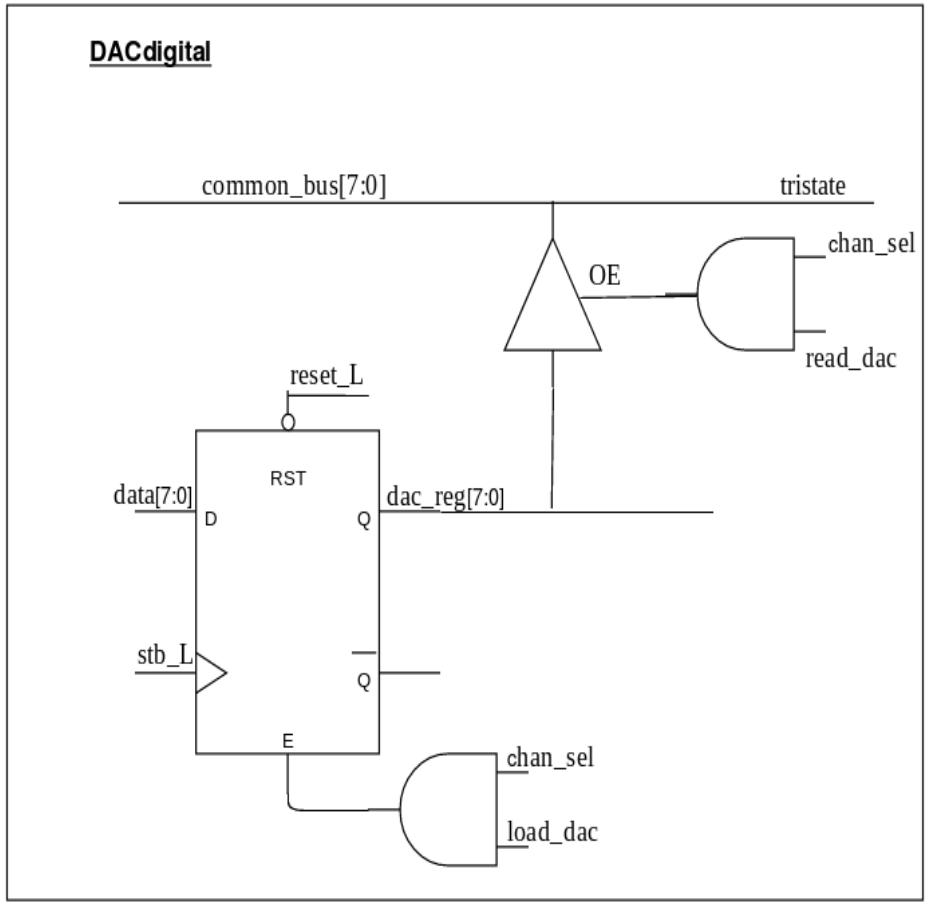


Fig.13 DAC digital circuit in signal channel

Table 4. BIT assignments of DAC register in signal channel