Southern Illinois University Edwardsville

Design and Analysis of the Linear Branch of an Integrated Circuit for Use in Nuclear Physics Experiments Employing Si-Strip Detectors

by
Anıl Korkmaz

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George L. Engel, D.Sc

Advisory Committee

Bradley Noble, D.Sc
Timothy York, PhD.

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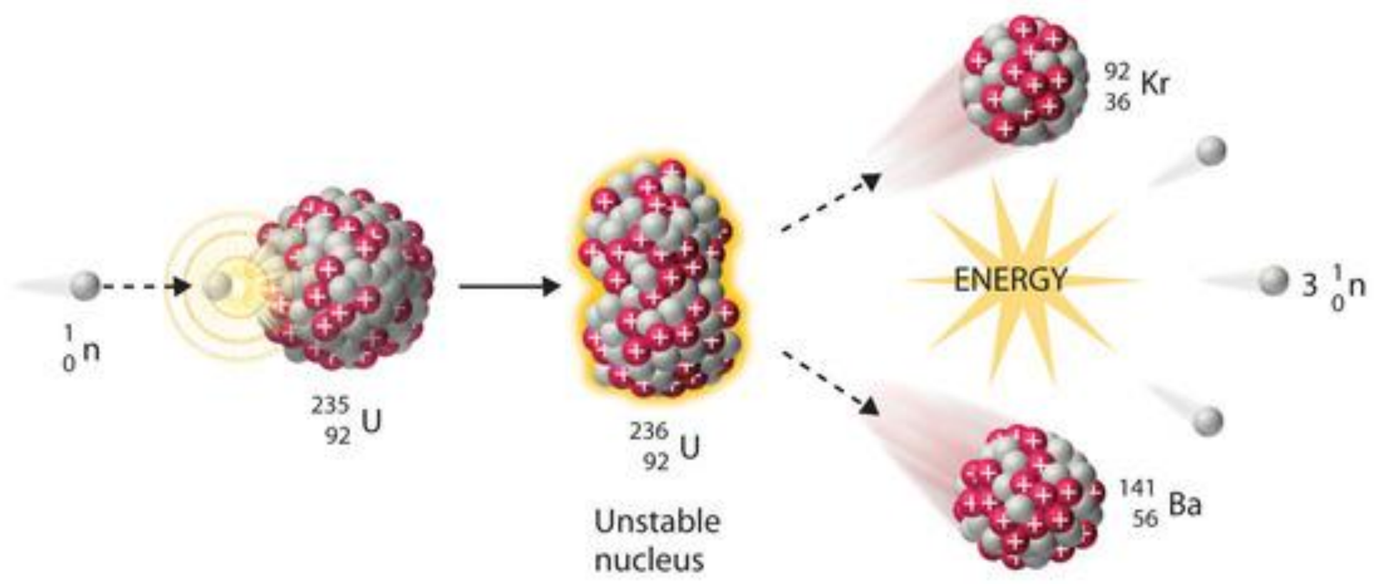
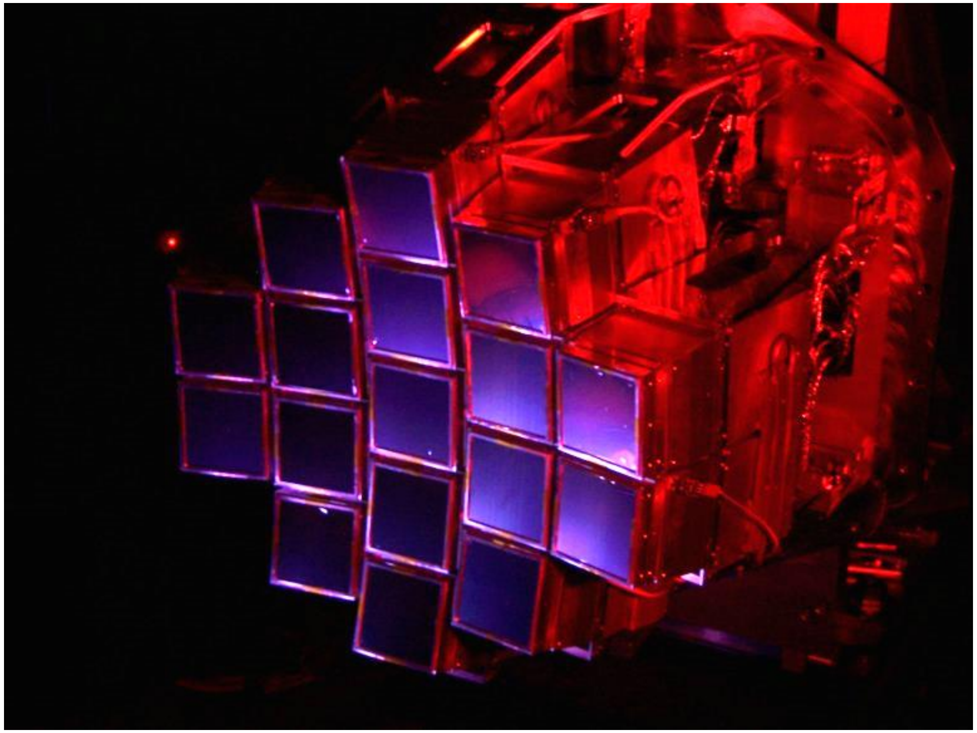
Ionizing Radiation

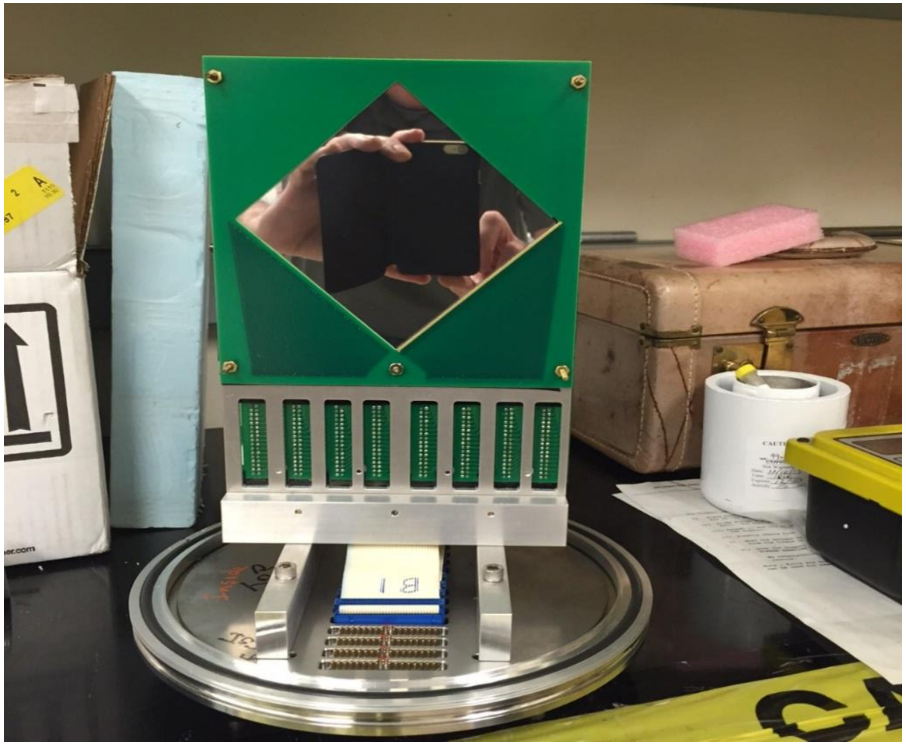
- WUSTL Nuclear Reactions group works on ionizing radiation and unstable nuclei to obtain information about origins of the Universe.
- An ion hits a stable atom and converts it to an unstable atom. This interaction emits particles such as alpha, beta, gamma, neutron, etc.
- Scientists in WUSTL are trying to obtain meaningful information from the position/timing information, energy levels and particle type.

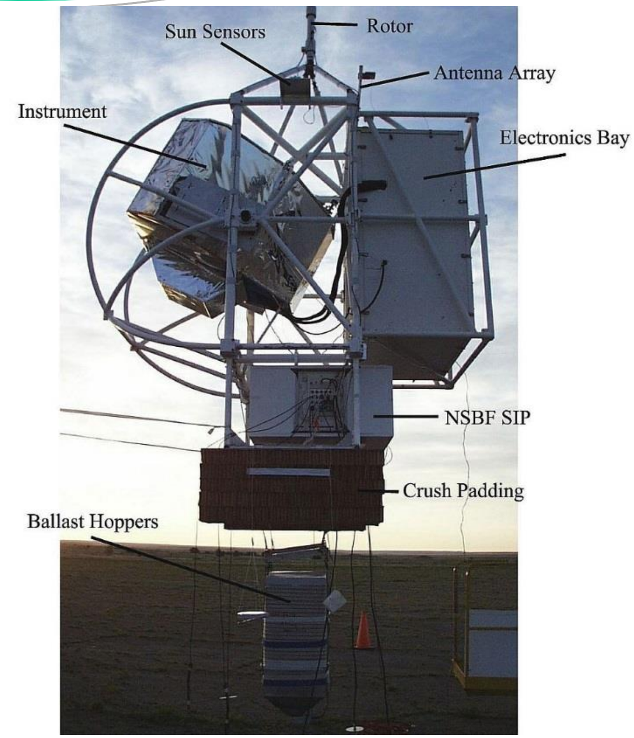


Si- Strip Detectors

- Particles are detected by Si- strip detectors, then position and timing information is acquired.
- A custom IC is needed to accurately measure energy of the radiation.
- Si- strip detectors are fully depleted reverse biased p-n junctions.
- Charge = Q_e * (Particle Energy / 3.6)

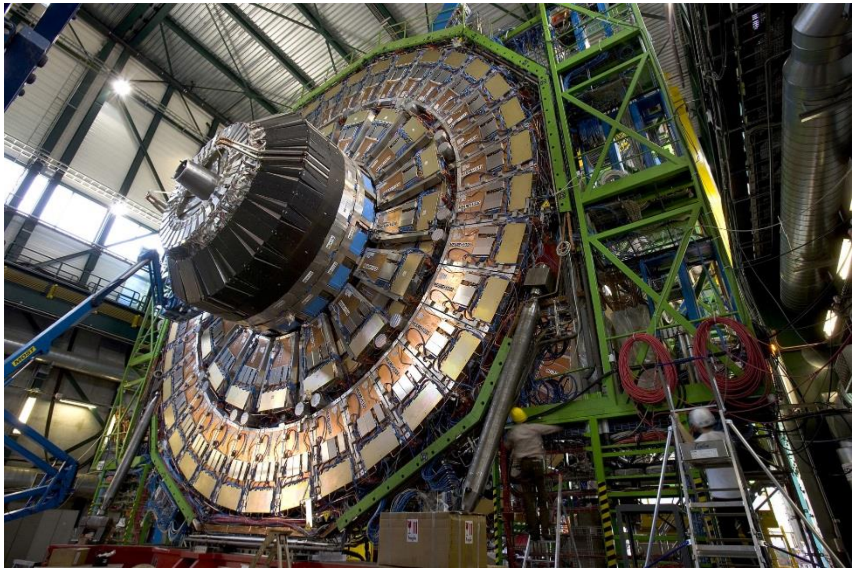






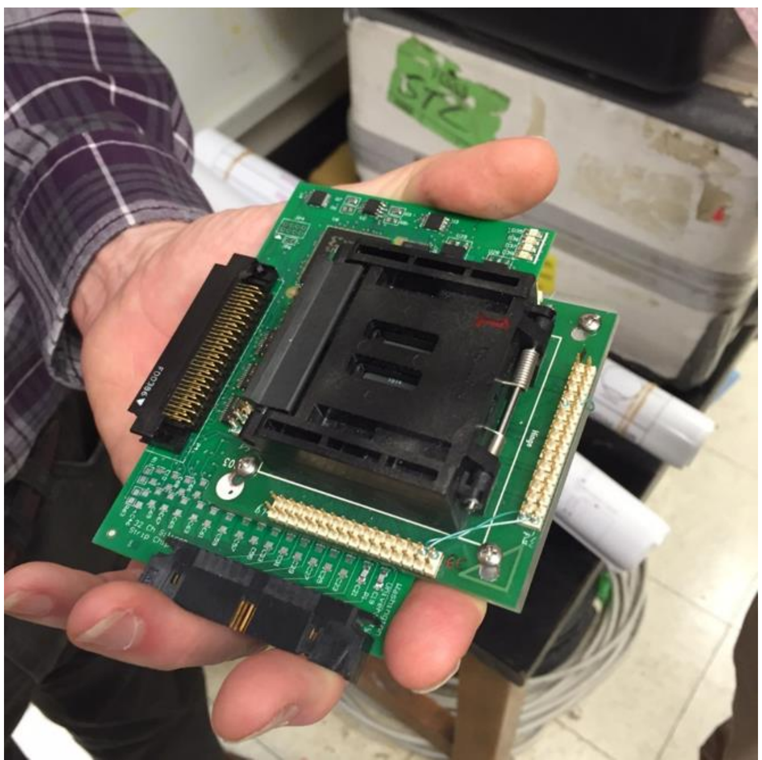
Si- Strip Detectors Applications

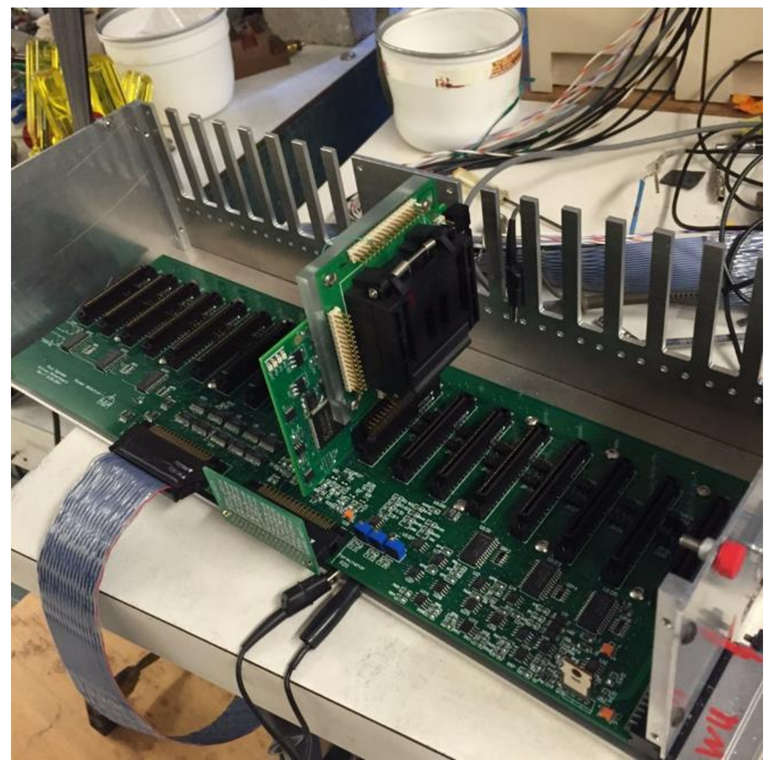
- In physics; High Energy Proton-Proton Collision, Large Hadron Collider (LHC), High Luminosity Large Hadron Collider (HL-LHC).
- In astrophysics; SilEye (Silicon Eye) detectors, Compton Telescope and Nuclear Compton Telescopes.
- In medicine; Nanodosimetry, Mammography, MRI, CT.



Radiation Monitoring System

- Every Si- strip detector array connected to 2 custom Integrated Circuits (IC). (16+16 Channel).
- Every chip board has 2 ICs, an FPGA (Field Programmable Gate Array) and three ADCs (Analog-to-Digital Converter).
- Every motherboard contains up to 16 chip boards (512 Channels).



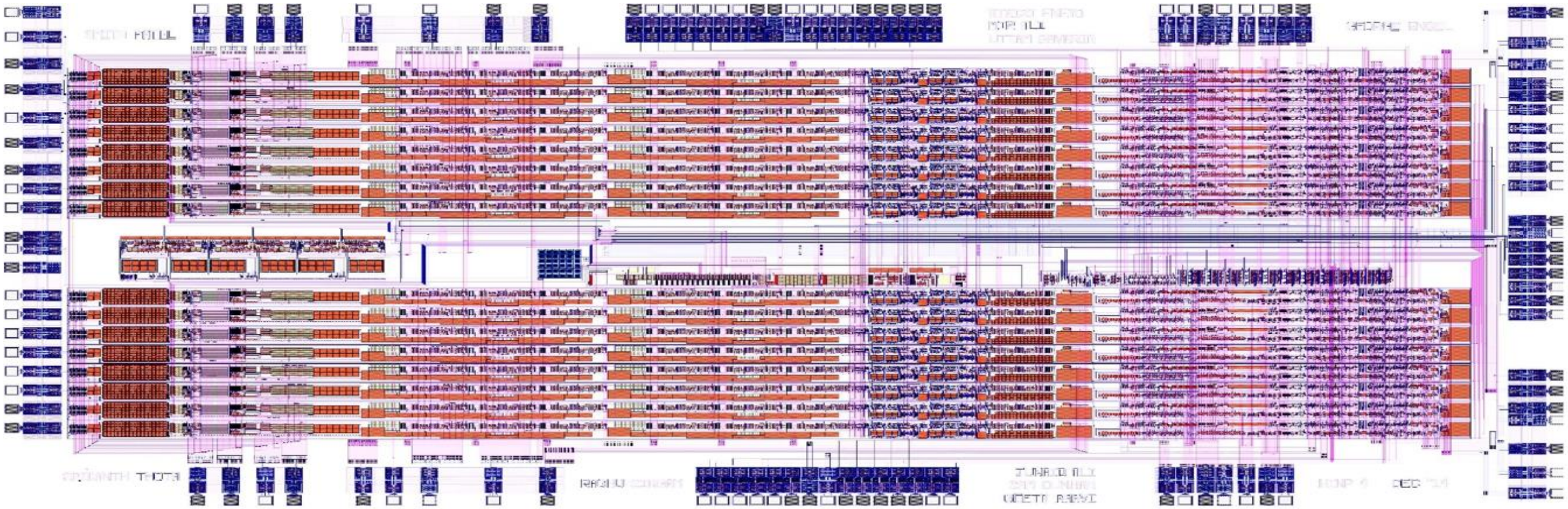


HINP IC – Heavy Ion Nuclear Physics IC

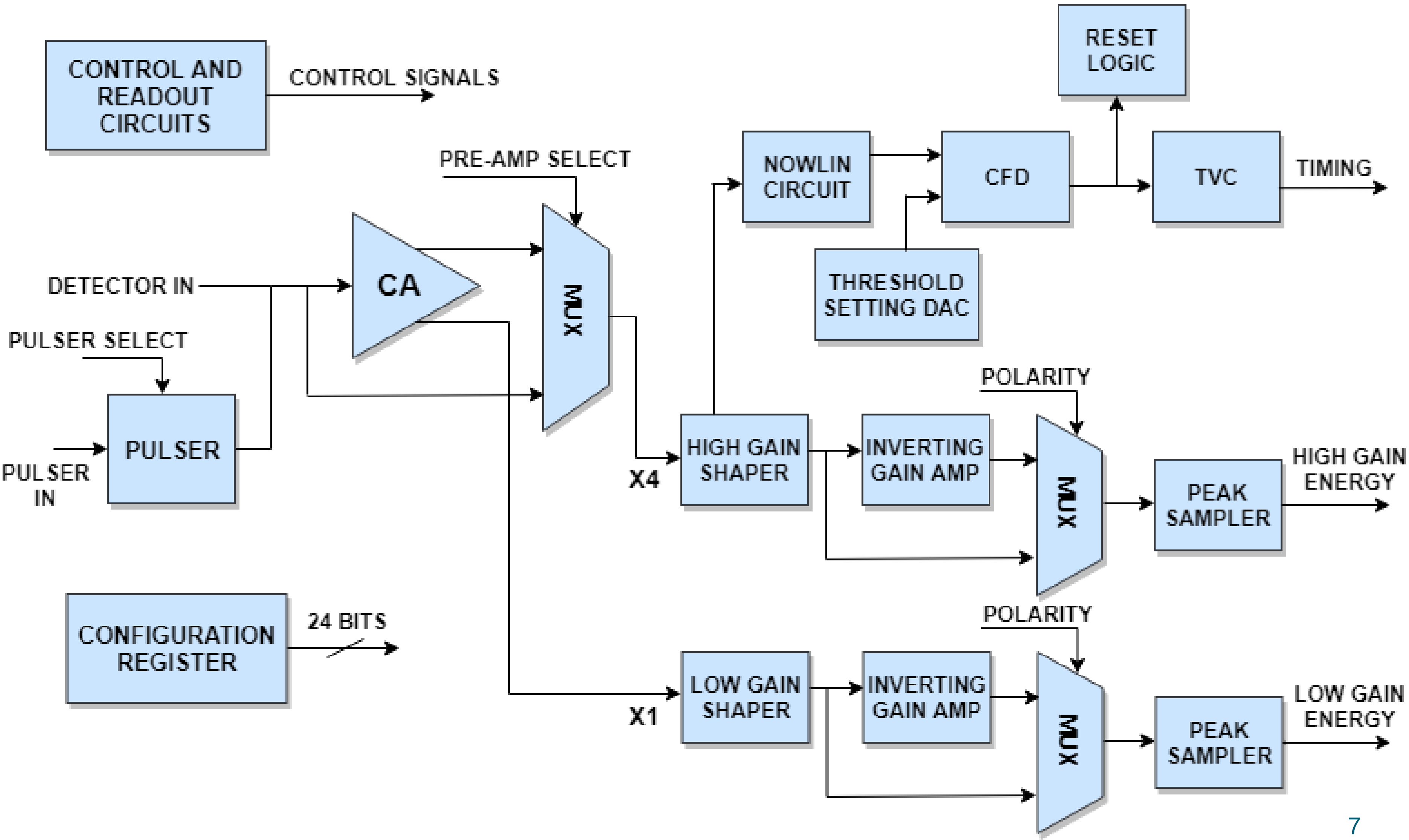
Why did we need to redesign HINP?

- To improve linearity,
- To improve energy resolution,
- 0.5 µm process was going away,
- To obtain lower power consumption,
- To improve time resolution,
- To add external pre-amplifier option,
- Reduce the silicon die and shrink the package from 128 pins to 64 pins,
- 0.35 µm process with 3.3V supply voltage is allowed us to achieve such specifications.

Current HINP chip → Needed to be improved



HINP5 – Block Diagram

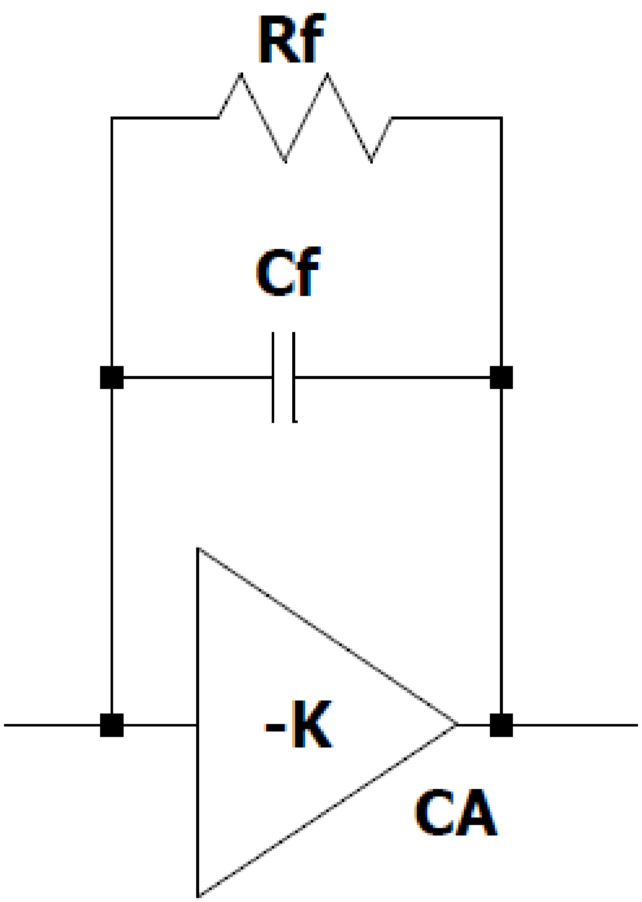


HINP5 / Linear Branch – Features

- Very low noise (< 25 keV).
- High dynamic range (100 keV - 400 MeV).
- Detection of both polarities (Electron and Hole Collection)
- Two different gain modes opearating simultaneously, namely high gain and low gain.
- Utilization of external pre-amplifers for even higher gain.
- Utilization of external pulser for verification purposes.

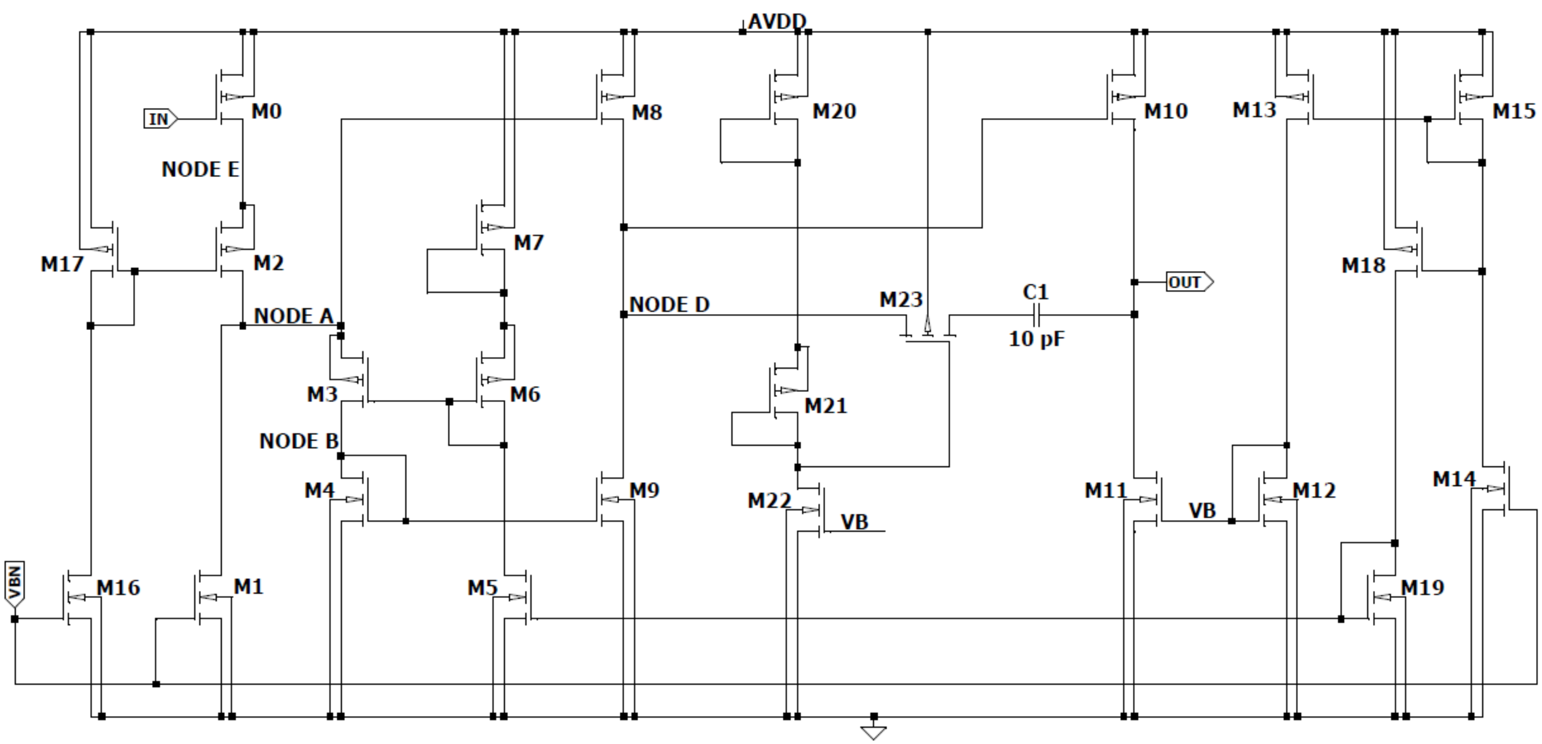
Feedback Capacitance and Resistance

- $Q_{max} = Q_e * \frac{E_{max}}{3.6eV}$
- $V_{max} = V_{DD} - |V_{TP}|$
- $C_F = \frac{Q_{max}}{V_{max}}$ (7 pF)
- $R_F = \frac{t_{decay}}{2.2 * C_f}$ (1.5 MΩ)



Core Amplifier

- Dual Cascode Structure (DCS) (Input stage)
- Complementary Common Source Amplifier (First Stage)
- Common Source Amplifier (Second Stage)
- 10 pF compensation capacitor and compensation resistor.
- Input transistor with a very large shape factor (1 mm/0.35 µm)



Core Amplifier's Performance and Frequency Response

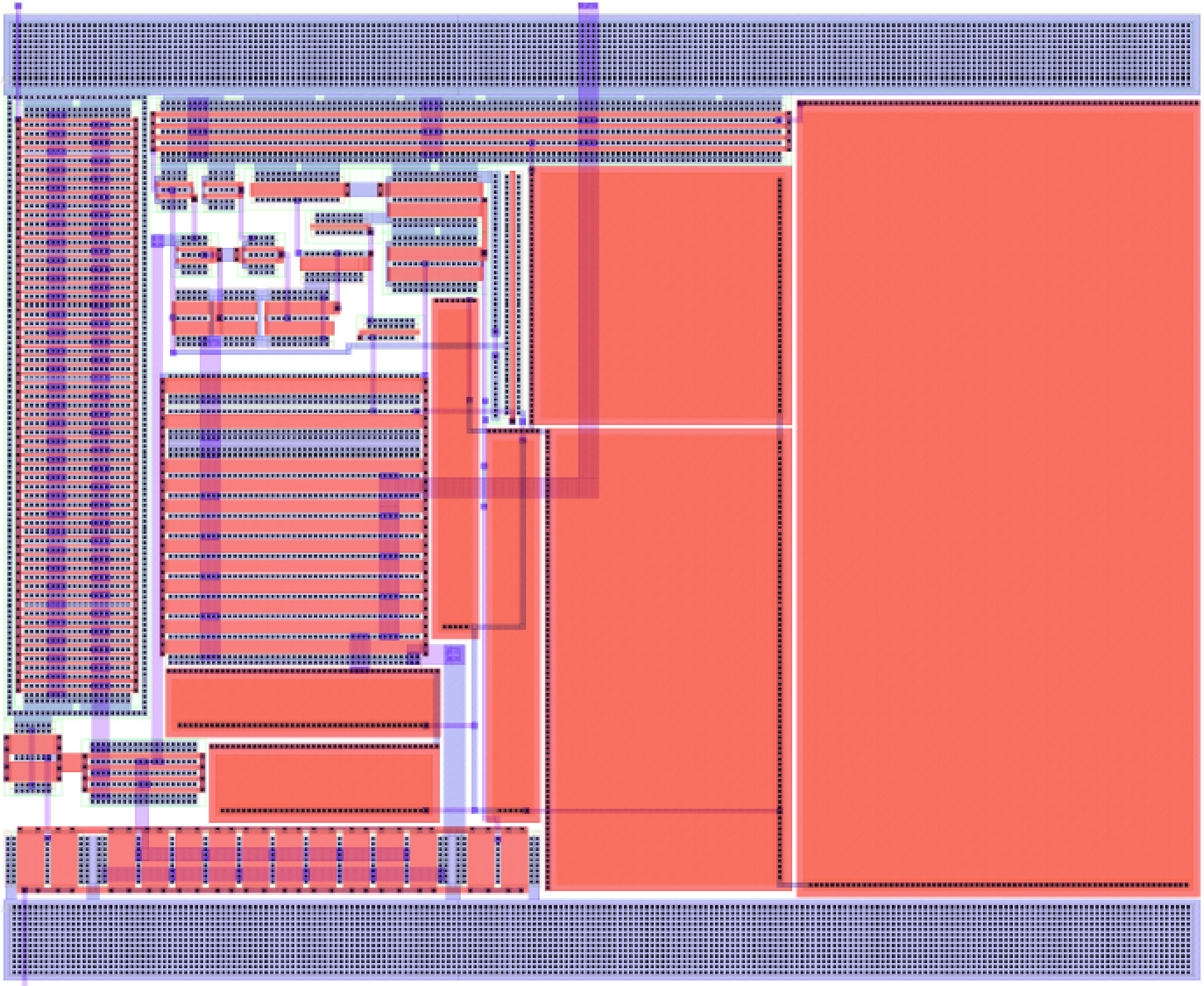
	Calculation	Simulation
Gain	106 dB	98 dB
GBW	160 MHz	130 MHz
Phase M. ($C_{DET} = 25pF$)	43°	46°
Corner Frequency	2.5 kHz	2.8 kHz
t_r ($C_{DET} = 200pF$)	60 ns	75 ns

Table 1: Performance comparison between calculation and simulation

	Pole Location (Hz)
Node A	$248 \cdot 10^6$ (Parasitic)
Node B	$318 \cdot 10^6$ (Parasitic)
Node D	$2.5 \cdot 10^3$ (Dominant)
Node E	$183 \cdot 10^6$ (Parasitic)
Output	$27 \cdot 10^6$ (Cancelled)

Table 2: Core amp. pole locations

Core Amplifier Layout



Width: 120 μm

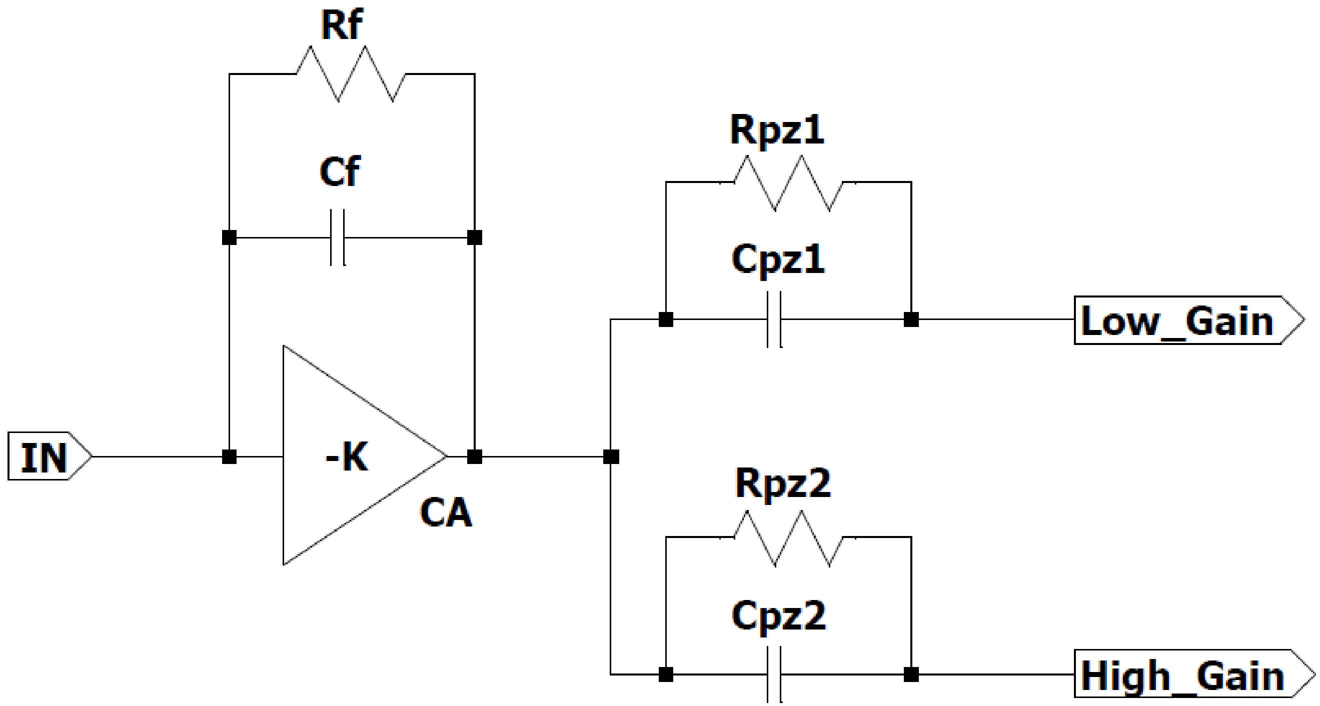
Length: 180 μm

Area: 0.2 mm^2

Charge Amplifier / Pole – Zero Cancellation

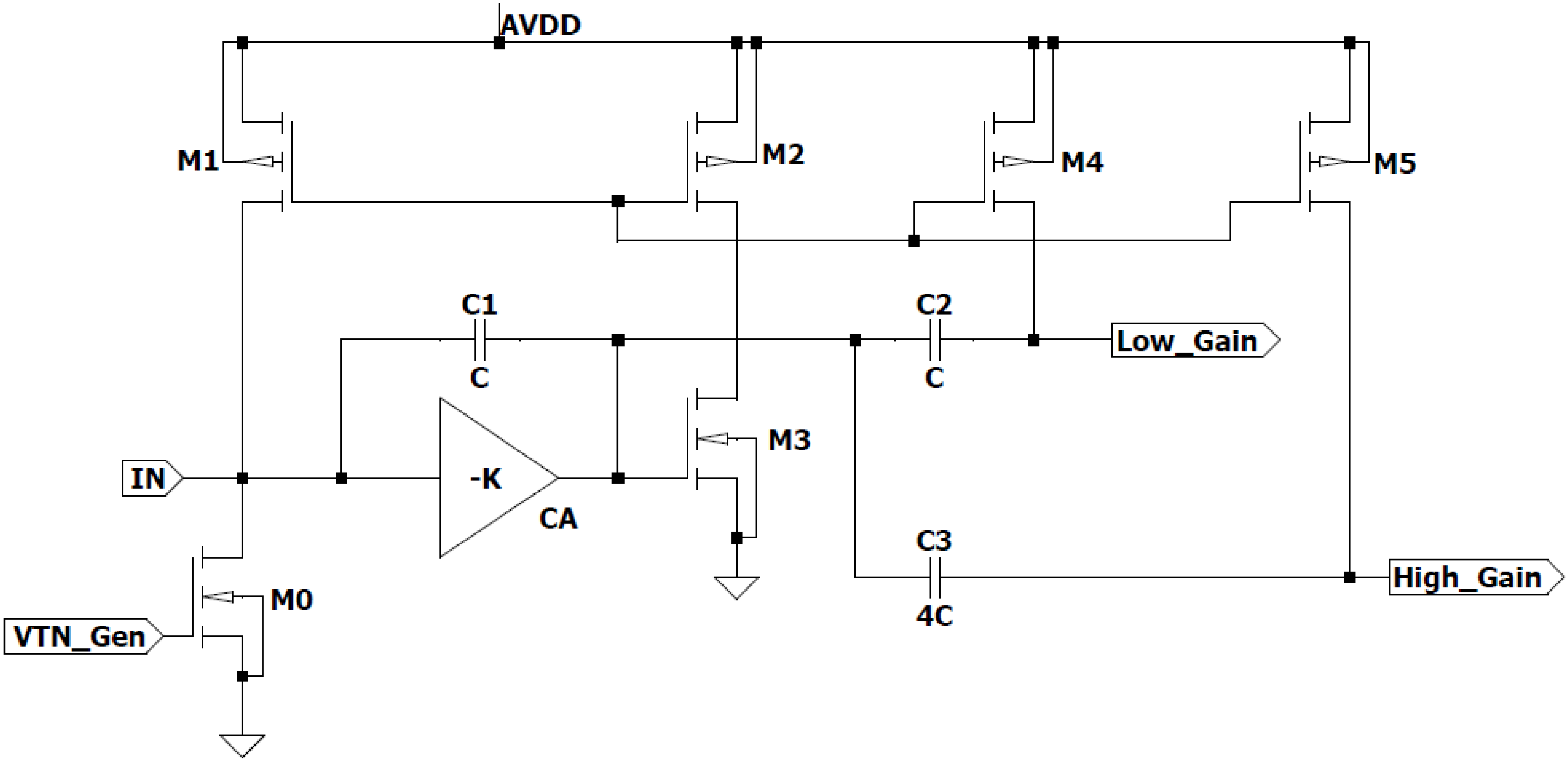
- $TF(s) = \frac{Q_{out}}{Q_{in}} = \frac{R_f}{s*C_f*R_f+1} * \frac{s*C_{pz}*R_{pz}+1}{R_{pz}}$

- $C_f * R_f = C_{pz1} * R_{pz1} = C_{pz2} * R_{pz2}$ where $C_{pz2} = 4 * C_{pz1}$



Continuous Reset Circuit with Pseudo MOS Resistors

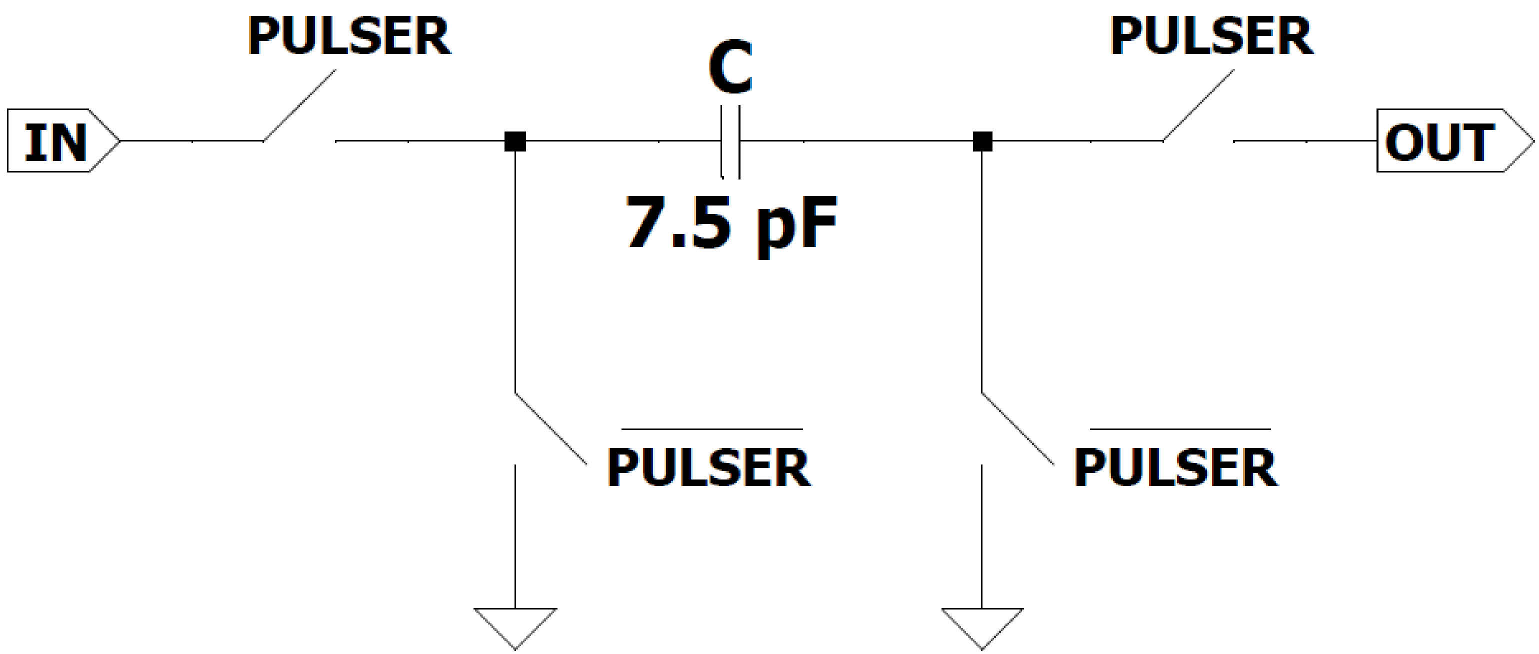
- Real resistors occupy very large area and do not allow to maximize dynamic range for both polarities.



Electron Collection

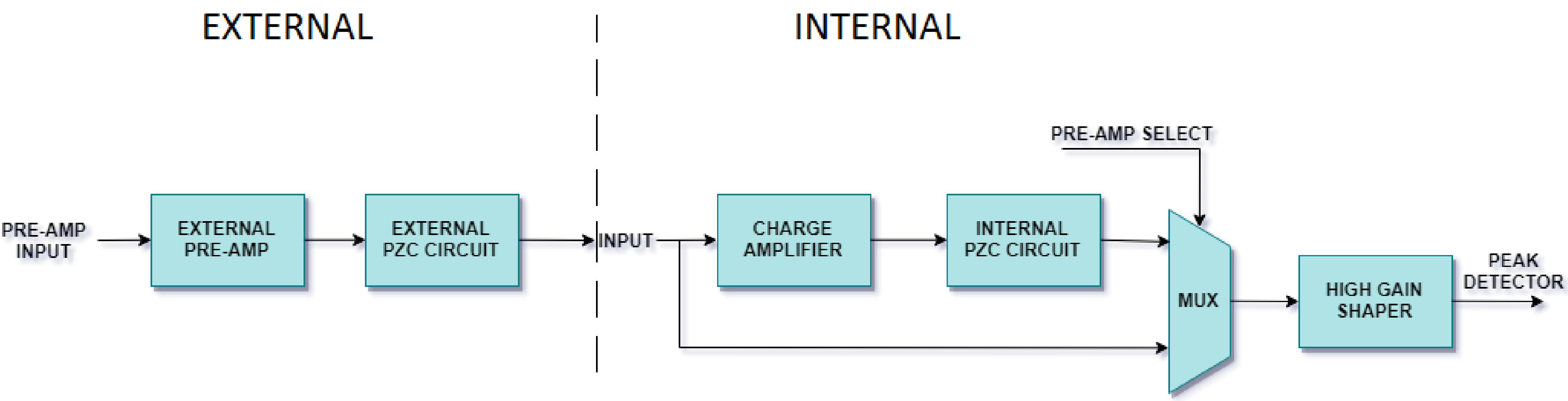
Pulser Block

- External pulser provides verification
- Instead of charge package, it provides voltage pulses



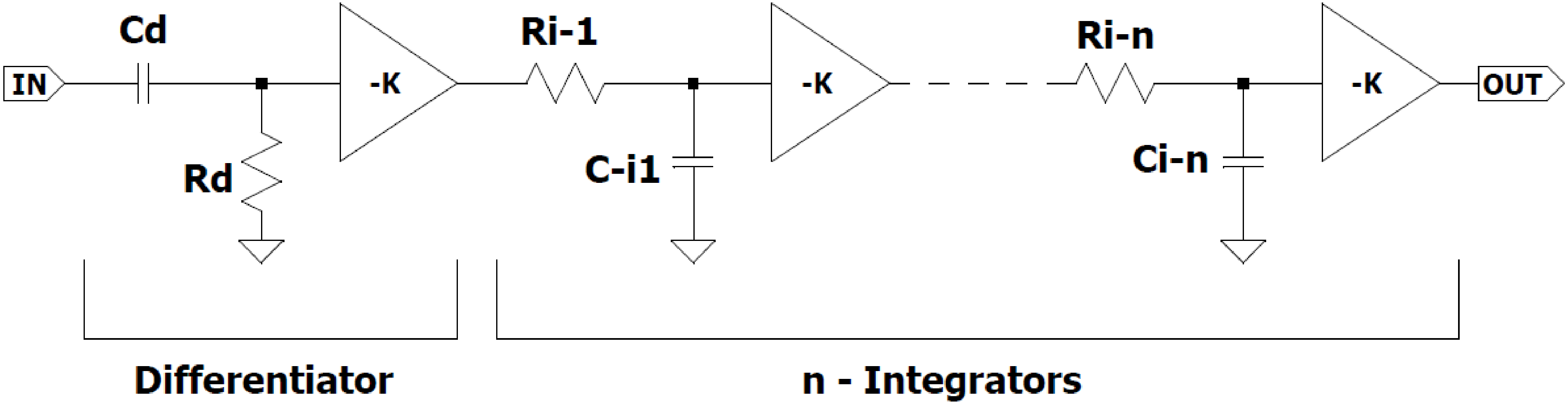
External Pre-Amplifier

- It cannot be used with an internal charge amplifier
- It is user's responsibility to provide an external pole-zero cancellation



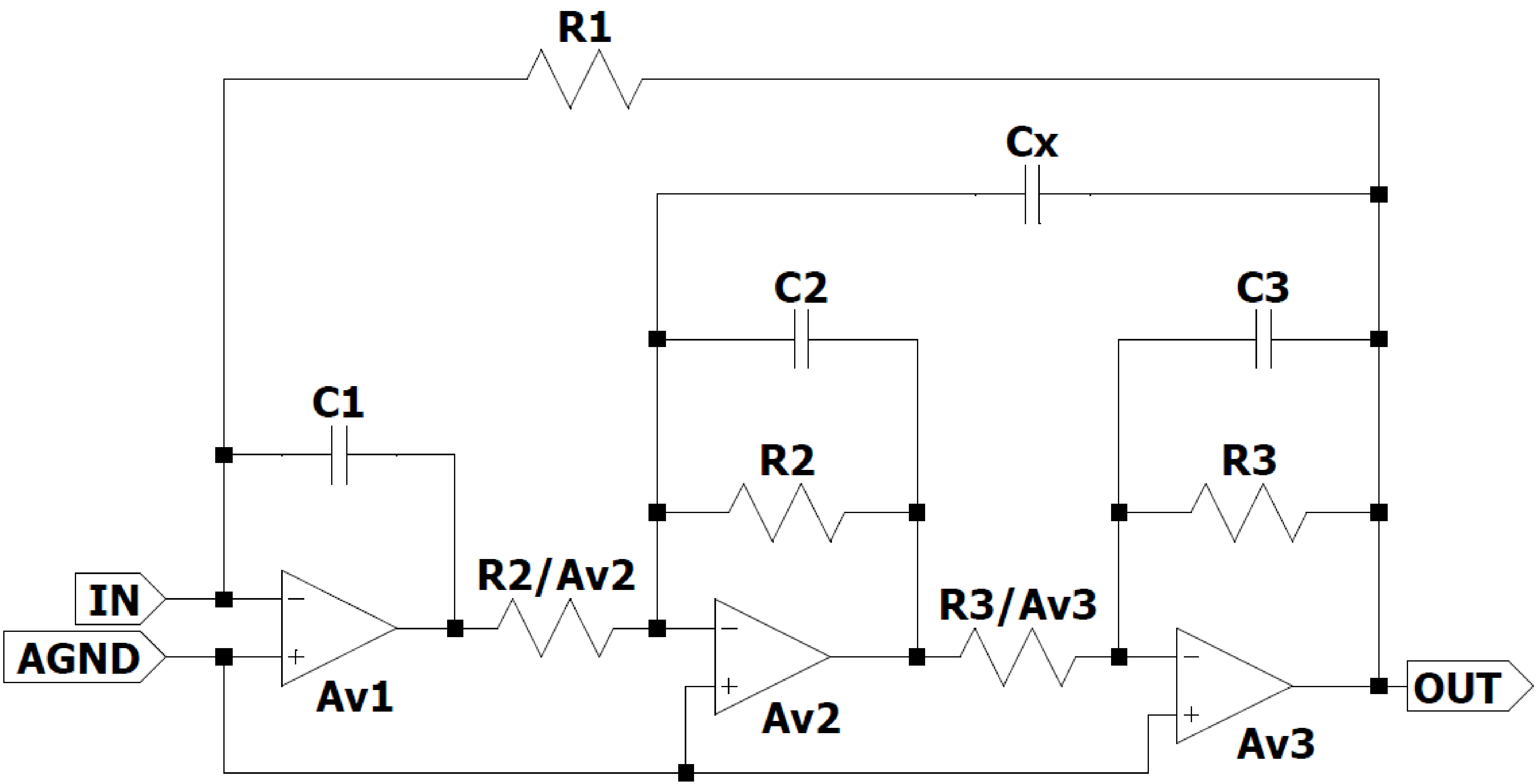
Semi-Gaussian Shaper

- Maximizes signal-to-noise ratio by limiting bandwidth
- Amplitude proportional to the energy level of a particle
- Order of the filter: n+1



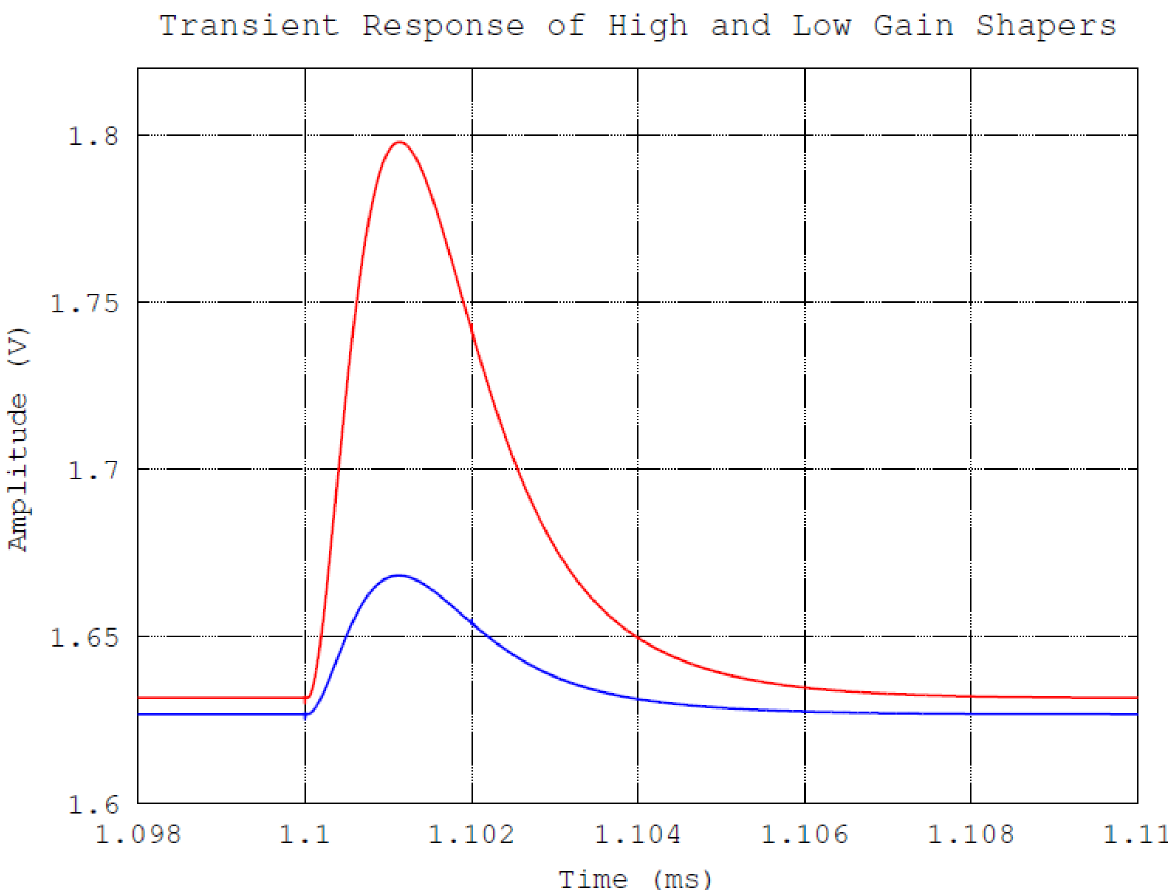
DDF (Delayed Dissipative Feedback) Configuration

- Delays the resistive feedback from the furthest node in a signal path



Shaper Transient Response and Noise Properties

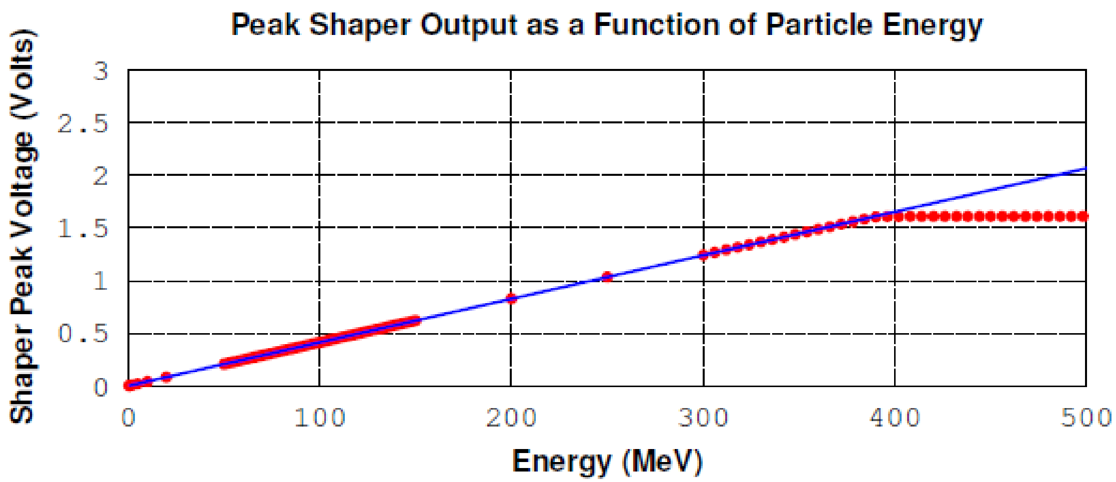
- High gain shaper outputs 4 times higher amplitude than the low gain shaper

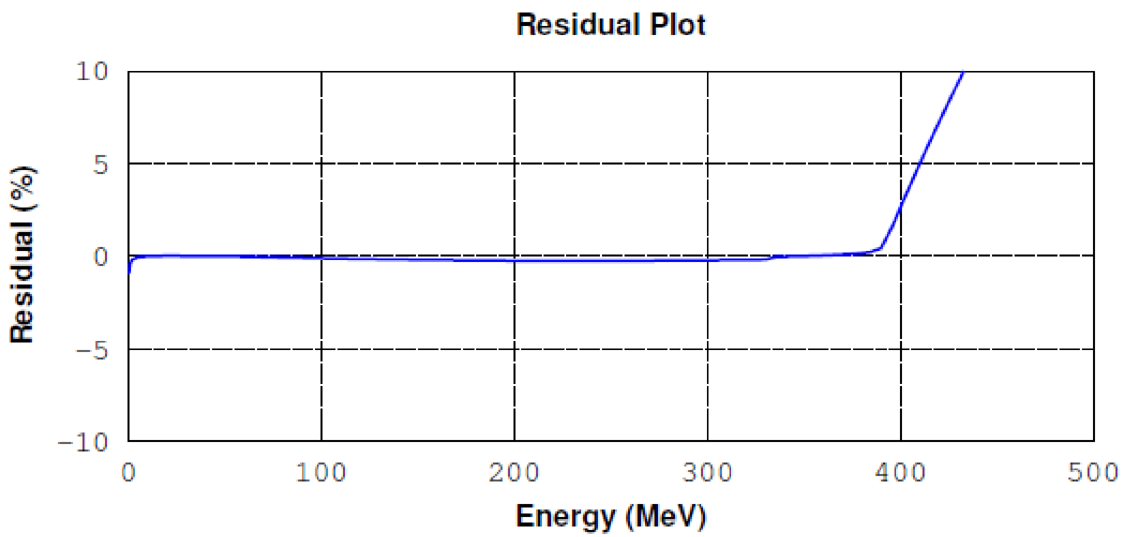


Device	Noise Type	Noise % of Total
Detector	Shot	42.51
Detector	Thermal	21.99
CA/M_0	Thermal	11.29
CA/M_8	Thermal	3.40
CA/M_6	Thermal	3.36

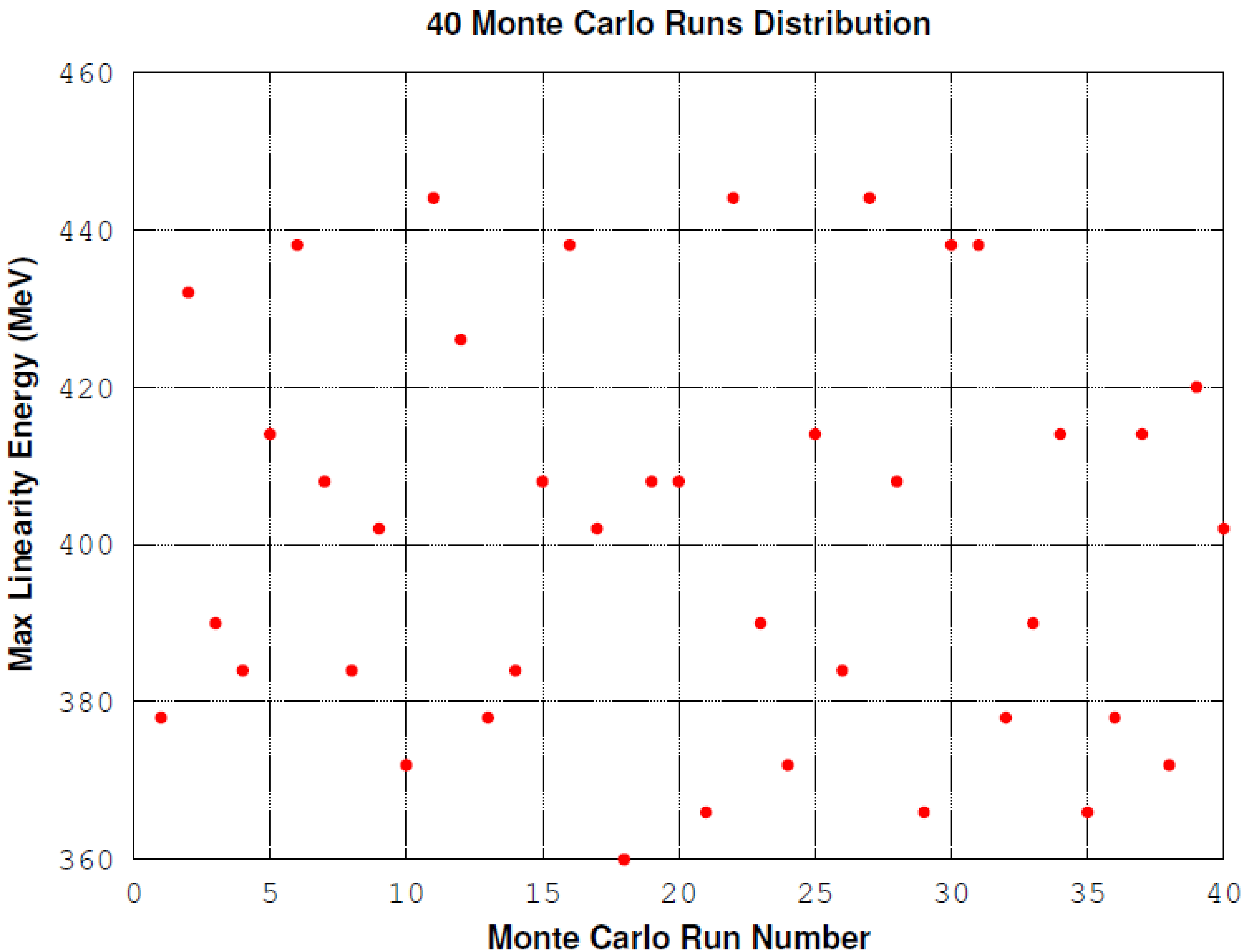
Total Equivalent Noise: 18 keV
(Detector Cap = 75pF)

Linearity Plots / Low Gain Shaper Output

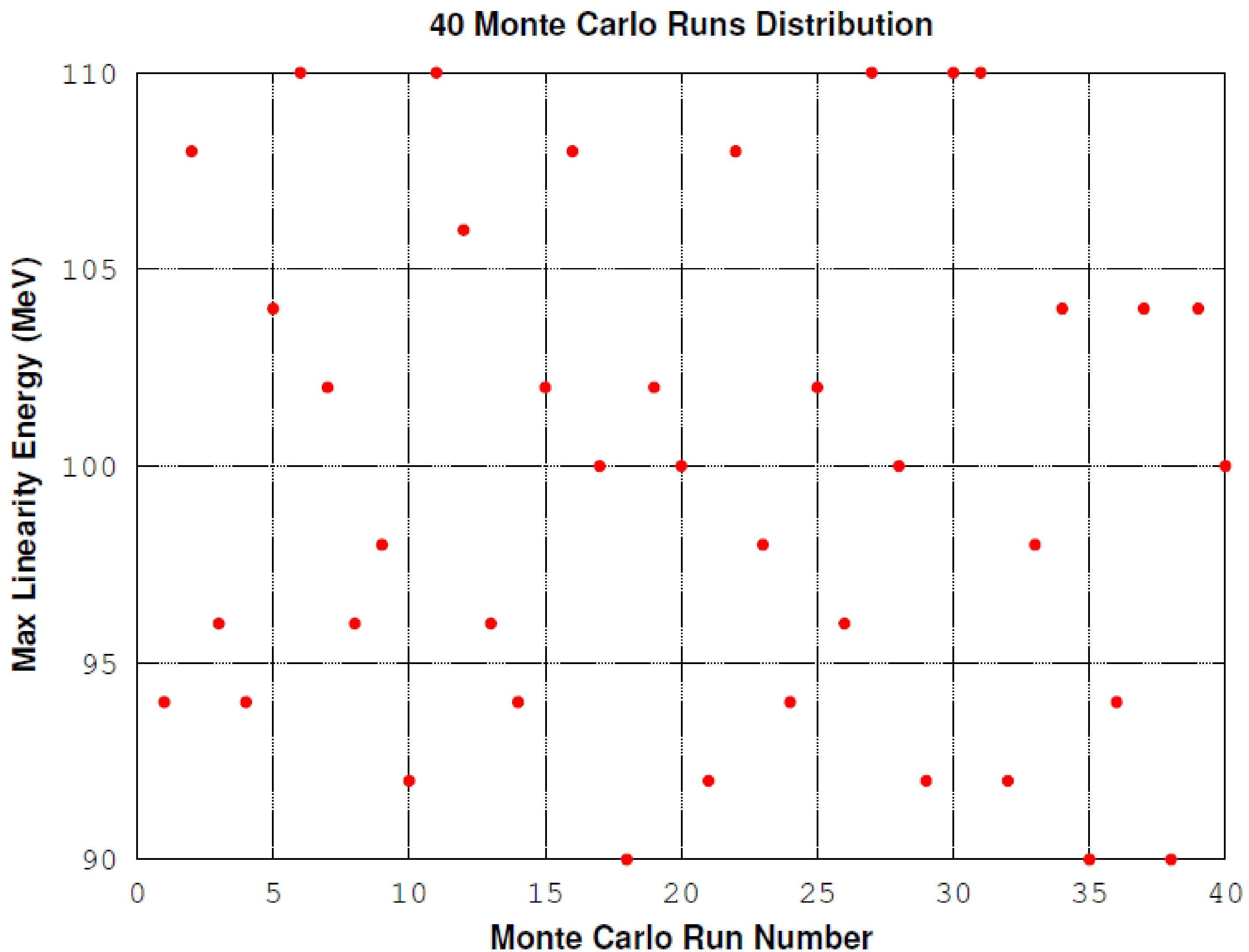




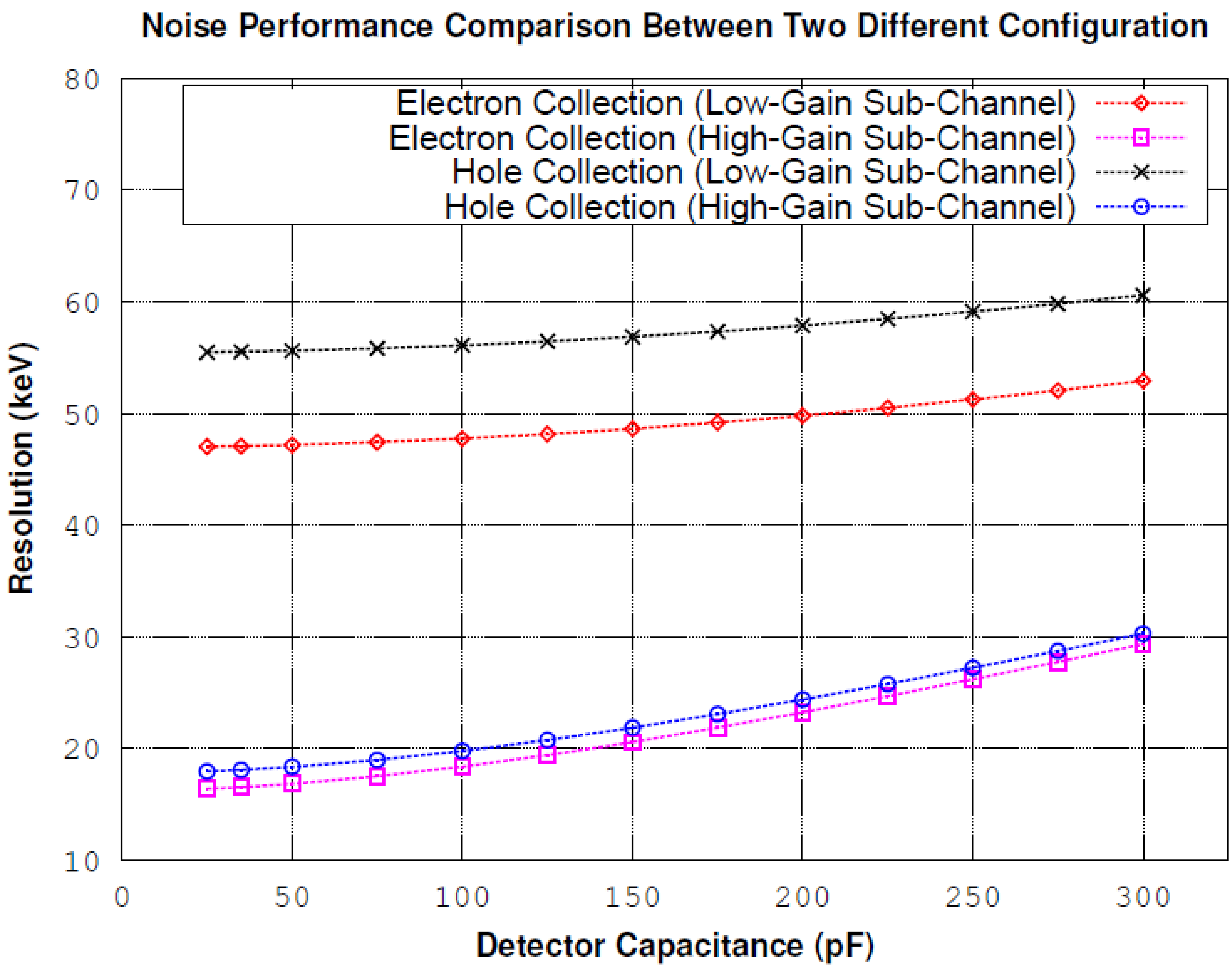
40 Monte Carlo Runs / Low Gain Shaper Output



40 Monte Carlo Runs / High Gain Shaper Output

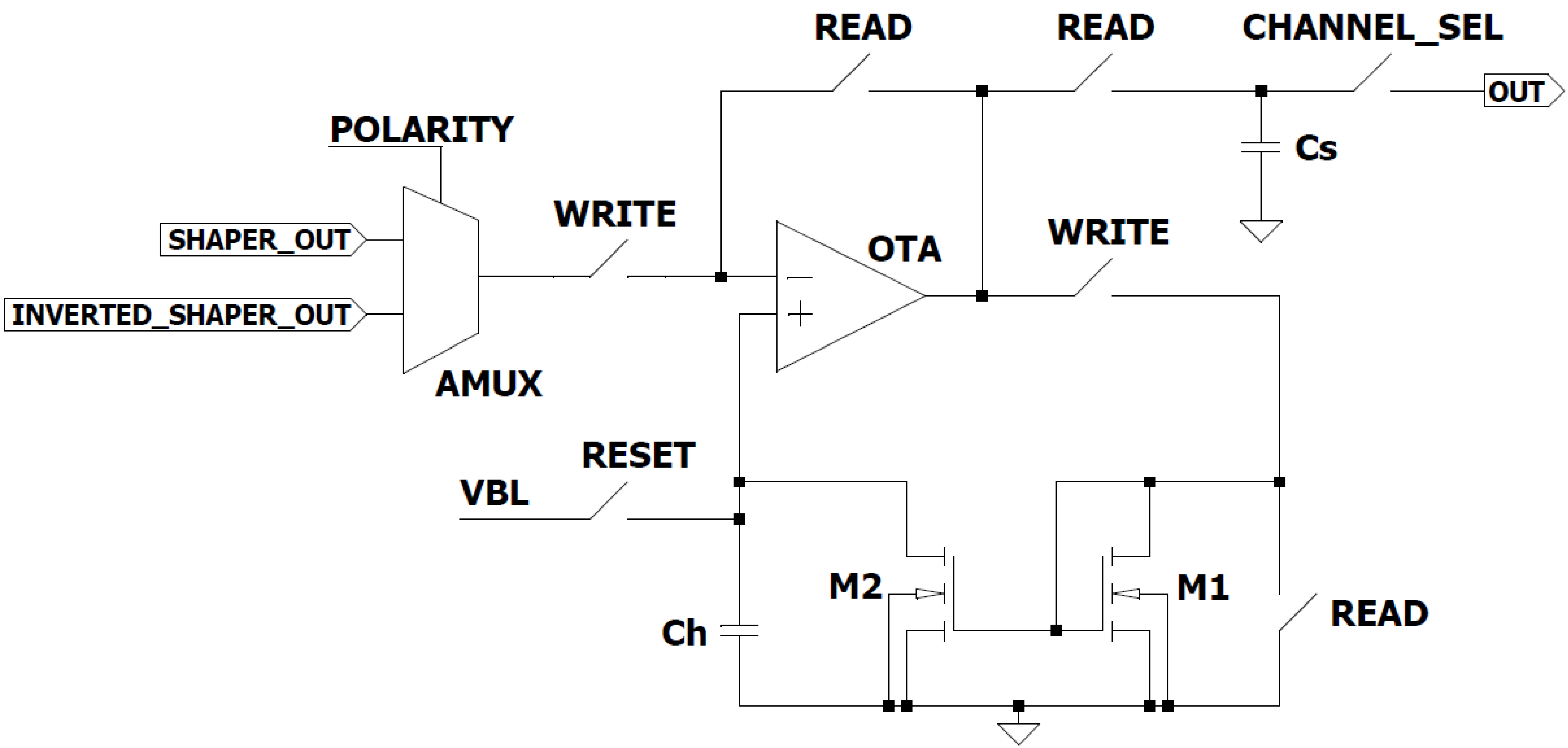


Energy Resolution

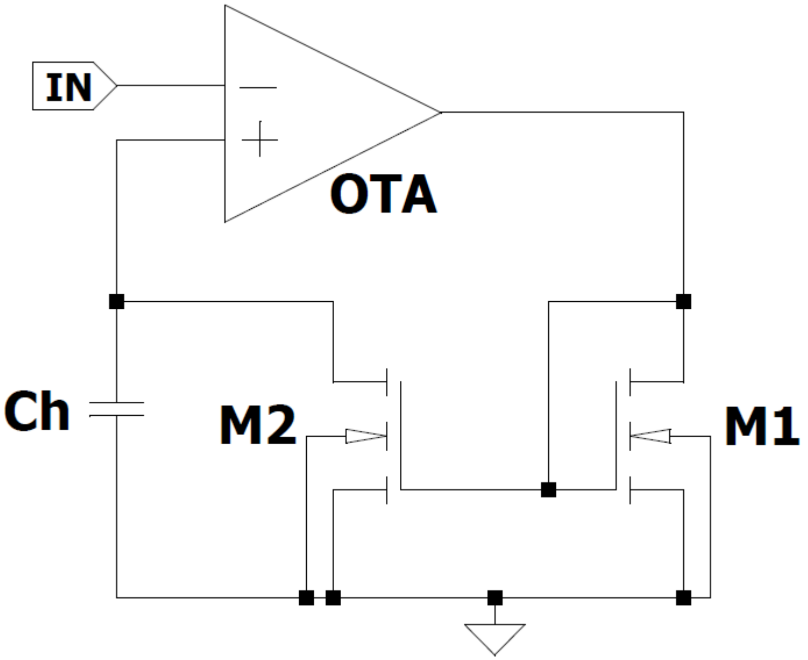


Peak Detector

- Detects negative peaks (Electron collection)
- Two phase peak detect-and-hold configuration
- CDS (Correlated Double Sampling to remove OTA offset voltage and 1/f noise.

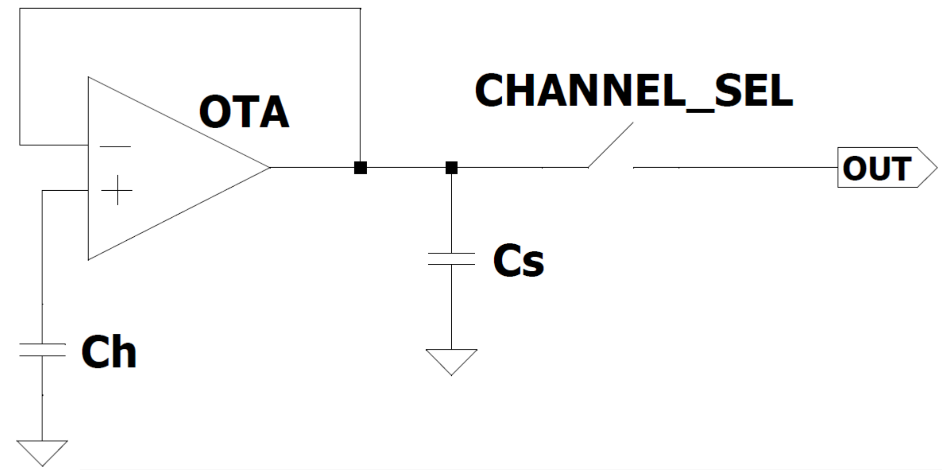


Write/Track Mode



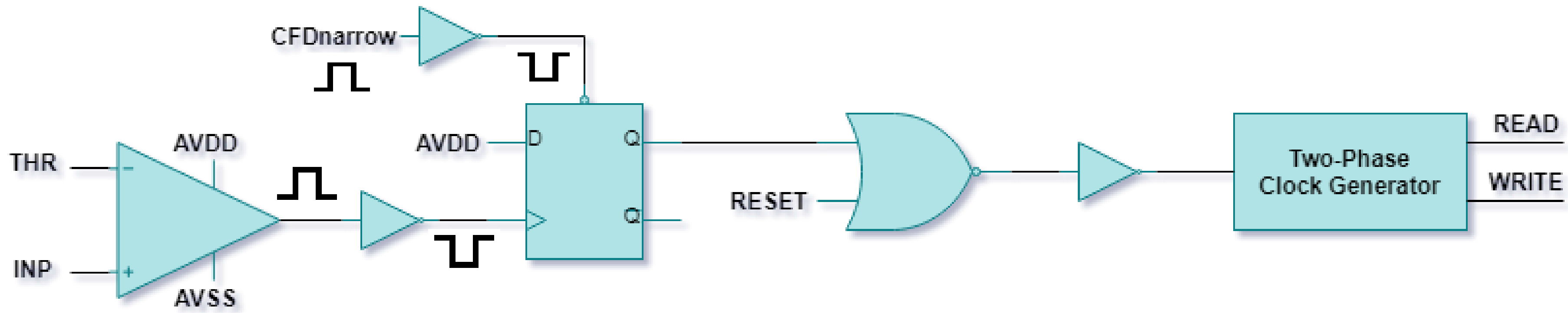
- Cap is being discharged to a value equilavent to peak amplitude.
- Peak value is stored in cap.
- Default cap value = 1.9 V

Read Mode

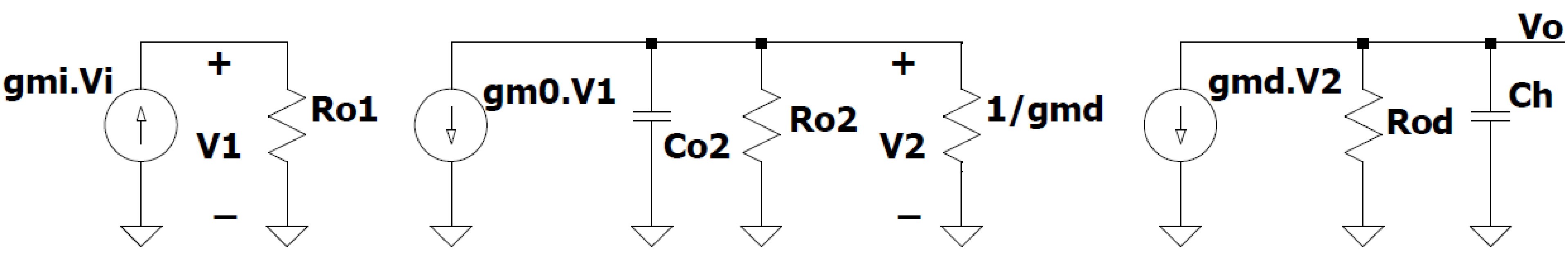


- The value stored in cap is being read by the output.
- Cs is a stabilization cap.
- Unity Gain Follower

Control Circuit



Small Signal Analysis



THANK YOU

ANY QUESTIONS ??