Multi-Channel Integrated Circuits For Use In Research With Radioactive Ion Beams

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Abstract. The Integrated Circuits Design Research Laboratory at Southern Illinois University Edwardsville (SIUE) has been collaborating over the past several years with the Nuclear Reactions Group at Washington University (WU) on the development of a family of custom, multi-channel Integrated Circuits (ICs). To date, the collaboration has successfully produced two micro-chips. The first was an analog shaped and peak sensing chip known as HINP16C (Heavy Ion Nuclear Physics – 16 Channel). The second chip, christened PSD8C (Pulse Shape Discrimination – 8 Channel), was designed to logically complement (in terms of detector types) the HINP16C chip. The HINP16C chip, for use with solid-state detectors, produces sparsified analog pulse trains for both linear (pulse height) and timing (relative to an external reference) signals. A shaper and peak detector are implemented in the linear branch, and a pseudo Constant-Fraction Discriminator (CFD) and Time-to-Voltage Converter (TVC) are implemented in the logic/timing branch. The internal and external gain options make the chip suitable for use in a wide variety of applications. PSD8C greatly simplifies the pulse-processing electronics needed for large arrays of scintillation detectors. As the PSD8C employs user-controlled, multi-region charge integration, particle identification is inherent in the design. Each of the three pulse-height sub-channels consists of a gated integrator with eight programmable charging rates and an externally programmable gate generator that defines the start (with 4 time ranges) and the width (with 4 time ranges) of the gate, relative to an external discriminator signal. Moreover, each channel on the chip also contains a TVC. This paper describes the design, capabilities, and features of the HINP16C and PSD8C ICs along with a description of how the chips are being used. It also discusses modifications and enhancements which have been made to both chips and their associated prototypical systems in order to improve ease of use and increase performance.

Keywords: integrated circuit, pulse shape discrimination, analog signal processing, Si strip detectors
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INTRODUCTION

The Nuclear Reactions Group at WU and the Integrated Circuits Design Research Laboratory at SIUE have been working over the past decade on a family of multi-channel custom integrated circuits (ICs) for use in research with radioactive ion beams. The group's first success was an analog shaped and peak sensing chip. This IC, known as HINP16C (Heavy-Ion Nuclear Physics – 16 Channel) [1] is designed for use with arrays of Si-strip detectors with a few hundred to a few thousand channels. The second chip, christened PSD8C (Pulse Shape Discrimination – 8 Channel) [2], performs Pulse-Shape Discrimination (PSD), and thus particle identification, if the time dependence of the light output of the scintillator depends on particle type. Moreover, both chips use almost all of the same supporting hardware and both ICs were fabricated in the ON-Semiconductor (formerly AMI) 0.5 μm n-well process (C5N), available through MOSIS (see www.mosis.com).

ANALOG SHAPED AND PEAK SENSING IC

The architecture of the HINP16C chip is illustrated in Fig. 1. The basic architecture has remained virtually unchanged throughout the course of several design revisions. The first generation HINP16C chip is described in detail in [1]. HINP16C produces sparsified pulse trains for both linear (pulse height) and timing (relative to an external reference). A shaper and peak detector are implemented in the linear branch, and a Constant-Fraction Discriminator (CFD)

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and Time-to-Voltage Converter (TVC) is implemented in the logic/timing branch. Two internal Charge Sensitive Amplifier (CSA) gain options and an external gain option along with the preparation of both pulse height and timing pulse trains with synchronized addresses (suitable for pipelined ADCs) make the chip suitable for a wide variety of applications. The pulse-height and the relative time are all stored on capacitors and are either reset (by the auto-reset circuits depicted in Fig. 1), after a user controlled time, or sequentially read out if acquisition of the event is desired.

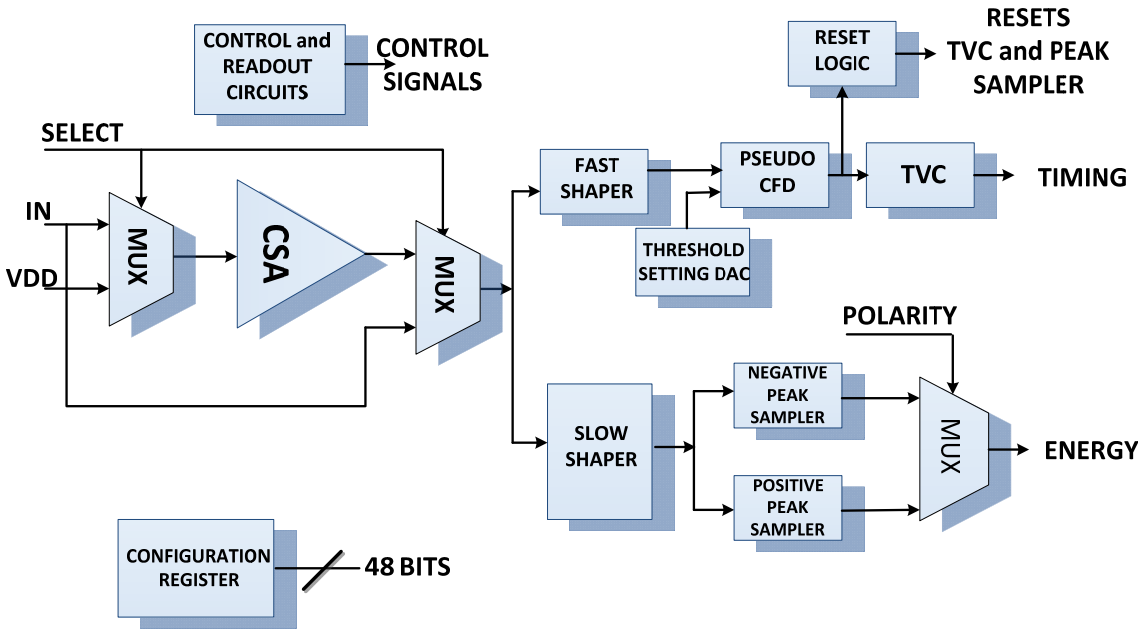

FIGURE 1. HINP16C Block Diagram.

The current version of HINP16C is 4 mm x 6.4 mm and is packaged in a 14 x 14 mm, 128 lead, thin quad flat pack. Power consumption is approximately 800 mW, and the cost per channel of the ASIC varies from $15 - $25 depending on the quantity ordered. Important features of HINP16C are summarized in Table 1.

Unfortunately, some changes made in order to improve the IC adversely impacted the performance of the aforementioned auto-reset circuit. The newest version of HINP16C is expected to be ready for fabrication in late 2010. In this upcoming version of HINP16C, problems with the auto-reset circuit will be fixed. Moreover, we plan to modify the existing CSA circuit (see Fig. 2) so as to include a single CSA gain (*high-gain*, 0.5 mV/fC), but the circuit may be programmed to include a diode-connected FET in the feedback path which will extend the dynamic range of this mode to approximately 400 MeV. This extension of range is needed for heavy-ion break-up experiments, conducted at hundreds of MeV per nucleon, when heavy ion residues, as well as light ions, hit the same detector. (The heavy-ions can drop 100's of MeV in a 300 µm Si while protons will drop less than a MeV). Simulation results demonstrating the CSA's extended dynamic range (electron collection) are presented in Fig. 3. Similar results were obtained when holes were collected.

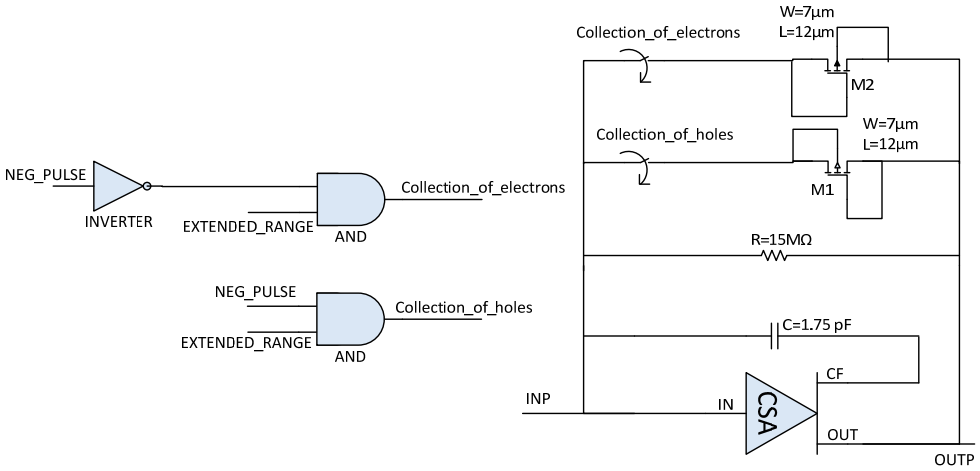

FIGURE 2. HINP16C (Rev. 4) CSA circuit with extended dynamic range.

PSD-ENABLING IC

Our PSD8C chip greatly simplifies the pulse-processing electronics needed for large arrays of scintillation detectors. The structure of a single PSD8C sub-channel is illustrated in Fig. 4. Each of the chip's 8 channels possesses 3 sub-channels. The sub-channels are referred to as A, B, and C. A sub-channel consists of an integrator and a gate generator. External control voltages (D_X, W_X where x = A, B, C) determine the gate delay and gate width. Because PSD8C employs (user-controlled) multi-region charge integration, particle identification is incorporated into the basic design. Each channel on the chip also contains a TVC which provides relative time information. The pulse-height integrals and the relative time are all stored on capacitors and are either reset, after a user controlled time, or sequentially read out if acquisition of the event is desired in a manner similar to that of HINP16C.

PSD8C is described in detail in [2]. The IC is 2.25 mm x 5.7 mm and is packaged in a 14 x 14 mm, 128 lead thin quad flat pack. Power consumption is 60 mW (low-bias mode) or 135 mW (high-bias mode). The cost per channel is $25. Key features of the design are summarized in Table 2.

A second version of PSD8C was submitted for fabrication in May 2010. This version attempts to correct several minor problems identified (over the past year or so) during testing of the PSD8C IC. First, it was found that the TVC circuits could inadvertently be re-started. This logic error has been fixed.

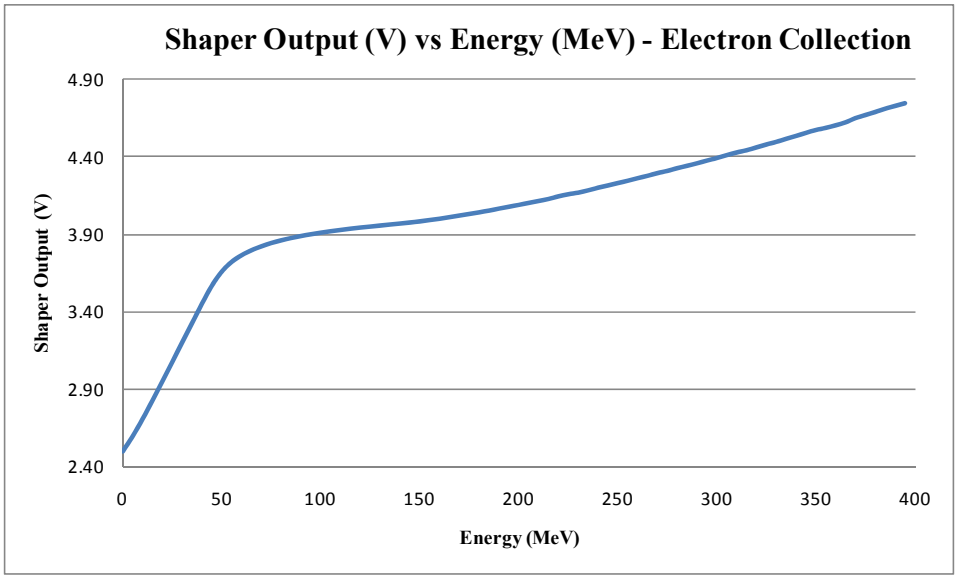

FIGURE 3. Simulation demonstrating CSA's extended dynamic range.

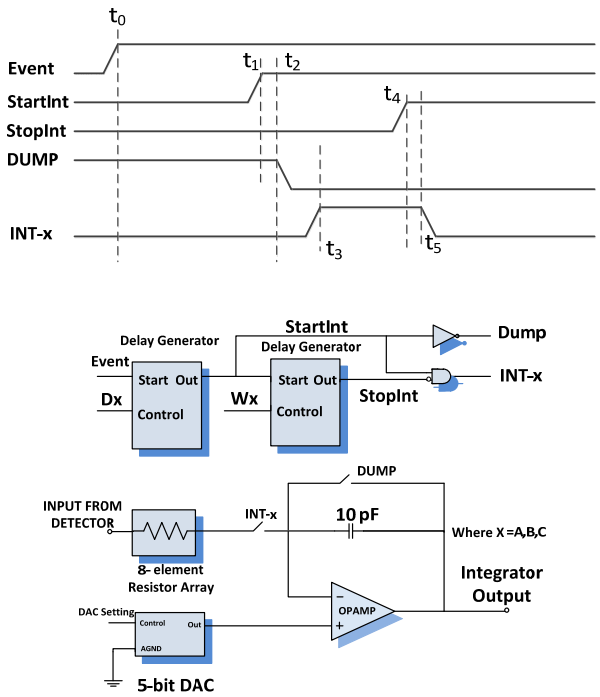

FIGURE 4. Each channel contains 3 sub-channels referred to in the text as sub-channels A, B and C. Here we show a representative sub-channel, X, where X is A, B or C

Second, undesirable temperature dependence (1 ns / C) in the TVC circuit was noted and traced to the local channel buffer. The buffer was re-designed, and the TVC temperature sensitivity has been greatly reduced (5 ps/C in the 500 ns mode, 40 ps/C in the 2 µs mode). Third, some TVC crosstalk issues were remedied.

Finally, at the system level, the chip-boards (printed-circuit boards) are being redesigned to include on-board ADCs (one for each of the chip's four analog output pulse trains). In the future, data will be transmitted in a digital format to the motherboard. This change will potentially reduce the time required for readout (since data from all chips in the system would be read out in parallel), make the IC easier to use, and improve performance since digital data is less susceptible to environmental noise than are low-level analog signals.

WHO IS USING THE ICs?

Nuclear Physics groups at Washington University (WU), Michigan State University (MSU), Indiana University (IU), Texas A&M University (TAMU), Oak Ridge National Laboratory (ORNL), Louisiana State University (LSU), and Florida State University (FSU) are either using HINP16C or will be doing so by summer of 2010.

The most productive use of the original HINP16C chip to date has been for the study of high-order multi-particle correlations in the study of the continuum structure of light nuclei. These works include the study of ^{6}Be [3, 4], ^{10}C [5, 6, 7], ^{12}Be and other light neutron-rich nuclei [8, 9]. However it has also been used for the study of nucleon knock-out from secondary beams [10] and for transfer reactions on both light and heavy Ar isotopes, also with secondary beams [11]. The current version of the HINP16C chip was used for a 5-particle correlation study of the decay of ^{8}C (into an alpha and 4 protons) [12] and for a set of transfer reactions on heavier systems than in the initial transfer work.

A group at Los Alamos National Laboratory (LANL) has been helping to characterize the PSD8C's performance using several different scintillators [13]. Ongoing work at LANL is using this chip for both the very bright Lathinum-Halide scintillators, (e.g. $LaBr_3$(Ce)) and the new class of CLYC scintillators (e.g. Cs_2LiYCl_6(Ce)) [14]. In the former case, it is just the simplification offered by the chip in running large arrays which is utilized while in the second case, the pulse-shape discrimination offered by the chip is used (along with pulse height) to differentiate neutrons from gamma rays.

At Washington University In St. Louis, the group led by D. G. Sarantites is planning on using this chip to provide the signal processing for a large array of scintillators using the fast plastic – CsI(Tl) phoswich concept employed by the ``Dwarf Ball and Wall'' device [15]. Light charged particles (p,d,t,^{3}He, ^{4}He, ^{6}He) are identified using the time dependence of the light output of the CsI(Tl) while the atomic number of elements with Z<8 are identified from the light partition between the fast plastic and the CsI(Tl). The latter concept is similar to that employed in standard dE-E telescopes. This application makes use of all three integration windows: one (prompt and narrow) for the fast plastic and two (delayed – to different extents) for the CsI(Tl). The device being built, unlike the Dwarf project, makes use of multi-element PMT's, have a position resolution of close to 1 mm, and will be designed to study heavy-ion transfer reactions using secondary beams.

SUMMARY

Since 2001, our university-based group has been working on the development of a "toolbox" of IC circuits useful for researchers working with radioactive ion beams. The circuits which we have designed can be composed in different ways to meet the researchers' evolving needs and desires. To date, the group has produced two micro-chips: one analog

shaped and peak sensing (HINP16C) while the other multi-sampling and PSD-enabling (PSD8C). The ICs are currently being used by a growing number of researchers across the country and the world.

TABLE 1. HINP16C parameters.

Parameter	Value
Number of channels	16
Programmable	via 48-bit register
Data sparsification	yes
CSA gain modes	0.5 mV/fC (high-gain) 0.1mV/fC (low-gain) external preamp
CSA decay time constant	25 µs
Full scale range	100 MeV (high-gain mode) 500 MeV (low-gain mode)
Energy resolution (C_{det} = 75 pF)	high-gain mode: 28 keV low-gain mode: 42 keV
Polarities supported	holes and electron
Slow shaper peaking time	1.2 µs (fixed)
Slow shaper return to baseline	< 20 µs
Fast shaper time constants	250 ns 620 ns
Automatic channel reset	set by external voltage
Discriminators on chip	Nowlin CFDs
Threshold setting DAC	6 bits
Range of CFD threshold setting DAC	1 MeV (step size 35 keV)
TVC ranges (full-scale)	500 ns and 2 µsec
Walk through CFD	< 1 ns over range of 40 dB
Jitter	1 ns
Diagnostic modes	yes
Power consumption	800 mW
Supply voltage	5 VDC
Cost per channel	$15 -$25
Die area	4 mm x 6.4 mm
Package	128 lead, TQFP
Technology	0.5 micron CMOS

TABLE 2. PSD8C parameters.

Parameter	Value
Number of channels	8
Programmable	via 48 bit register
Data sparsification	yes
Polarities supported	+/-
Input/Output voltage range	+/- 2V rel. AGND
Automatic channel reset	yes
TVC ranges (full scale)	500 ns and 2 µsec
Triggering modes	3
Integration regions	3
Delay and integration width ranges	20 ns – 70 ns 50 ns - 300 ns 200 ns - 1.5 µs 1 µs - 10 µs
Integrator programmable charging rates (8)	500 Ω - 100 kΩ
Integrator offset canceling DAC	5 bits, +/- 25 mV FS
Diagnostic modes	yes
Power modes	2 (slow/fast scintillators)
Power consumption	60 mW (low-power) 135 mW (high-power)
Supply voltage	5 VDC
Cost per channel	$25
Die area	2.25 mm x 5.7 mm
Package	128 lead, TQFP
Technology	0.5 micron CMOS

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