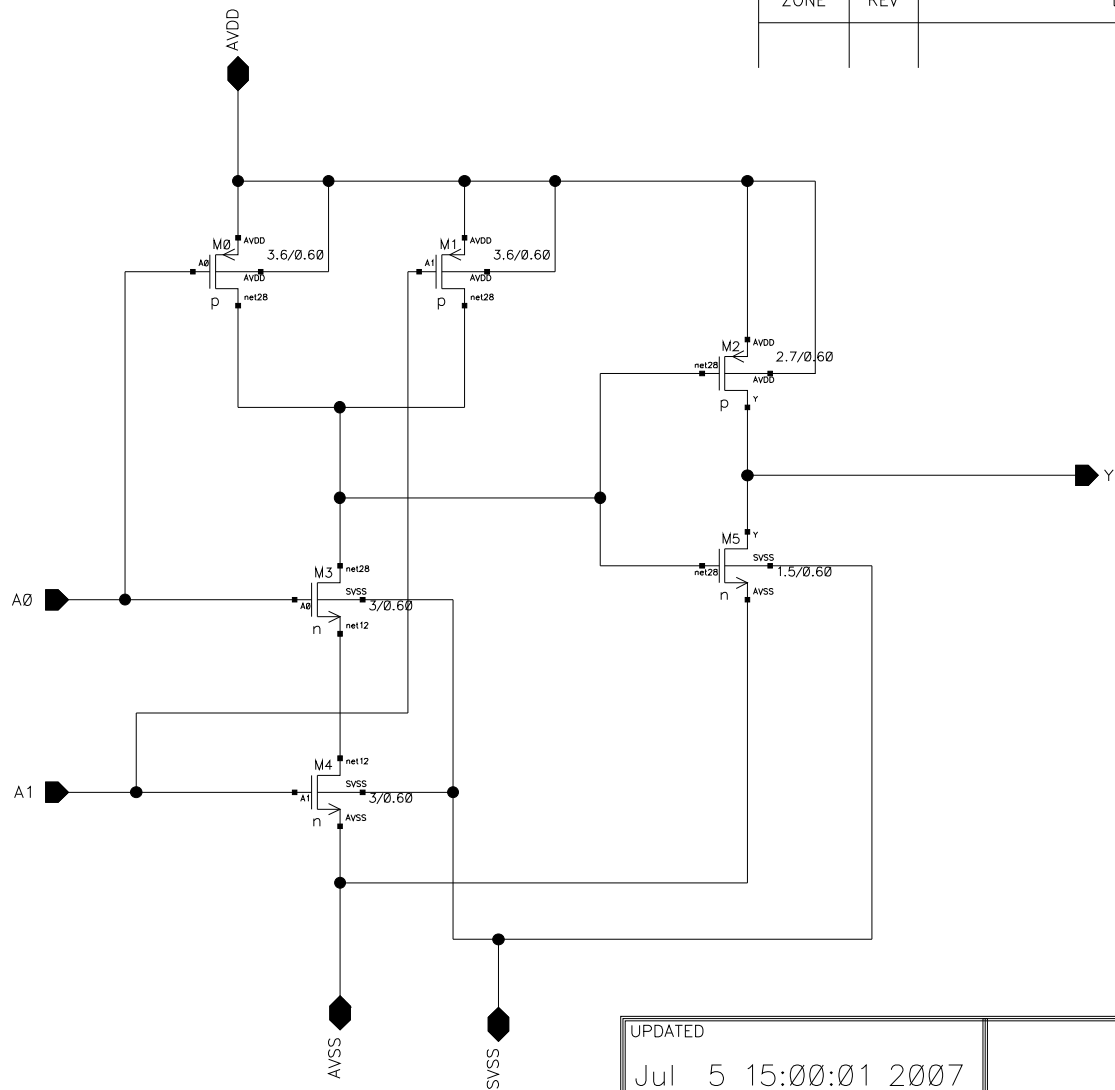
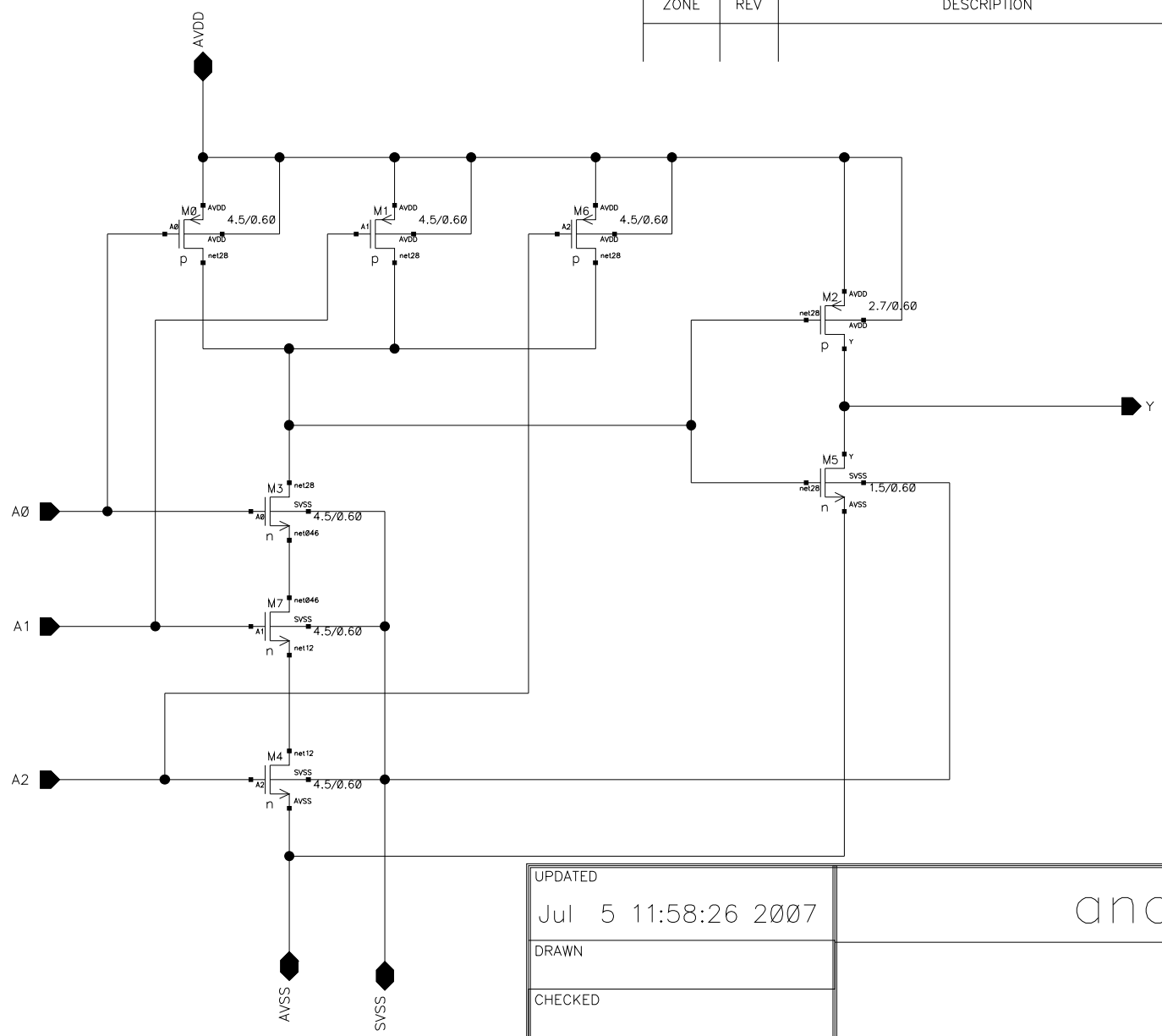


		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	and				
Jul 5 15:00:01 2007					
DRAWN					
CHECKED	SIZE A				
CHECKED					
ISSUED					
	CAGE NO.	DWG NO.		REV	
				SHEET 1 OF 1	

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	and03			
Jul 5 11:58:26 2007				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

		CAGE NO.	DWG NO.		SH 1	REV
		REVISIONS				
ZONE	REV	DESCRIPTION			DATE	APPROVED

A0

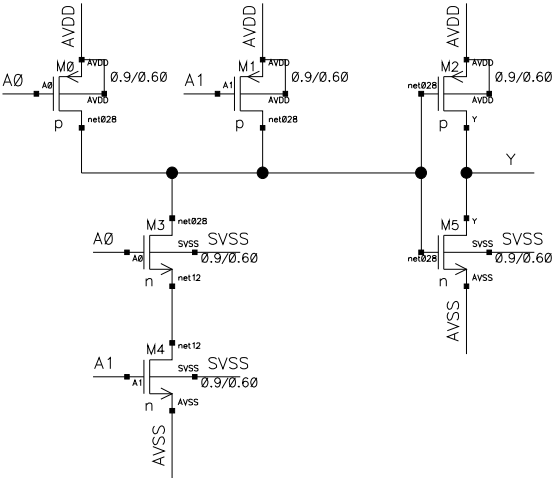
A1

AVDD

AVSS

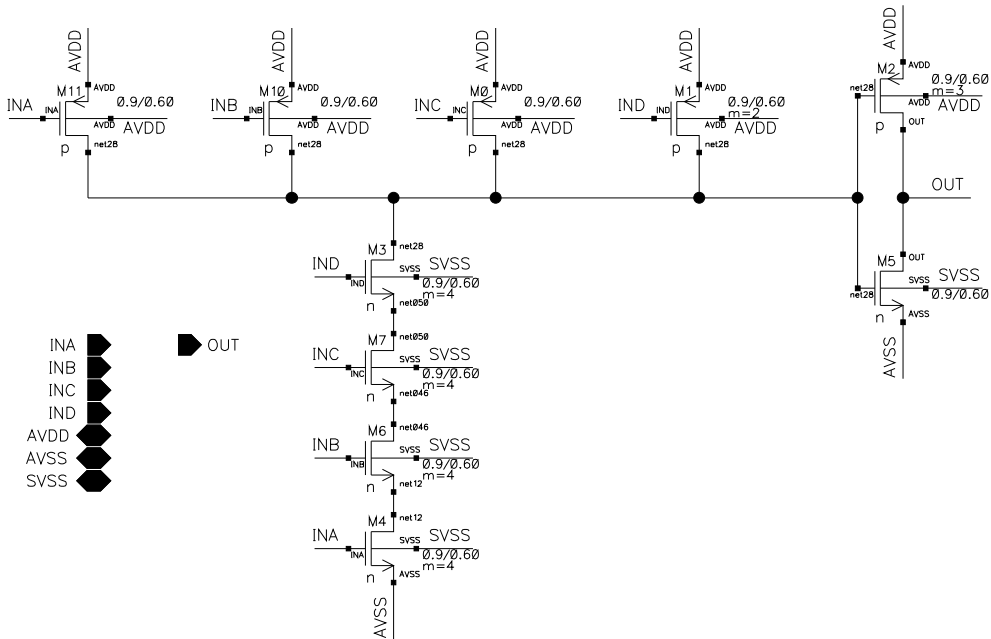
SVSS

Y



UPDATED	and				
Aug 8 14:14:18 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	A				
	SCALE			SHEET	1 OF 1

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



INA

INB

INC

IND

AVDD

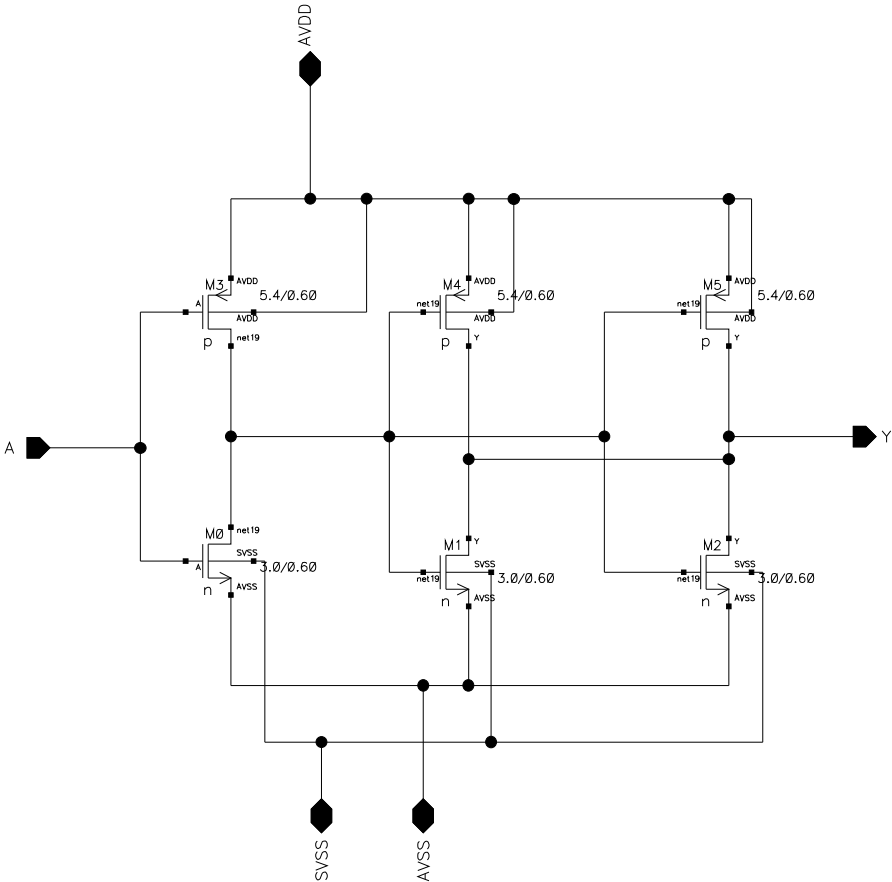
AVSS

SVSS

OUT

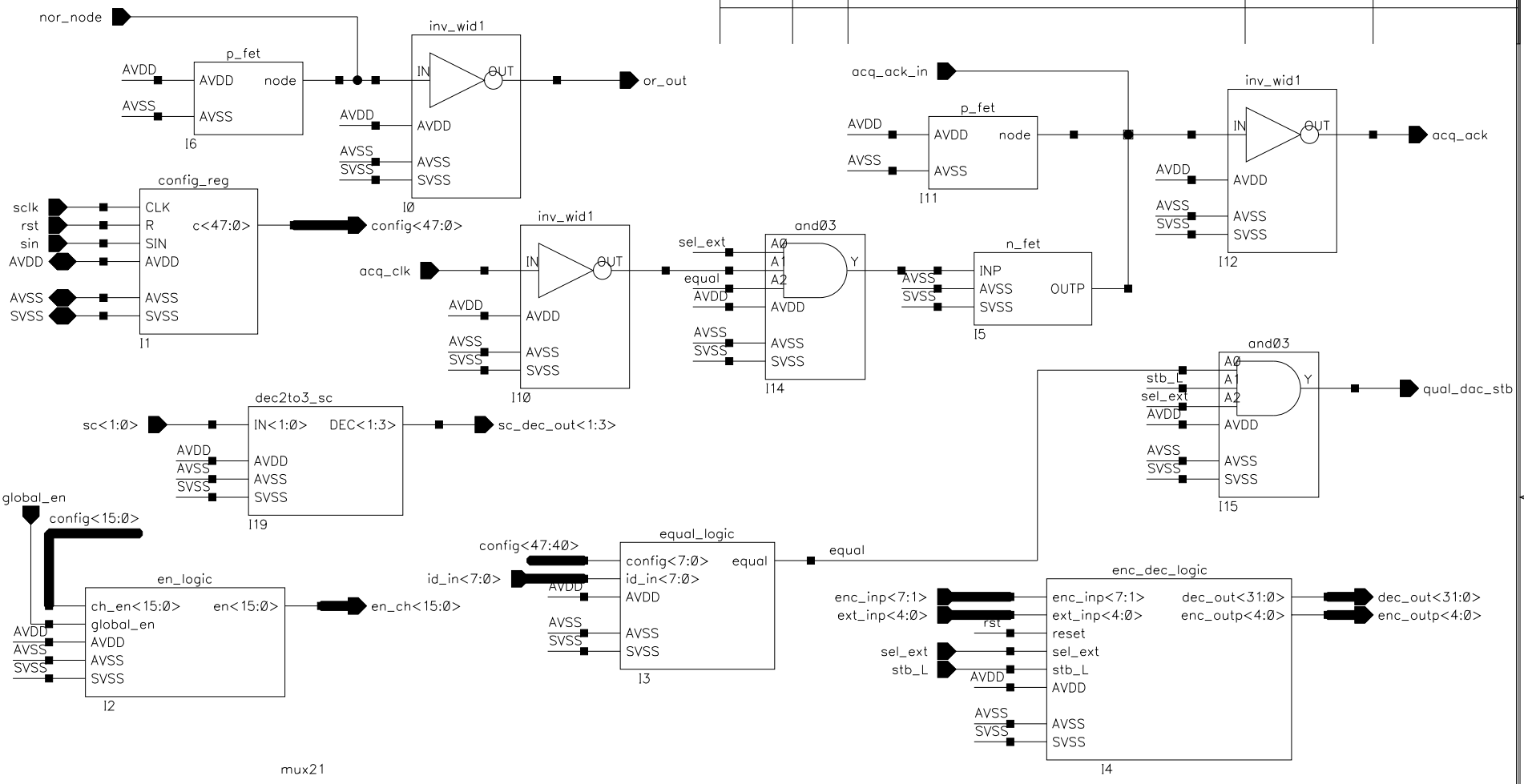
UPDATED	and				
Feb 20 16:35:34 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	A				
	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



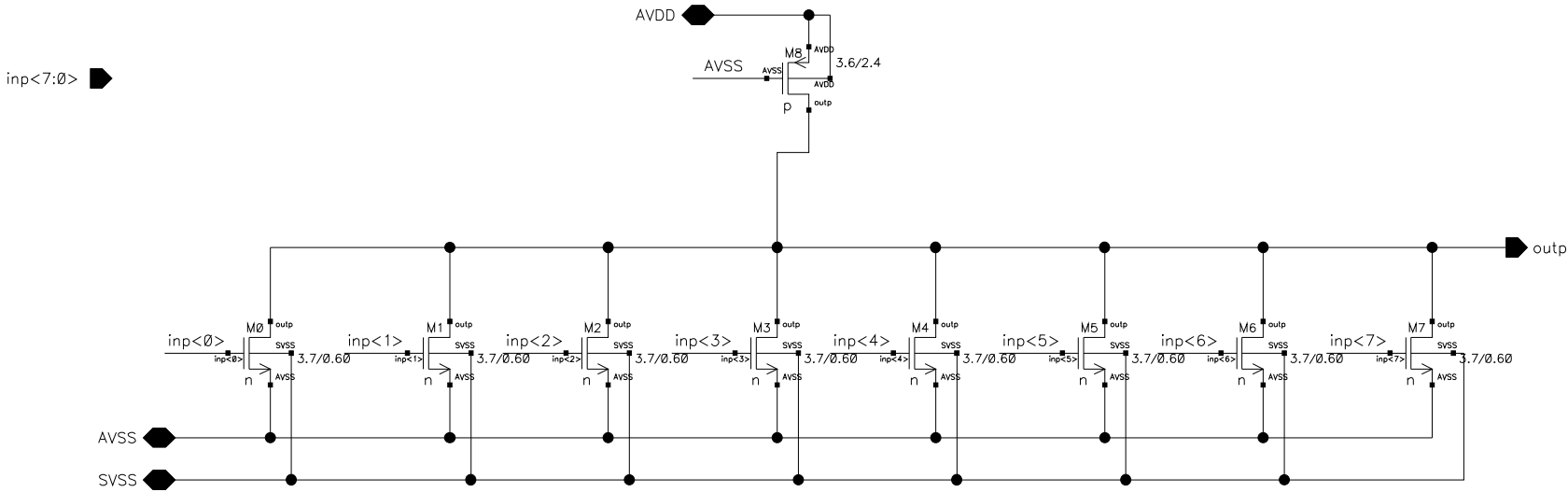
UPDATED		buffer_4			
Jun 15 14:49:33 2007					
DRAWN					
CHECKED					
CHECKED		SIZE	CAGE NO.	DWG NO.	REV
ISSUED		A			
		SCALE		SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



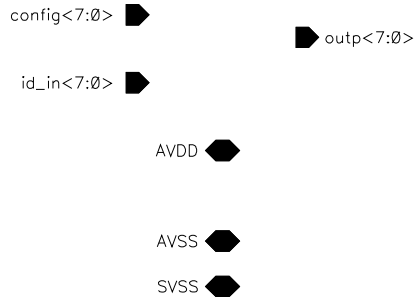
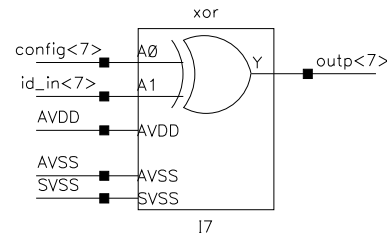
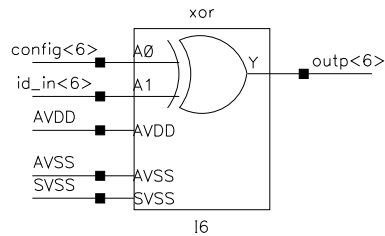
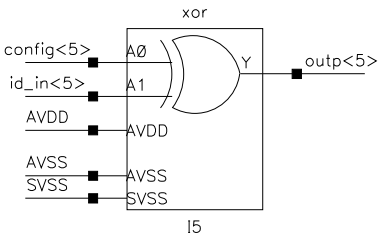
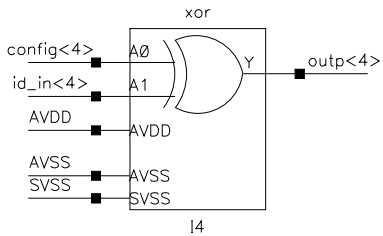
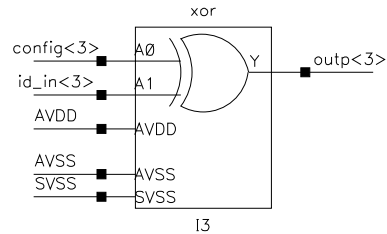
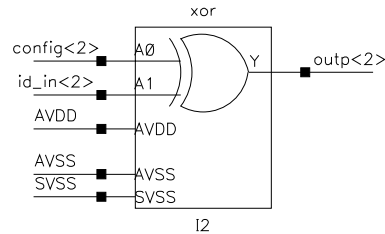
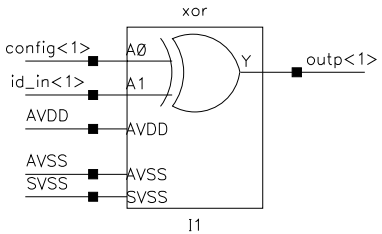
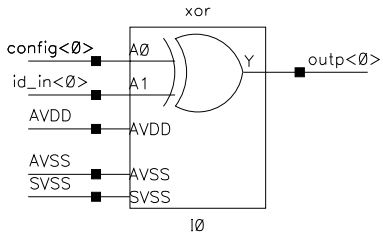
UPDATED		common_digital			
Mar 16 11:29:10 2010					
DRAWN					
CHECKED					
CHECKED					
ISSUED		SIZE	CAGE NO.	DWG NO.	REV
		A			
		SCALE			SHEET 1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	comp_nor			
Jul 6 10:56:07 2007				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



UPDATED		comparator			
Jul 9 14:04:08 2007					
DRAWN					
CHECKED					
CHECKED					
CHECKED					
ISSUED		SIZE	CAGE NO.	DWG NO.	REV
		A			
		SCALE			SHEET 1 OF 1

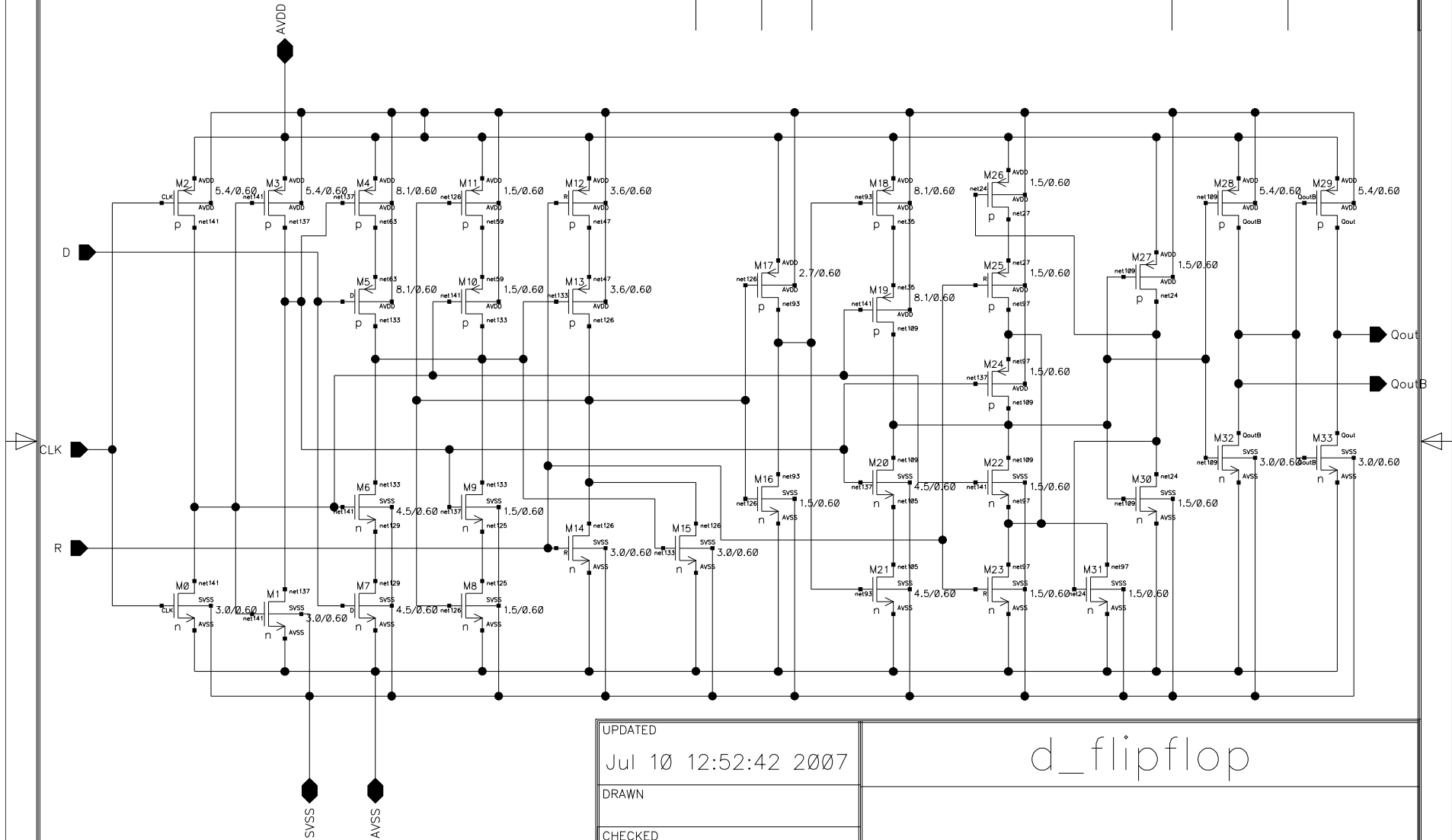
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jan 25 14:13:00 2008		config_reg		
DRAWN				
CHECKED				
CHECKED	SIZE C	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

CAGE NO. DWG NO. 1 REV

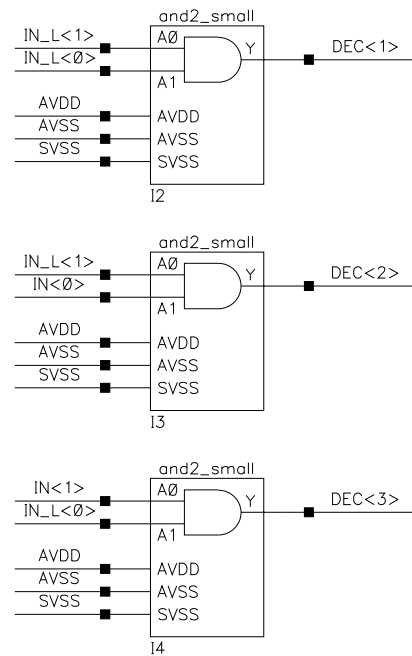
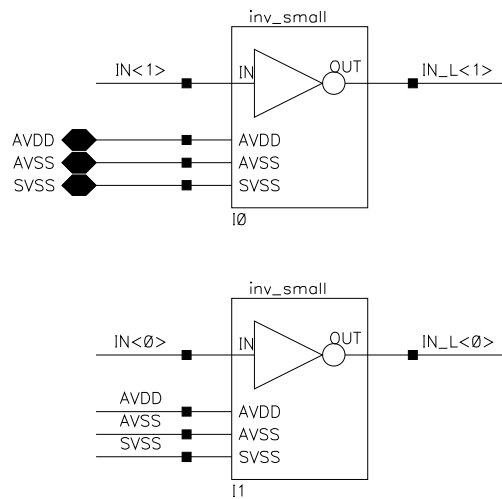
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jul 10 12:52:42 2007	d_flipflop			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

	CAGE NO.		DWG NO.		SH 1	REV A
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	

IN<1:0> DEC<1:3>



UPDATED	SIUE IC Design Lab Decoder 2 to 3 Subchannel Selects				
Sep 5 11:36:39 2007					
DRAWN					
CHECKED					
CHECKED					
ISSUED	SIZE A	CAGE NO.	DWG NO.	REV A	
SCALE		SHEET 1 OF 1			

4

3

2

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

D

D

C

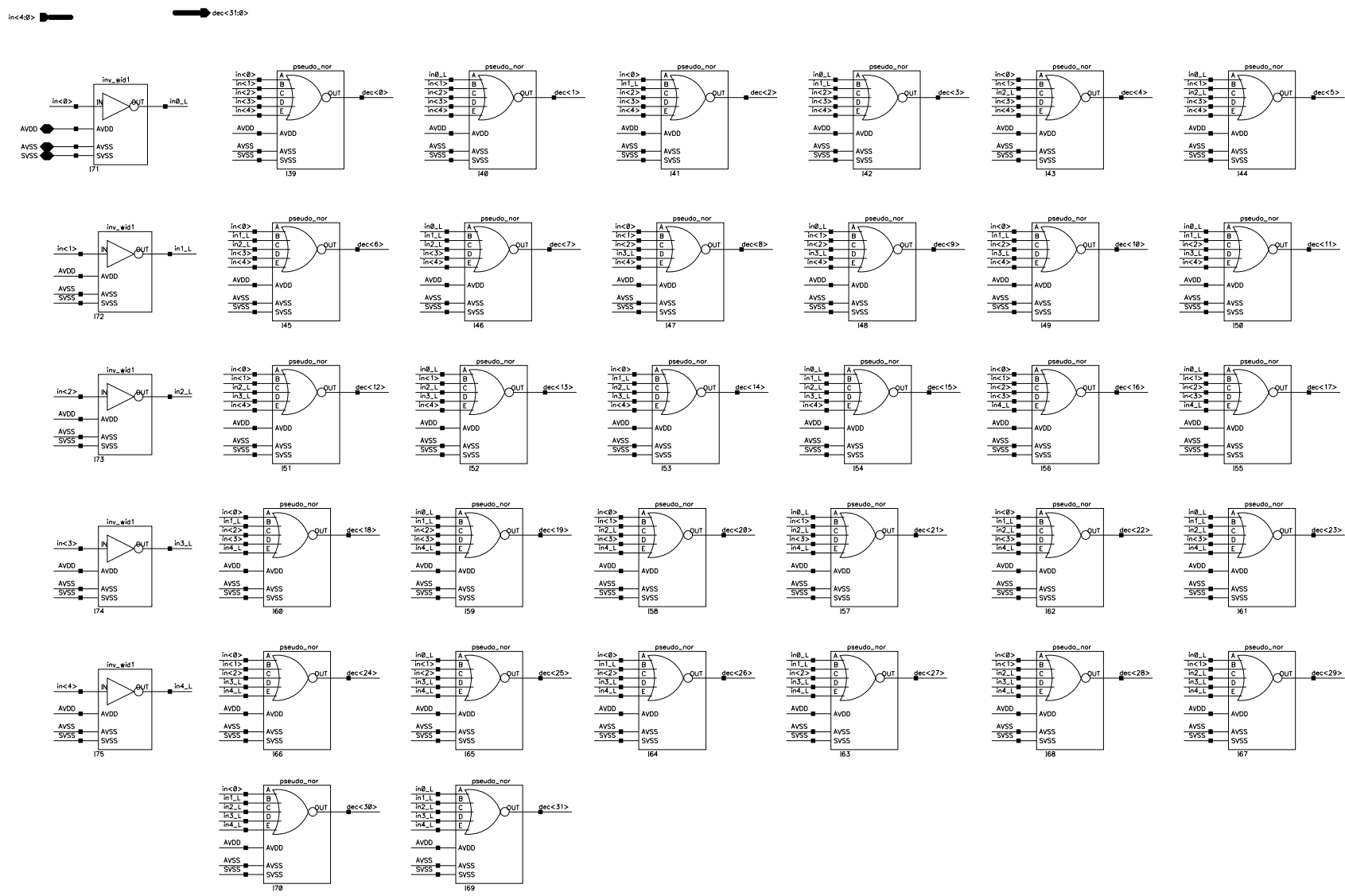
C

B

B

A

A



4

3

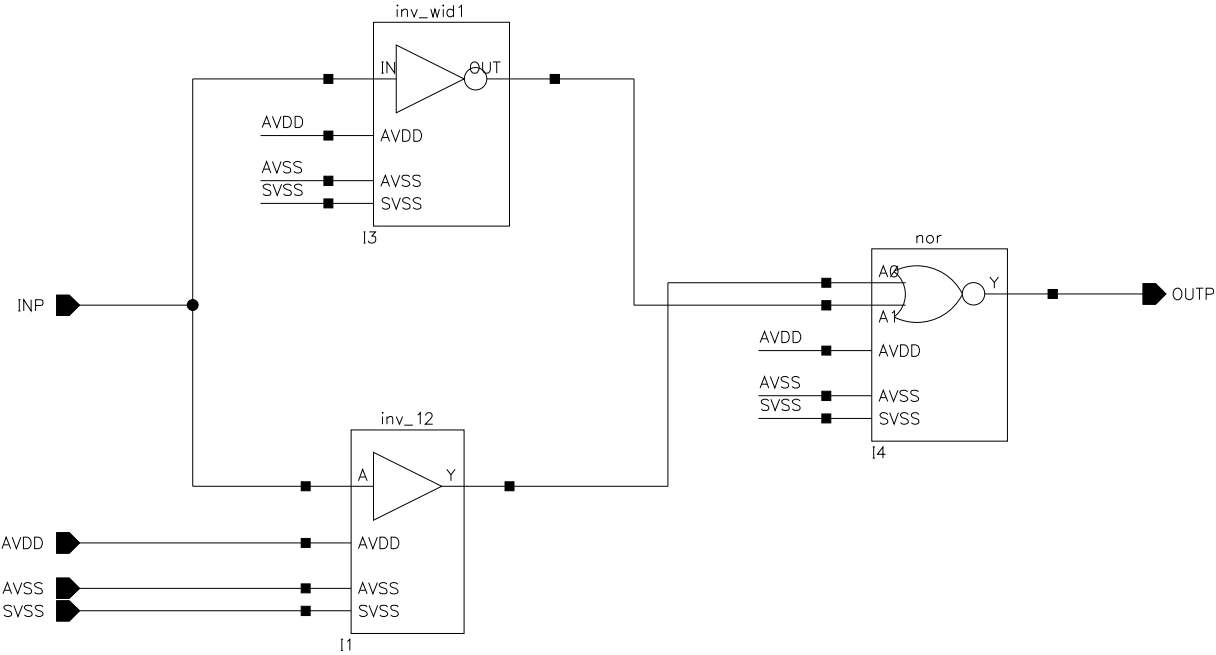
2

1

UPDATED Aug 1 12:15:27 2007		dec5to32		
DRAWN				
CHECKED				
CHECKED	SIZE C	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

CAGE NO. DWG NO. 1 REV

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED		edge_det_pos			
Mar 24 09:08:28 2010					
DRAWN					
CHECKED					
CHECKED		SIZE	CAGE NO.	DWG NO.	REV
ISSUED		A			
		SCALE		SHEET	1 OF 1

CAGE NO.

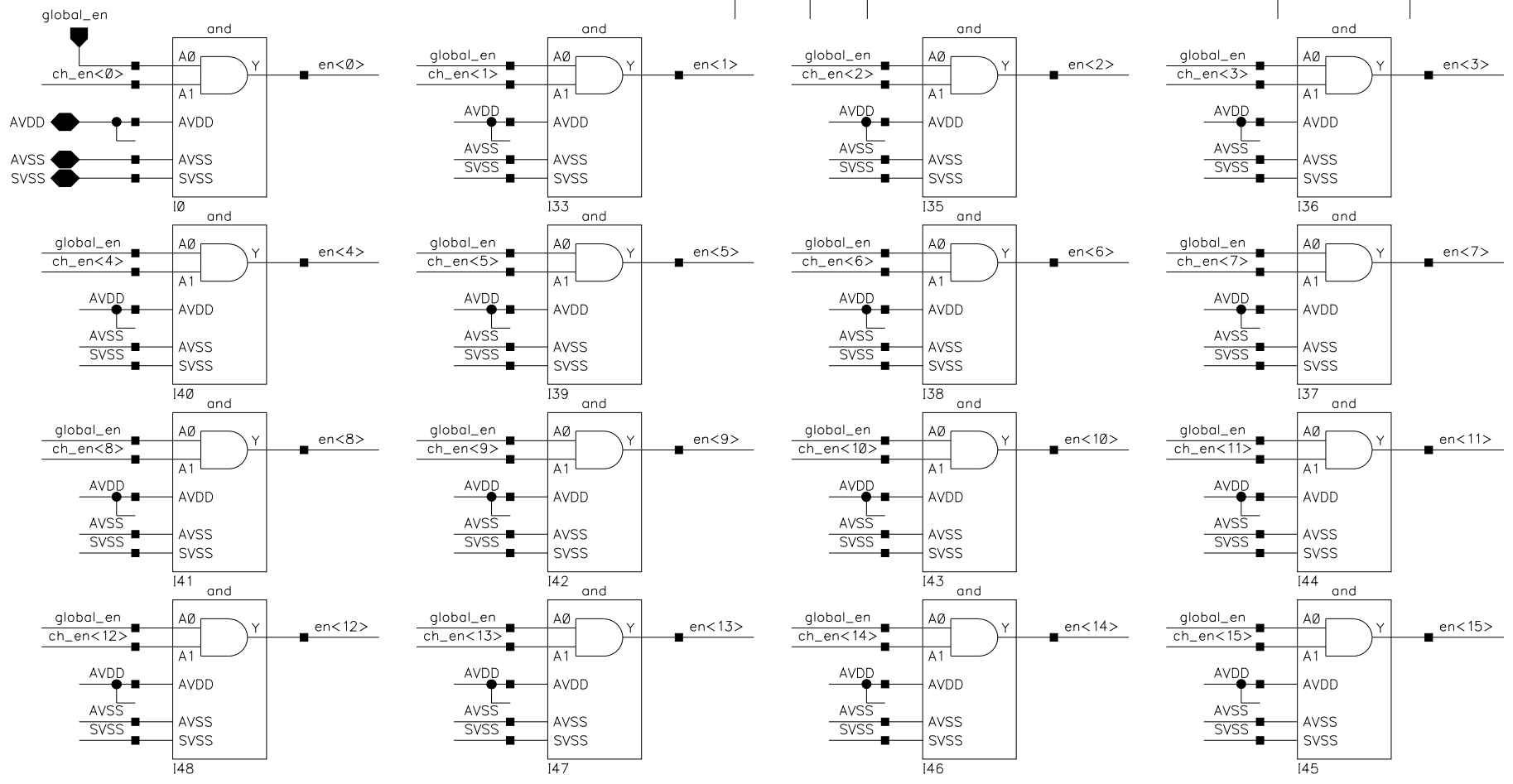
DWG NO.

SH 1

REV A

REVISIONS

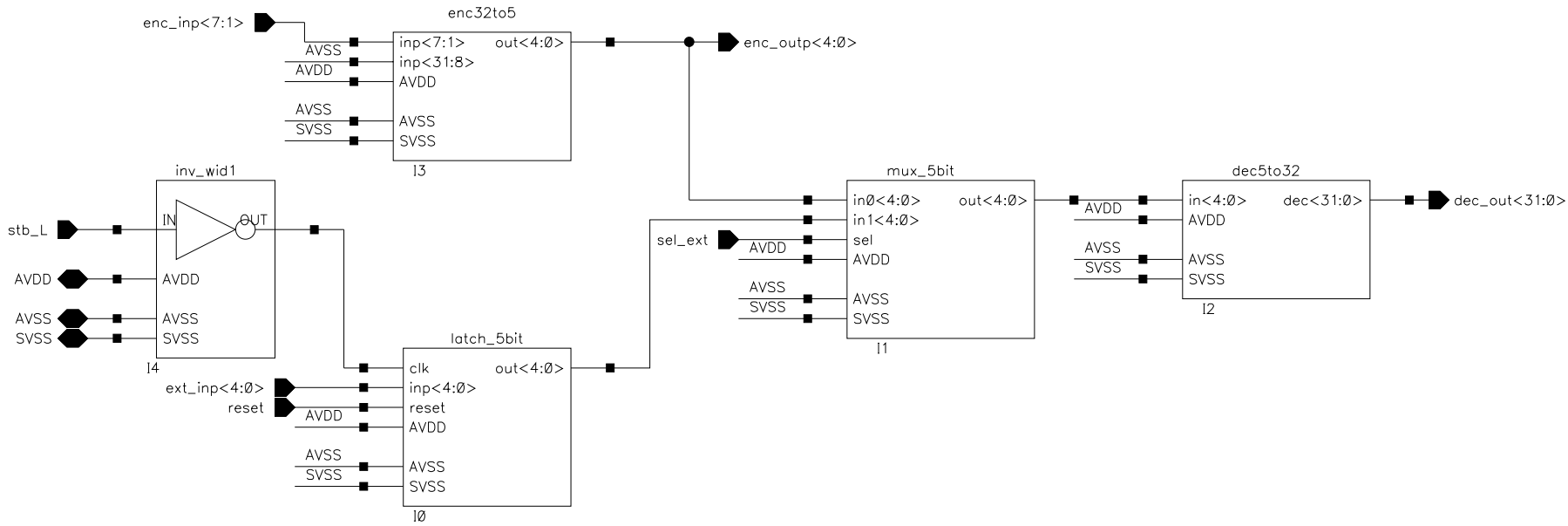
ZONE	REV	DESCRIPTION	DATE	APPROVED



ch_en<15:0> en<15:0>

UPDATED Jul 11 11:05:28 2007		SIUE IC Design Lab			
DRAWN		Enable Logic			
CHECKED					
CHECKED		SIZE A	CAGE NO.	DWG NO.	REV A
ISSUED		SCALE	SHEET 1 OF 1		

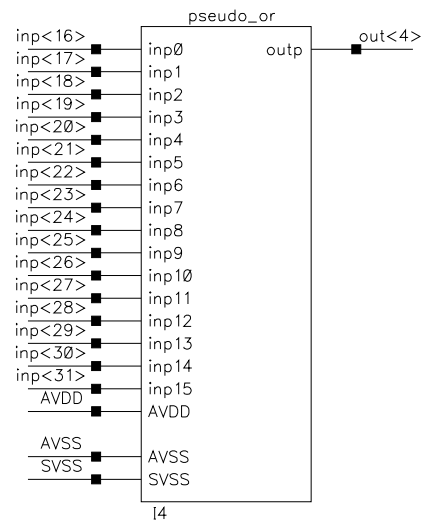
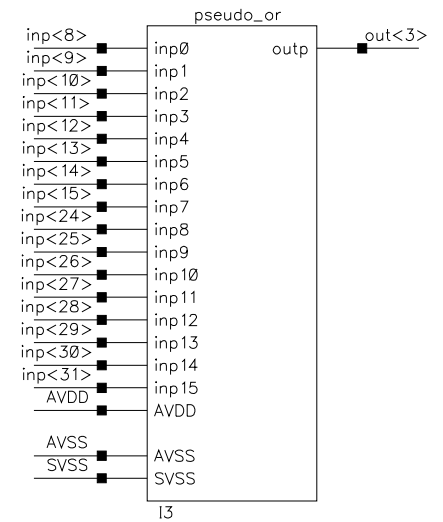
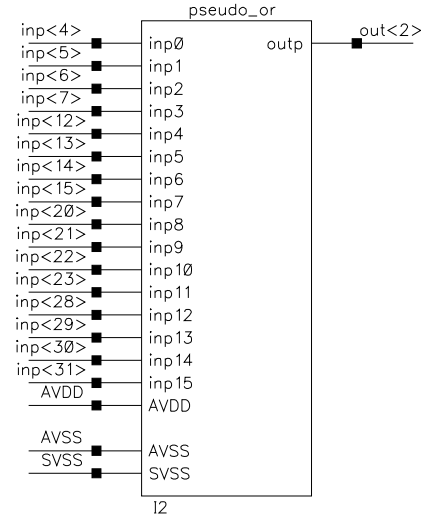
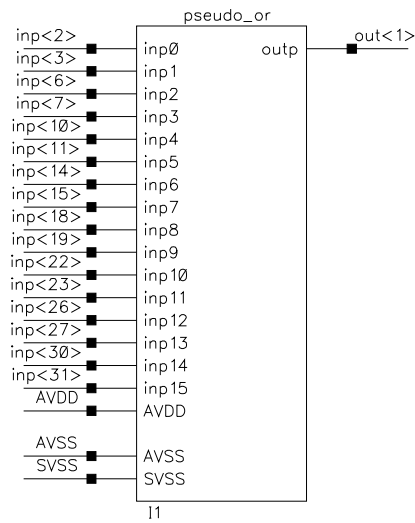
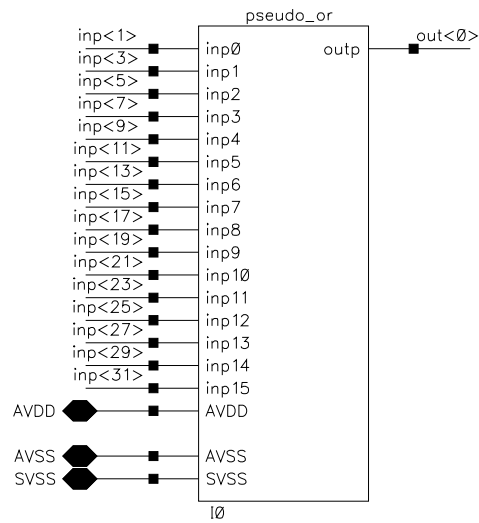
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	enc_dec_logic				
Mar 16 11:29:08 2010					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	A				
	SCALE			SHEET	1 OF 1

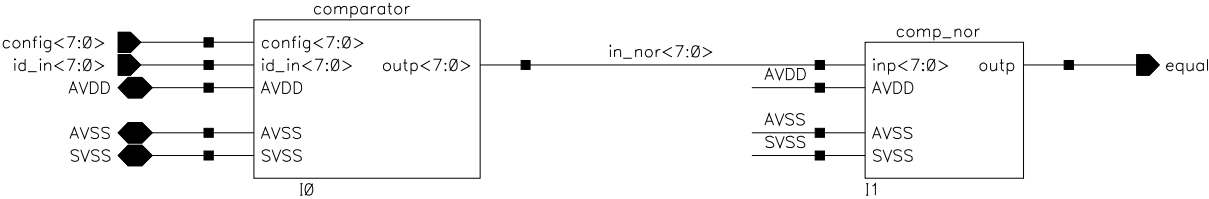
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

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inp<31:8> 



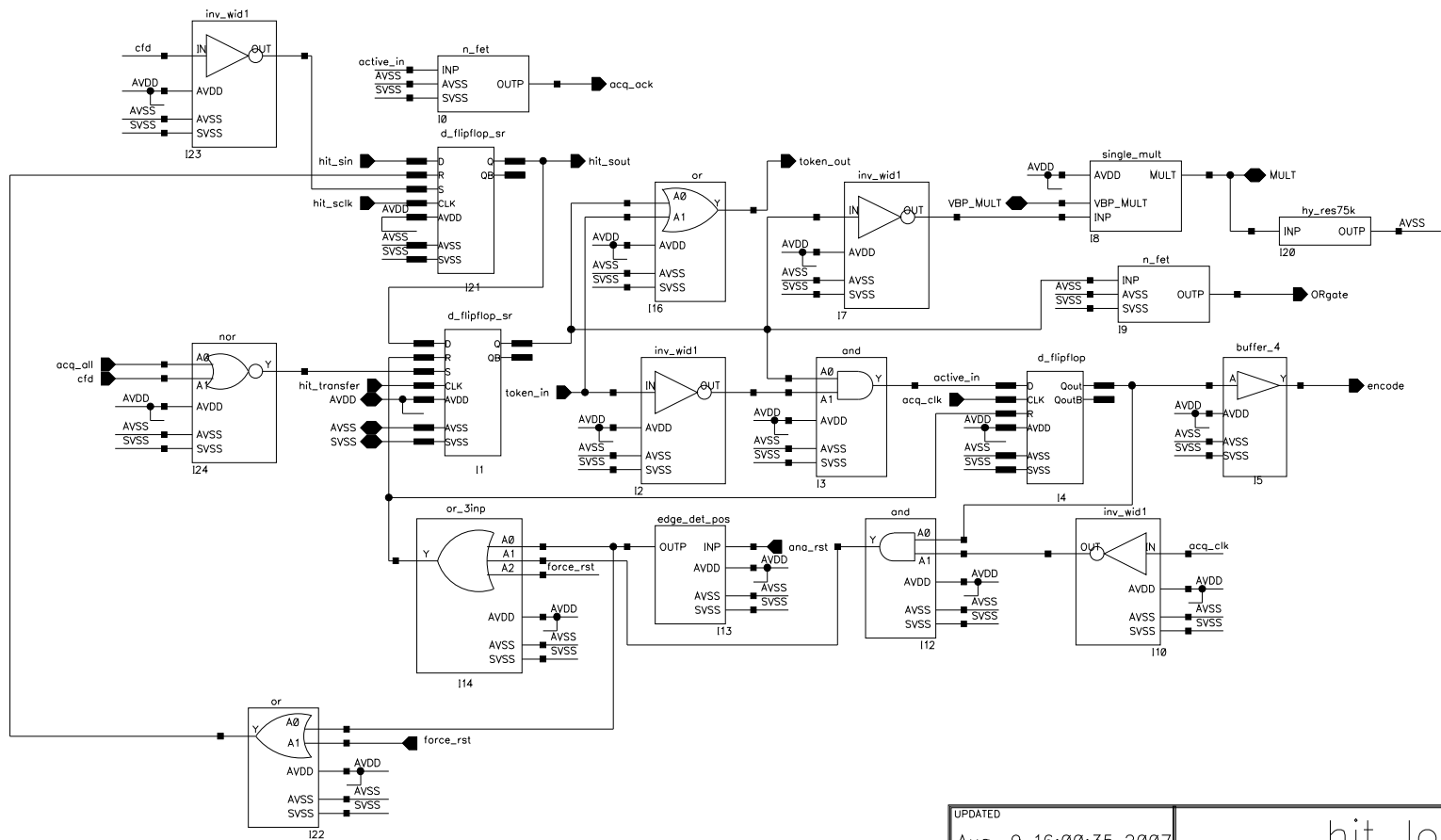
UPDATED	enc32to5			
Jul 31 11:15:11 2007				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



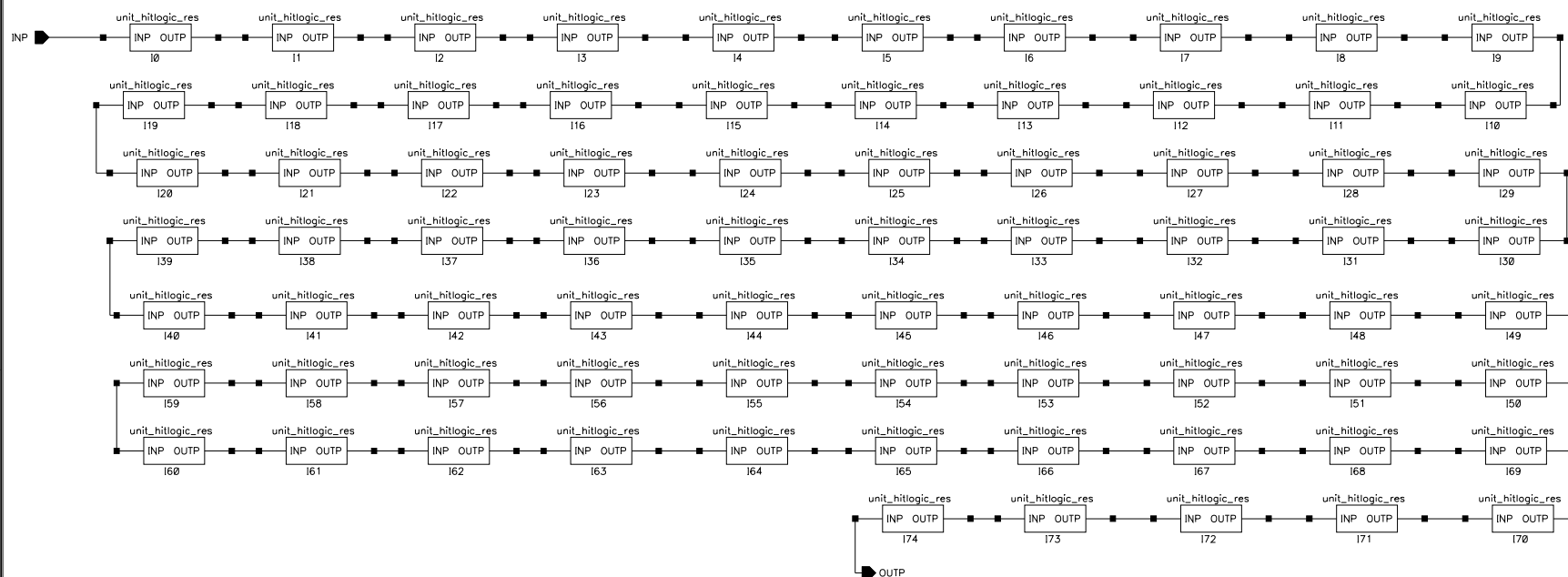
UPDATED	equal_logic			
Jul 9 14:10:40 2007				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Aug 9 16:00:35 2007		hit_logic		
DRAWN				
CHECKED				
CHECKED		SIZE B	CAGE NO.	DWG NO.
ISSUED		SCALE	SHEET 1 OF 1	

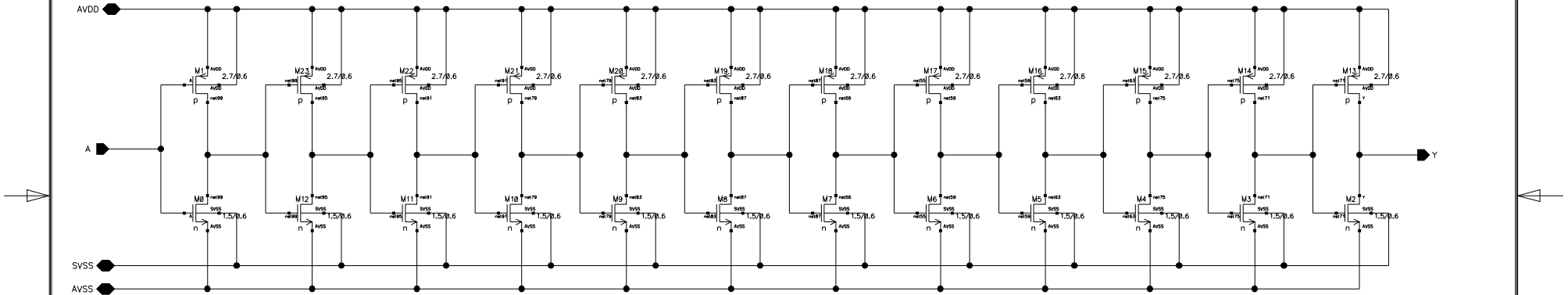
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jun 30 15:22:14 2005		HyRes75k		
DRAWN				
CHECKED				
CHECKED		SIZE B	CAGE NO.	DWG NO.
ISSUED		SCALE	SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV
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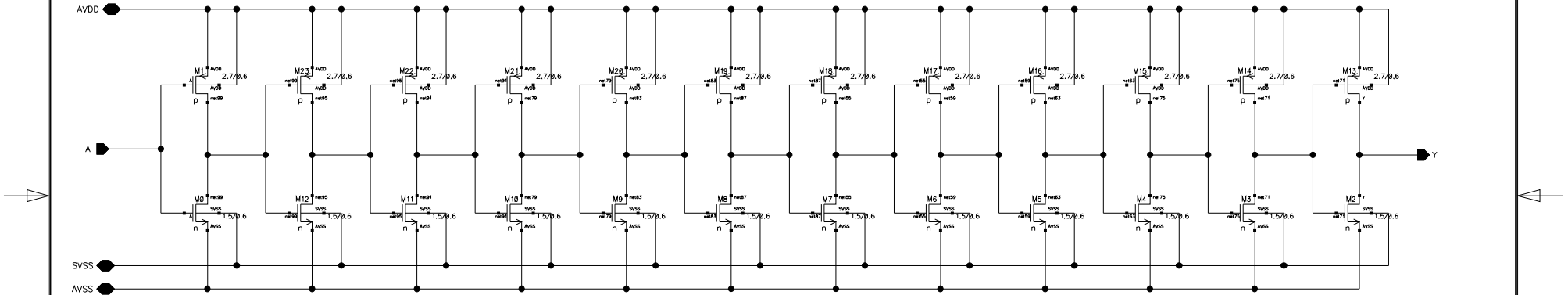
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	inv_12			
Jun 11 12:04:17 2007				
DRAWN				
CHECKED				
CHECKED	SIZE B	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	inv_12			
Jun 11 12:04:17 2007				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	B			
SCALE			SHEET	1 OF 1



CAGE NO.

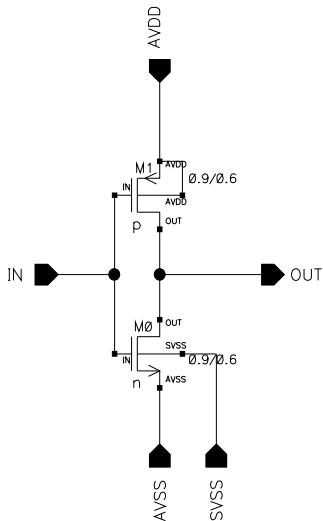
DWG NO.

SH 1

REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

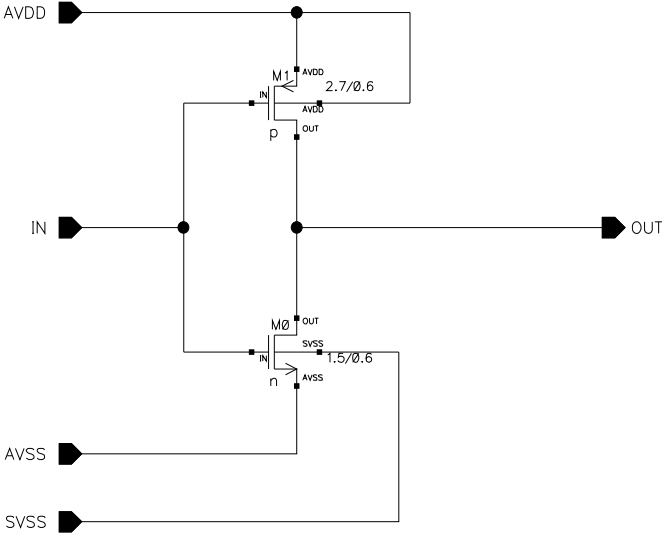


UPDATED
Aug 15 11:38:53 2007
DRAWN
CHECKED
CHECKED
ISSUED

inverter			
SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE			SHEET 1 OF 1



		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

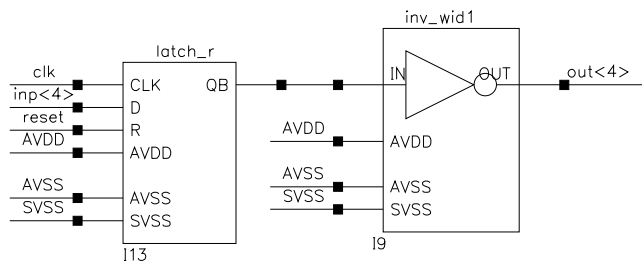
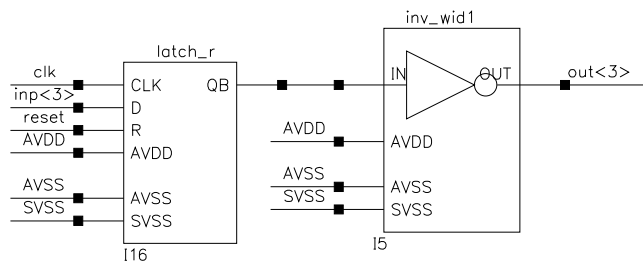
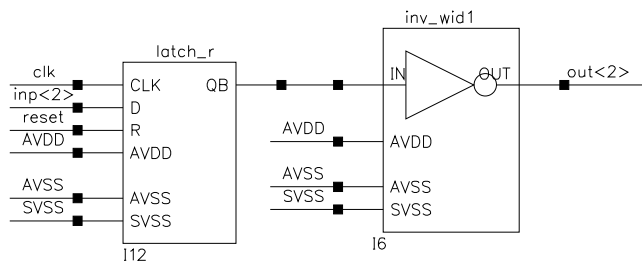
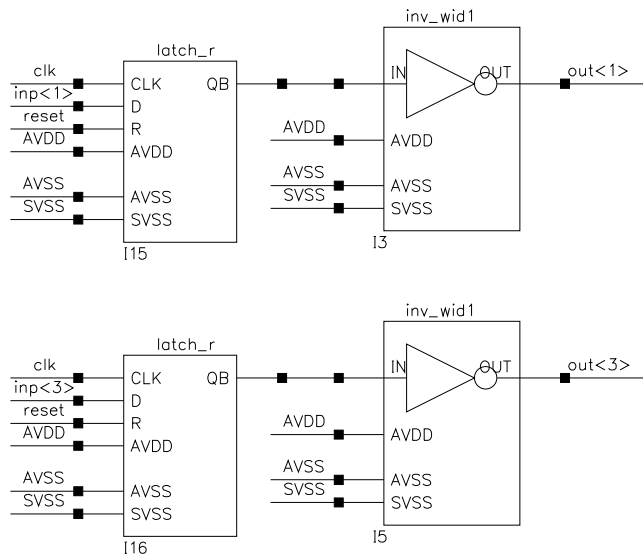
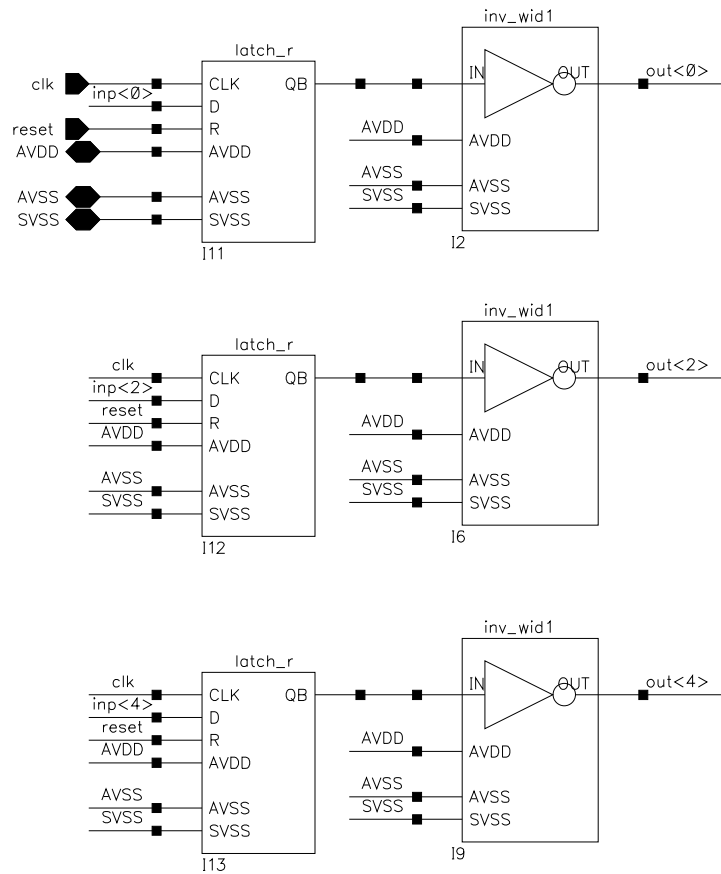


UPDATED	inv_wid1			
Jul 5 15:27:12 2007				
DRAWN				
CHECKED				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	

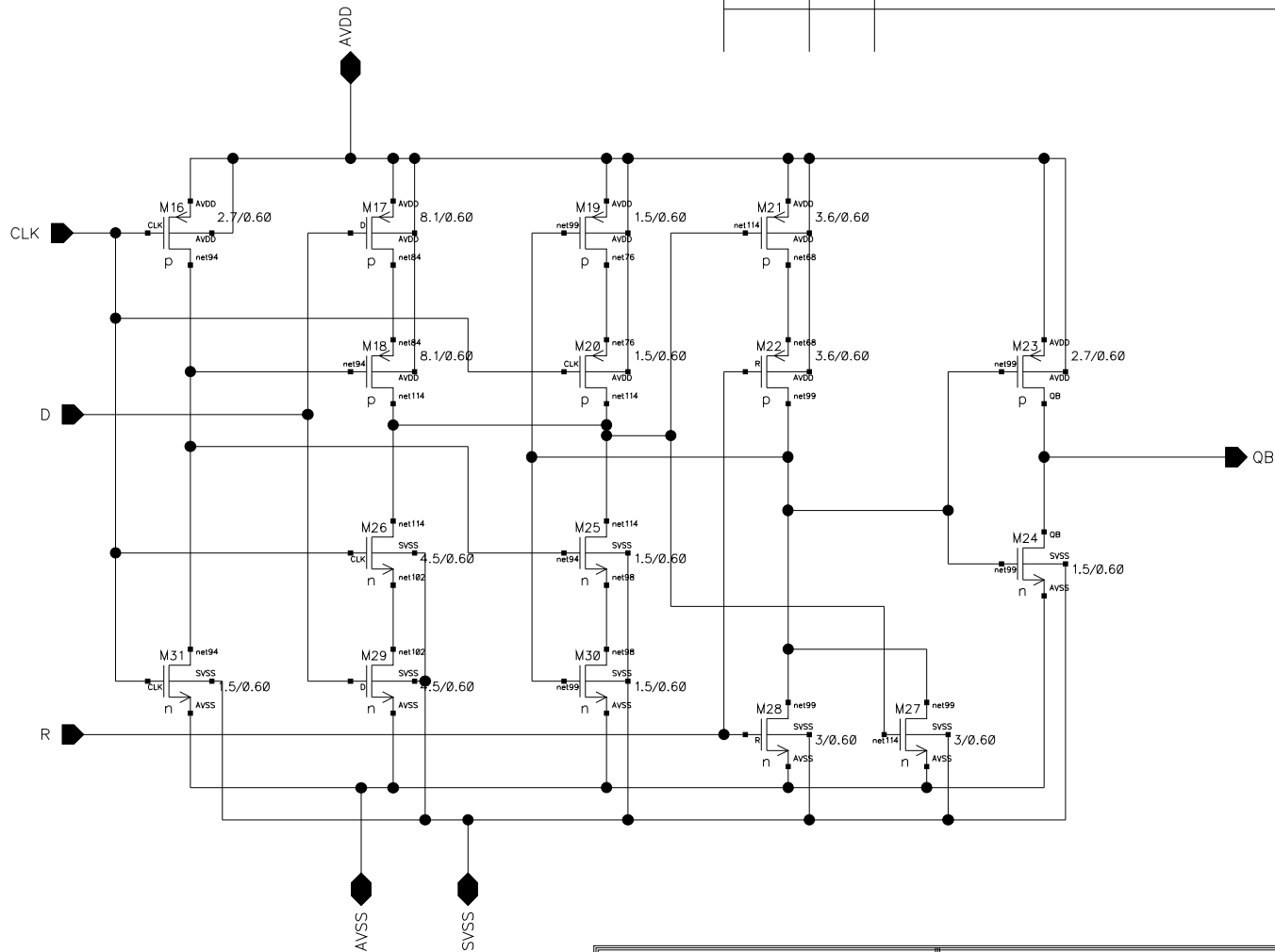
inp<4:0>

out<4:0>



UPDATED	latch_5bit				
Mar 16 13:12:31 2010					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



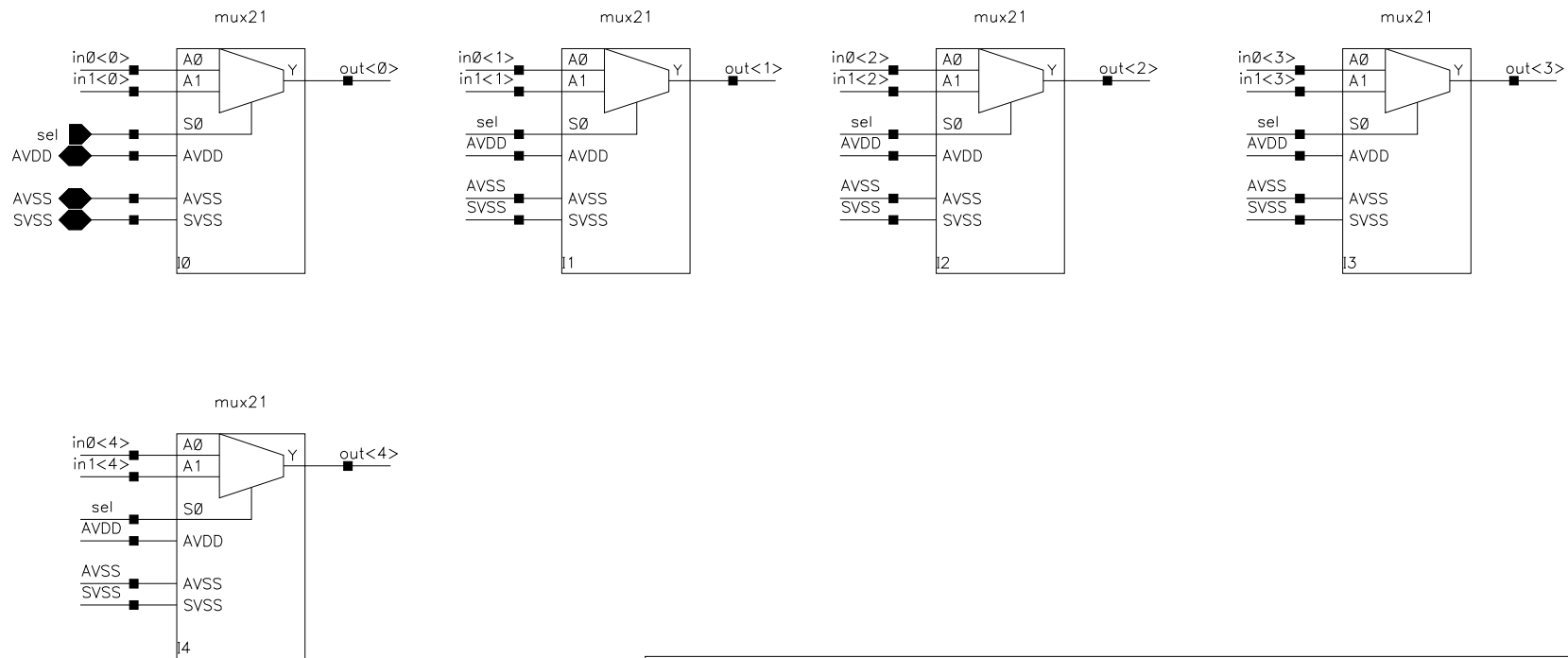
UPDATED		latch_r			
Mar 16 13:47:13 2010					
DRAWN					
CHECKED					
CHECKED					
ISSUED		SIZE	CAGE NO.	DWG NO.	REV
		A			
		SCALE			SHEET 1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

in0<4:0>

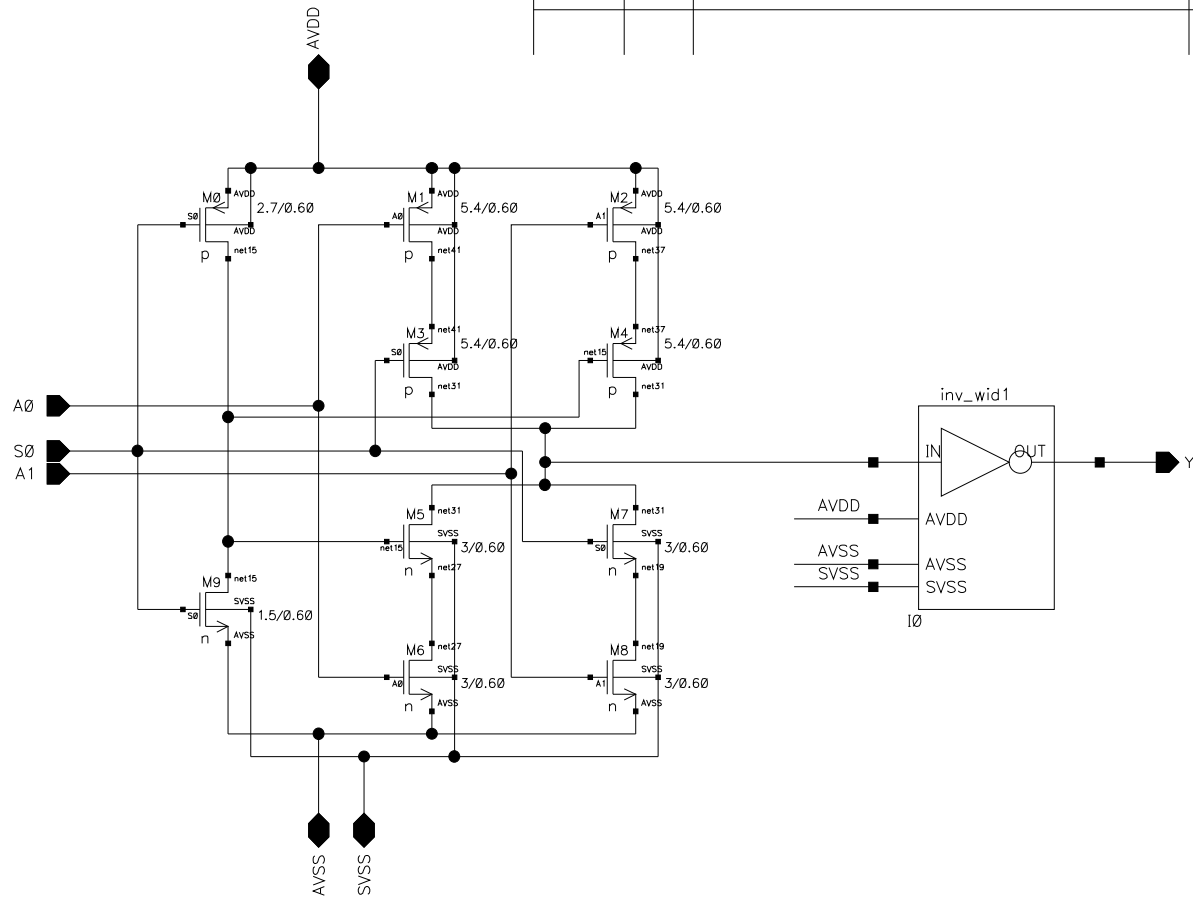
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out<4:0>

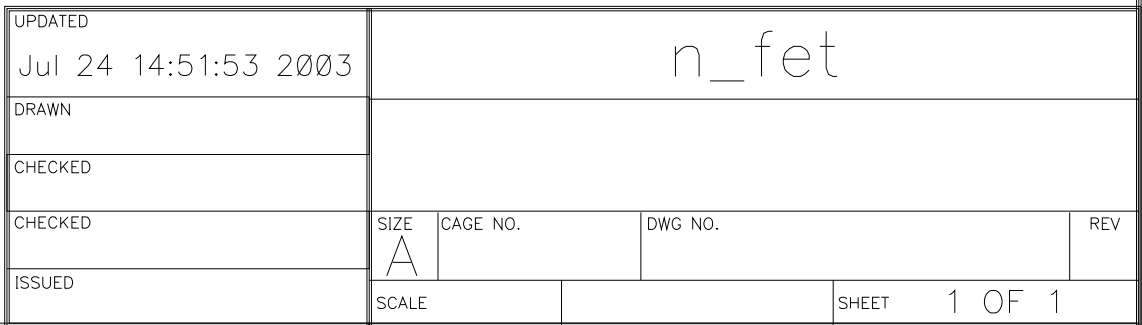


UPDATED	mux_5bit				
Jul 11 12:02:37 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	mux21			
Jul 5 15:27:21 2007				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1



CAGE NO.

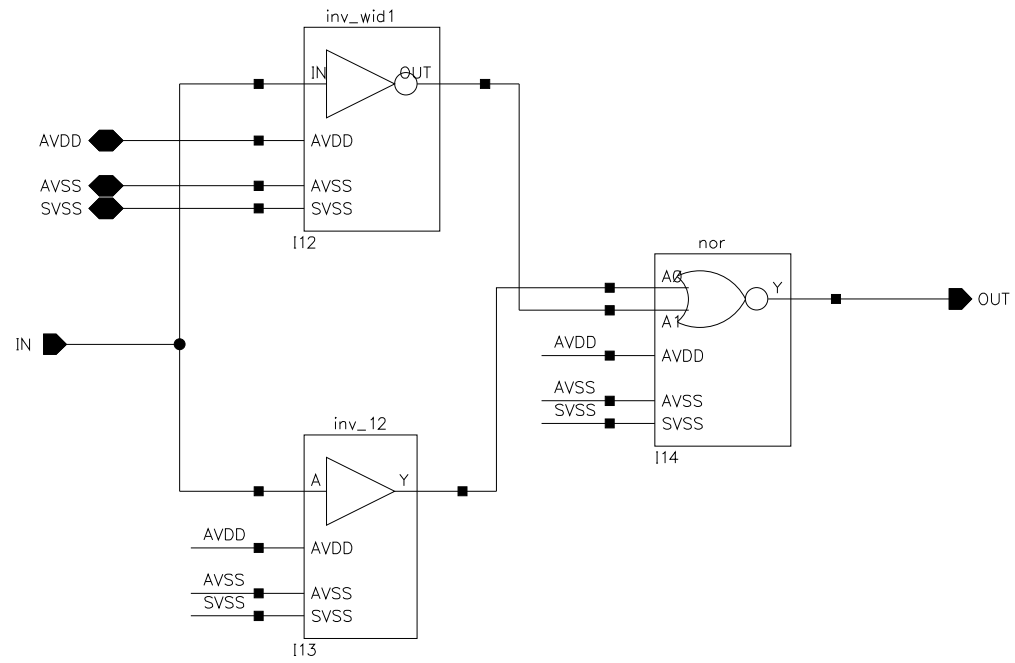
DWG NO.

SH 1

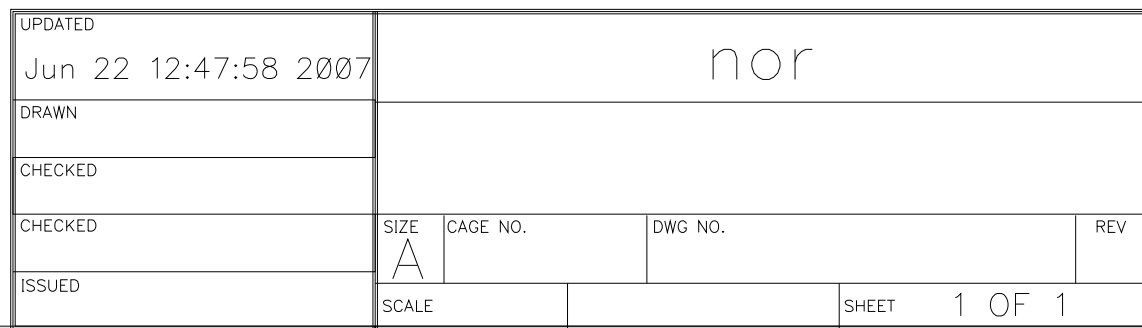
REV A

REVISIONS

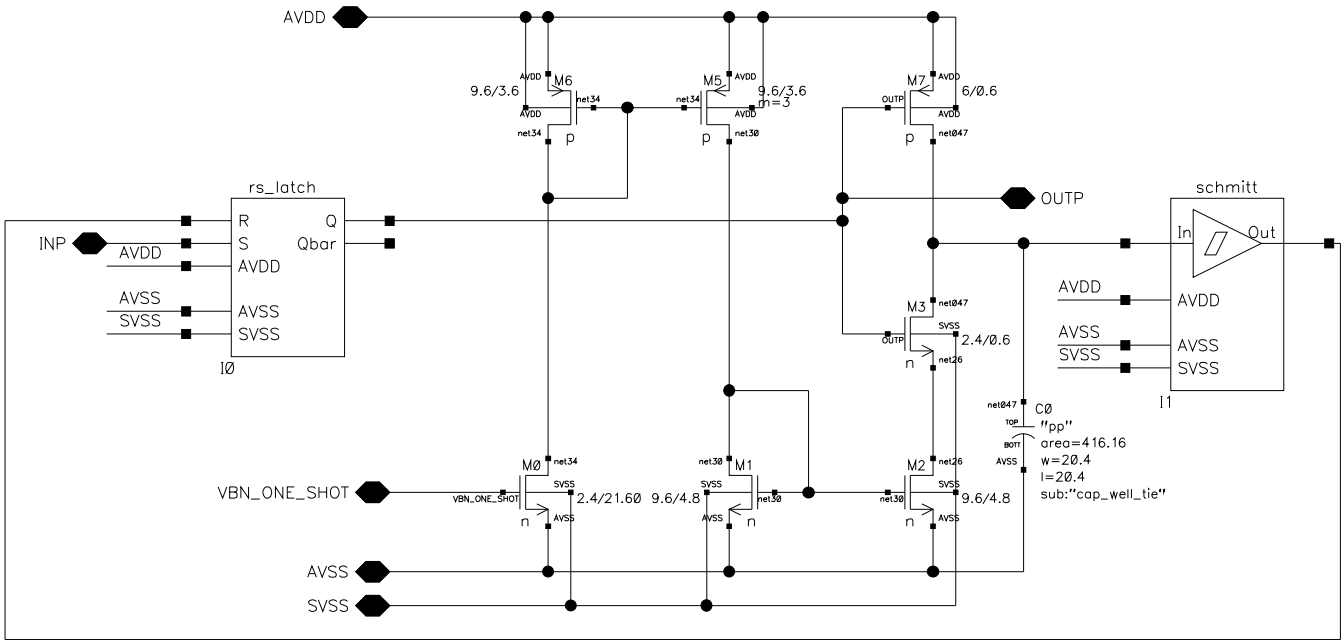
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	SIUE IC Design Lab			
Aug 13 15:53:22 2007				
DRAWN				
CHECKED	Narrow Pulse			
CHECKED				
ISSUED	SIZE A	CAGE NO.	DWG NO.	REV A
	SCALE		SHEET	1 OF 1

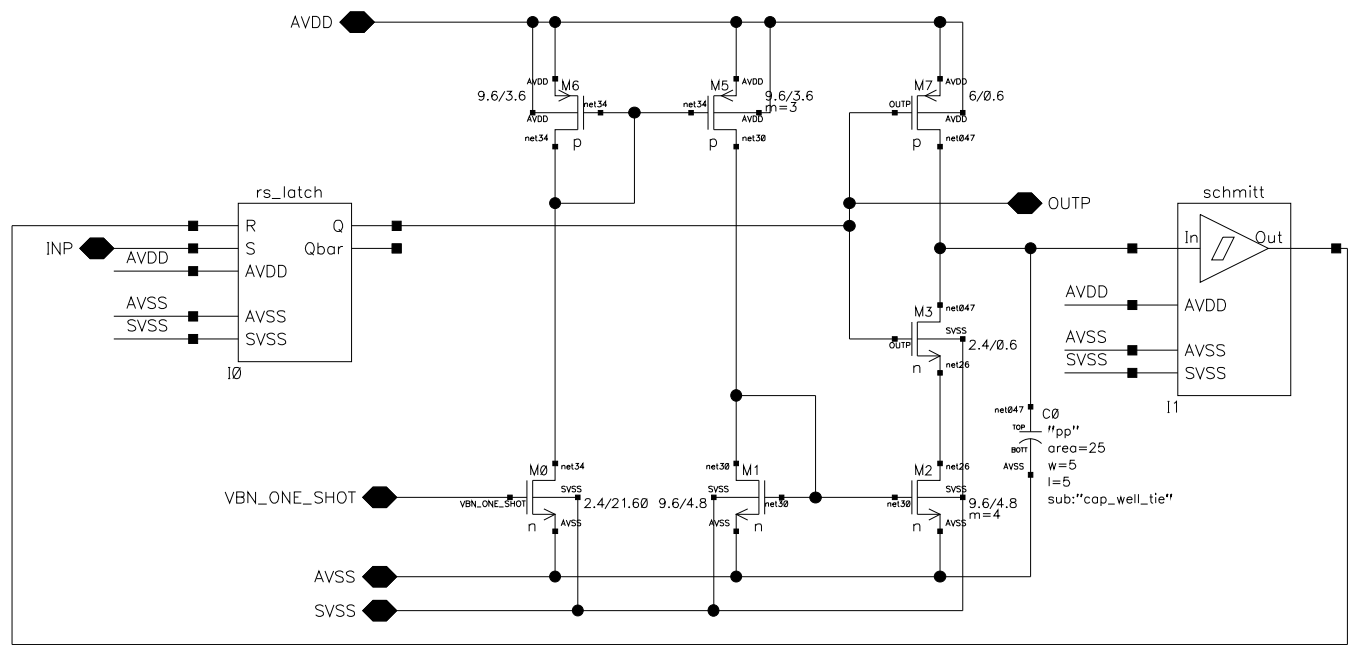


	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



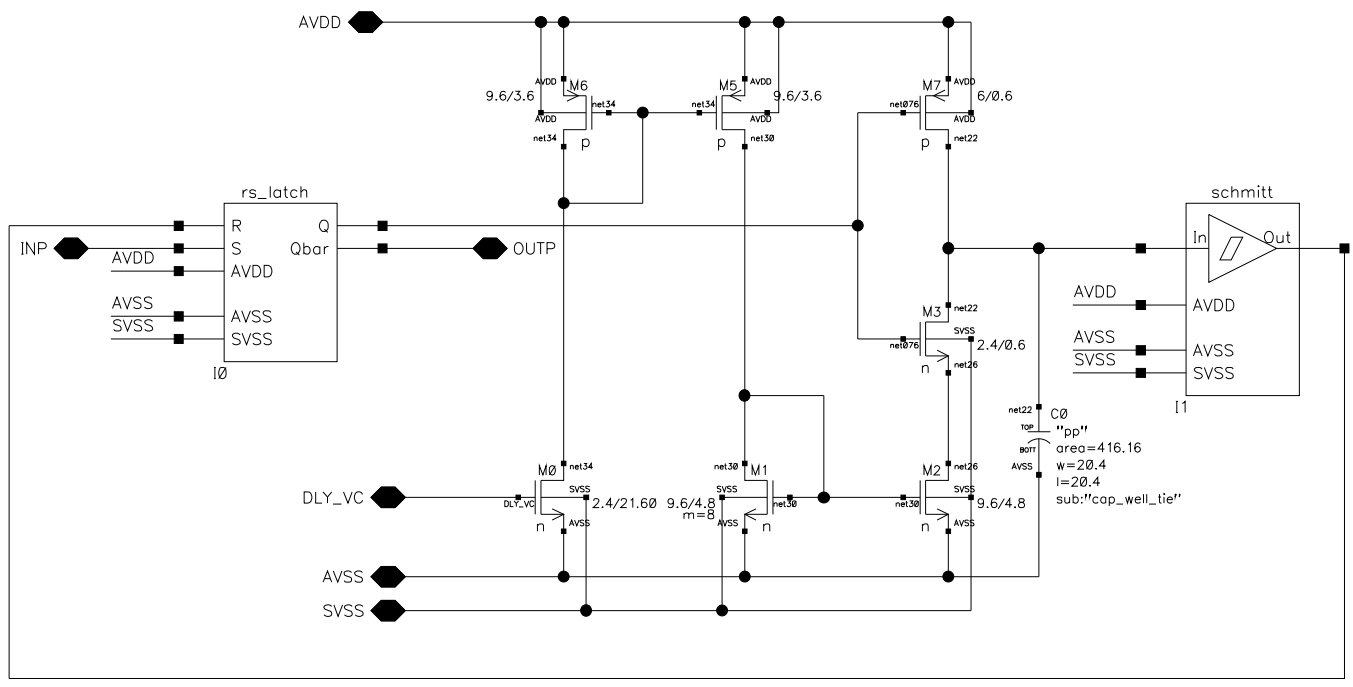
UPDATED		one_shot_100ns				
Aug 27 12:57:37 2007						
DRAWN						
CHECKED						
CHECKED		SIZE	CAGE NO.	DWG NO.		REV
ISSUED		A				
		SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



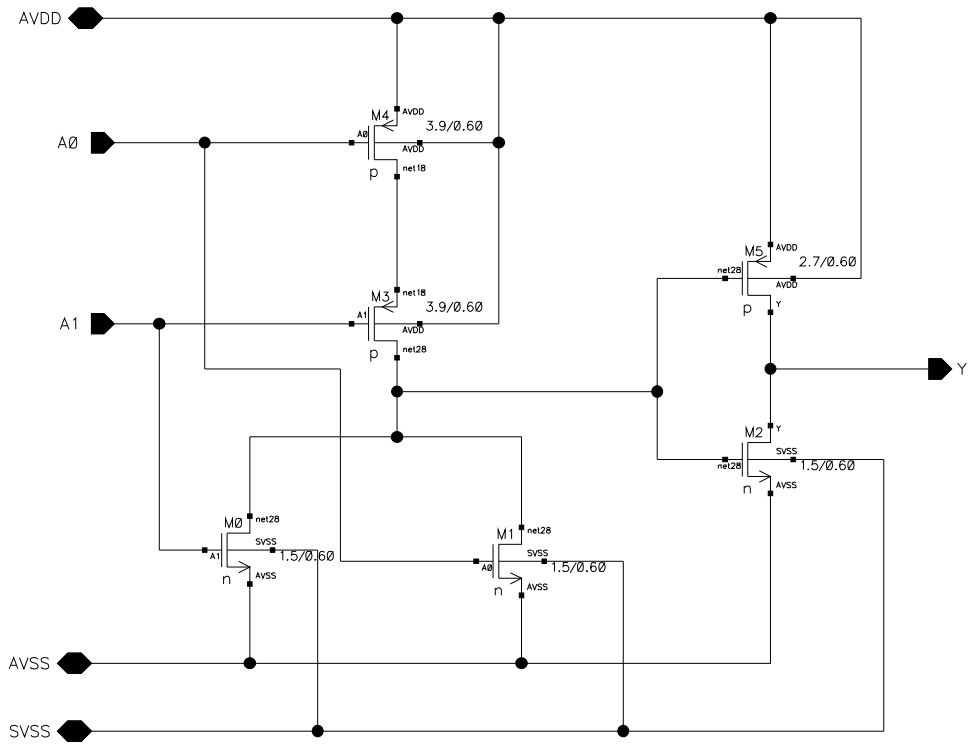
UPDATED Aug 27 12:57:37 2007		one_shot_100ns			
DRAWN					
CHECKED					
CHECKED		SIZE A	CAGE NO.	DWG NO.	REV
ISSUED		SCALE	SHEET 1 OF 1		

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



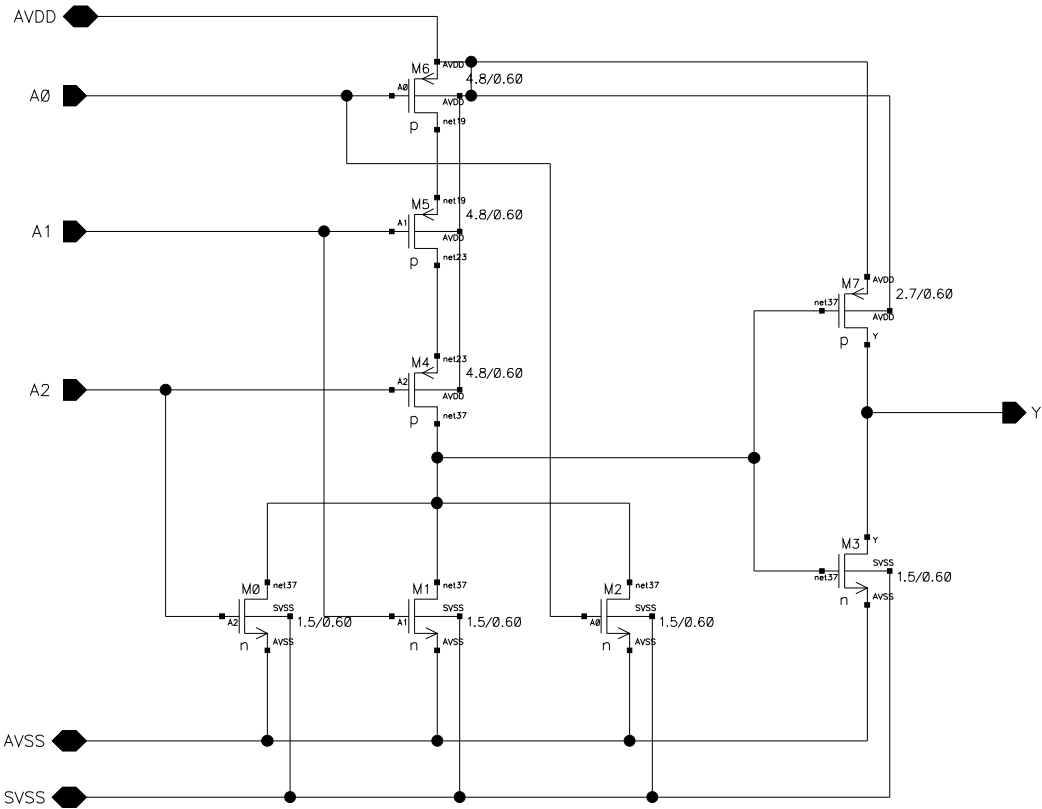
UPDATED	one_shot_vari				
Aug 14 10:41:49 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



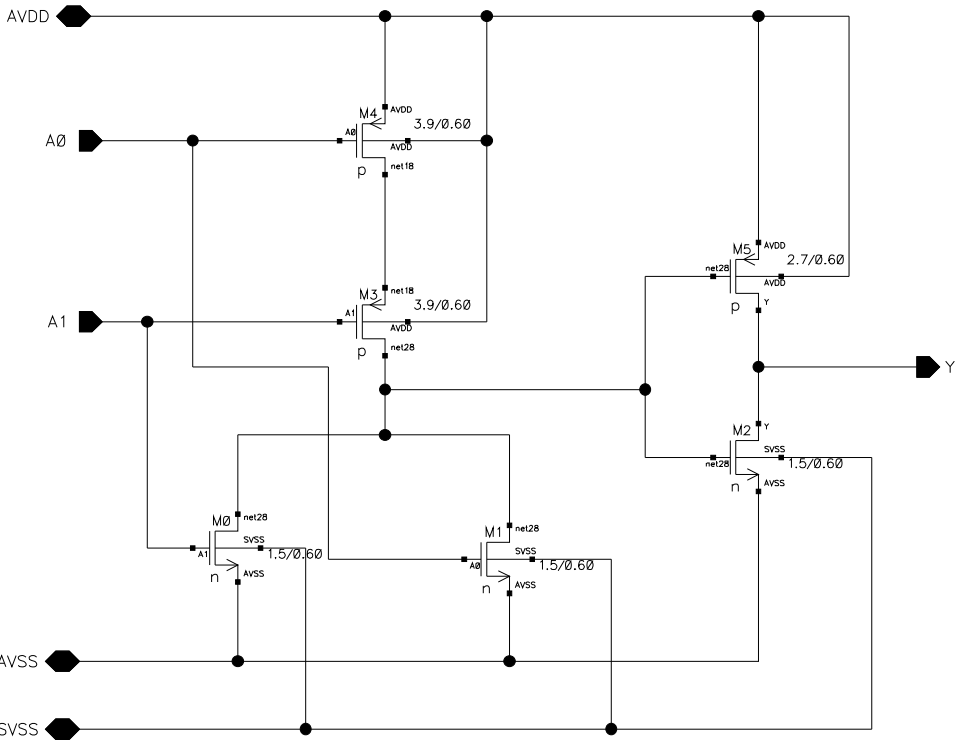
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Jun 11 15:23:02 2007					
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CHECKED	SIZE CAGE NO. DWG NO. REV				
CHECKED					
ISSUED					
SCALE		SHEET 1 OF 1			

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



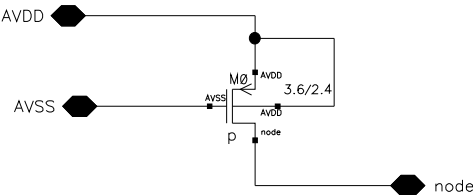
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		A			
		SCALE		SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



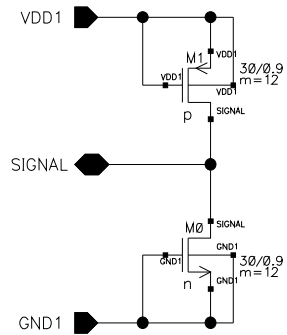
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ISSUED	SCALE	SHEET 1 OF 1			

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		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



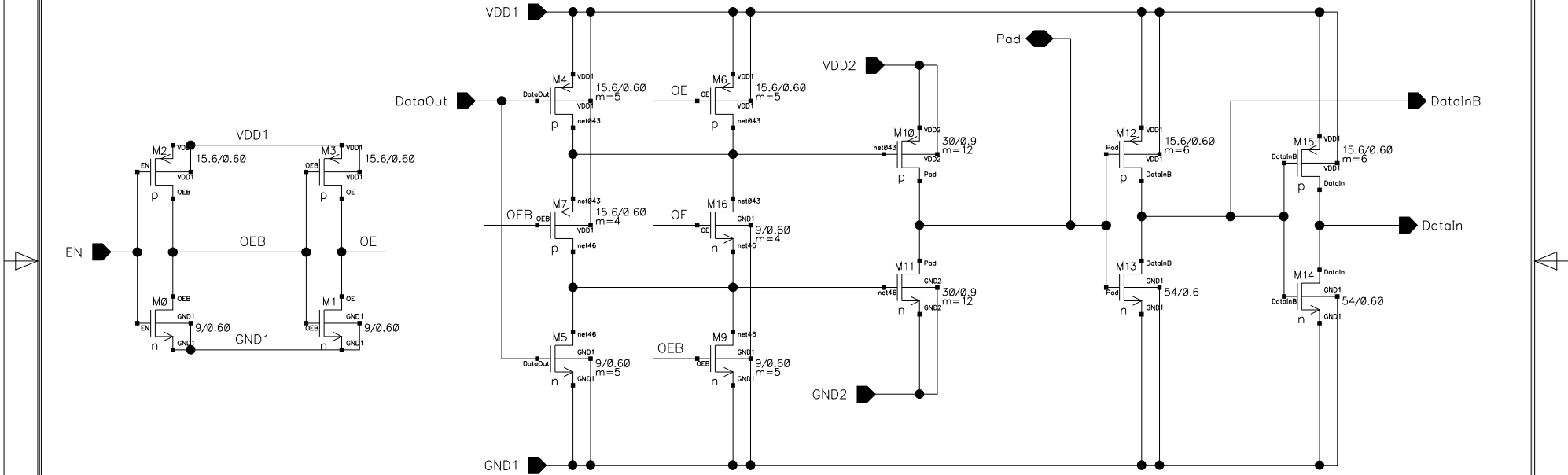
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Aug 3 14:33:16 2007					
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CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET 1	OF 1

		CAGE NO.	DWG NO.		SH 1	REV
		REVISIONS				
ZONE	REV	DESCRIPTION			DATE	APPROVED



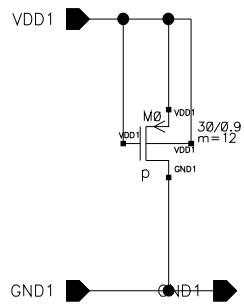
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ISSUED	SCALE			SHEET	1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



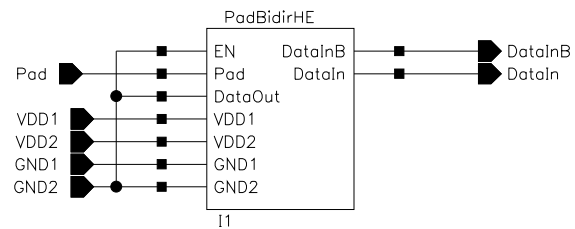
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Jul 9 16:28:29 2003					
DRAWN					
CHECKED					
CHECKED					
ISSUED		SIZE	CAGE NO.	DWG NO.	REV
		A			
		SCALE		SHEET	1 OF 1

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		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



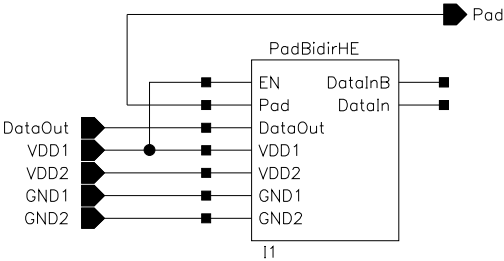
UPDATED	PadGnd				
Nov 11 15:38:19 2004					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

CAGE NO.		DWG NO.		SH 1	REV
REVISIONS					
ZONE	REV	DESCRIPTION	DATE	APPROVED	



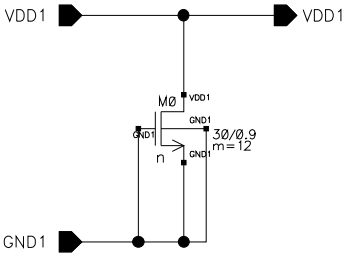
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CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	A			
SCALE		SHEET		1 OF 1

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		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



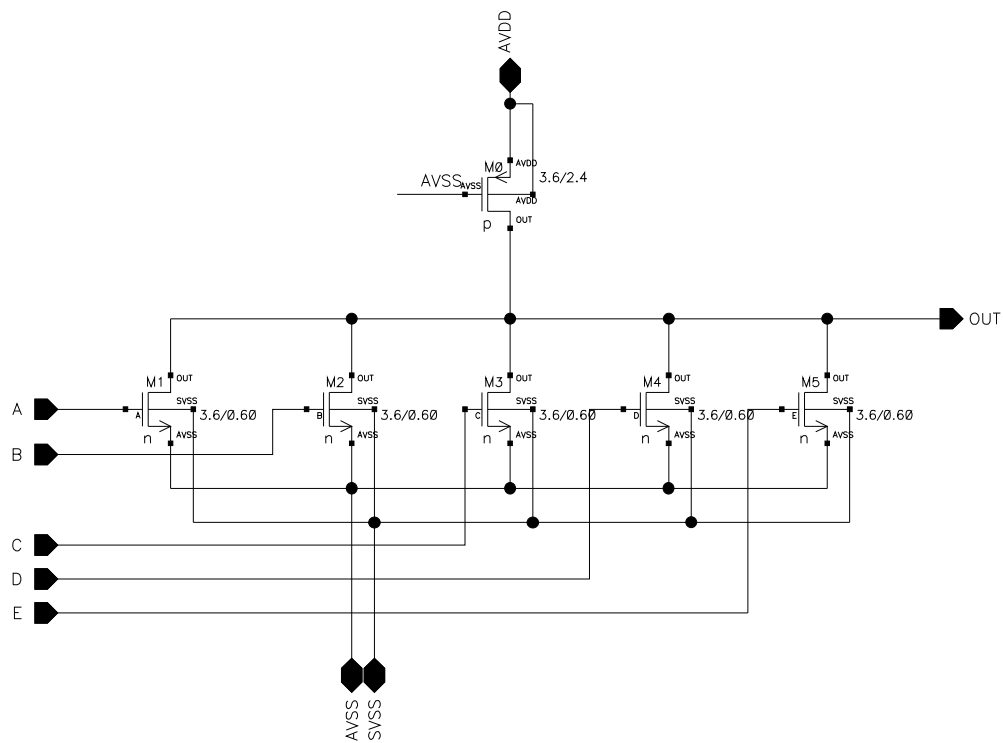
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Jul 9 16:11:11 2003					
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CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET 1	OF 1

		CAGE NO.	DWG NO.	SH 1	REV
REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED



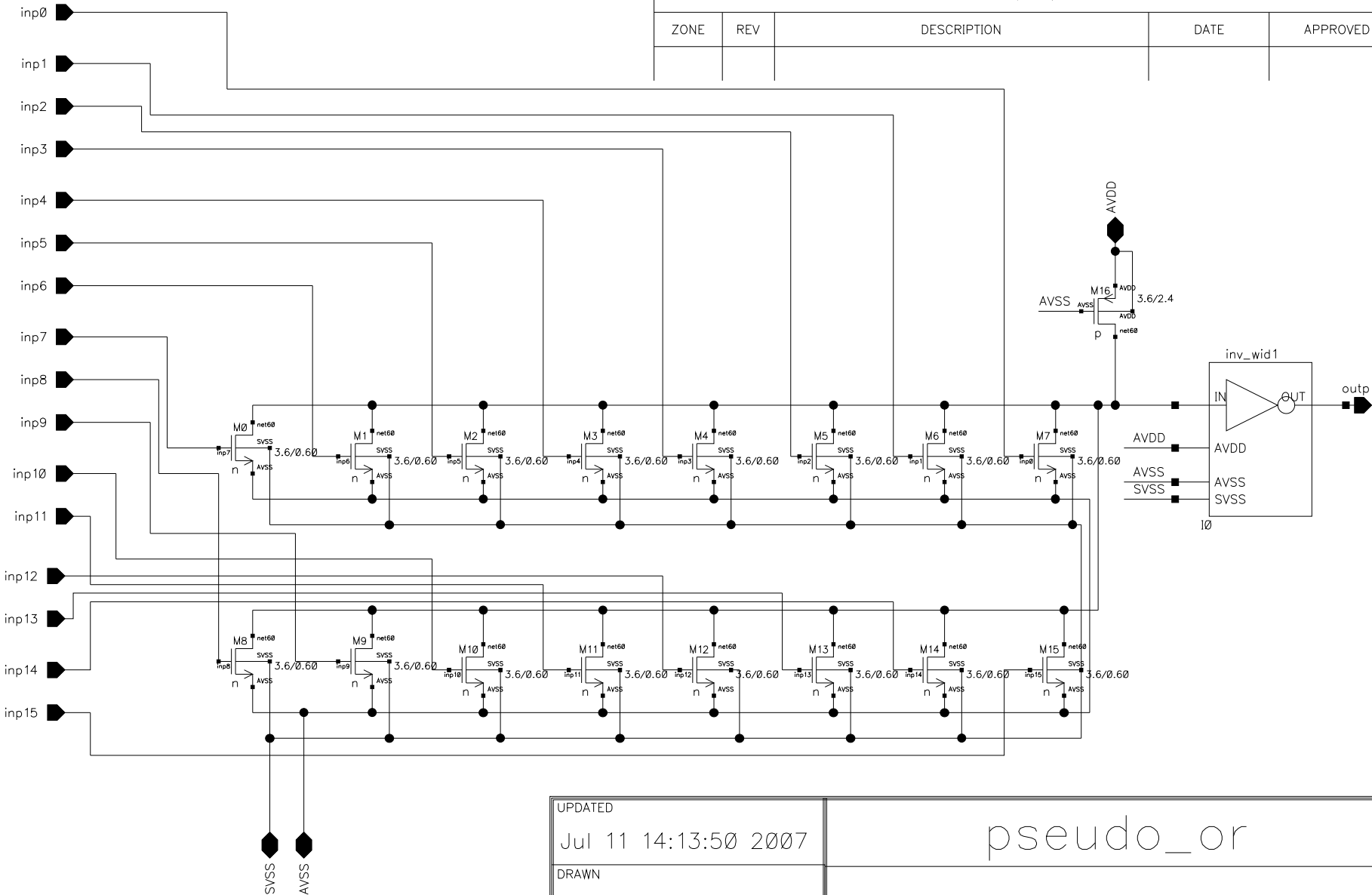
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Nov 11 15:36:54 2004					
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CHECKED					
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ISSUED	SCALE			SHEET 1	OF 1

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



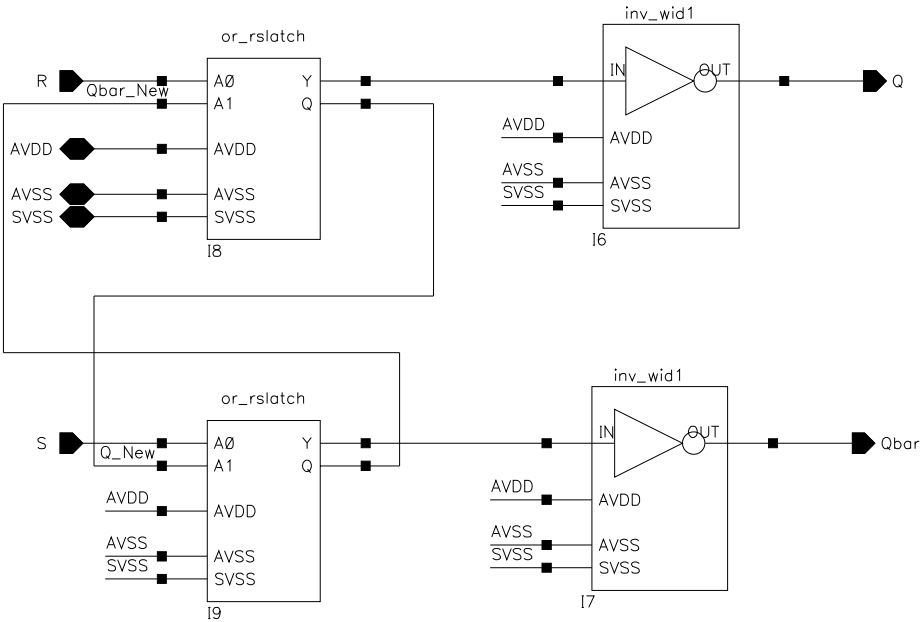
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Jul 11 13:37:50 2007					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



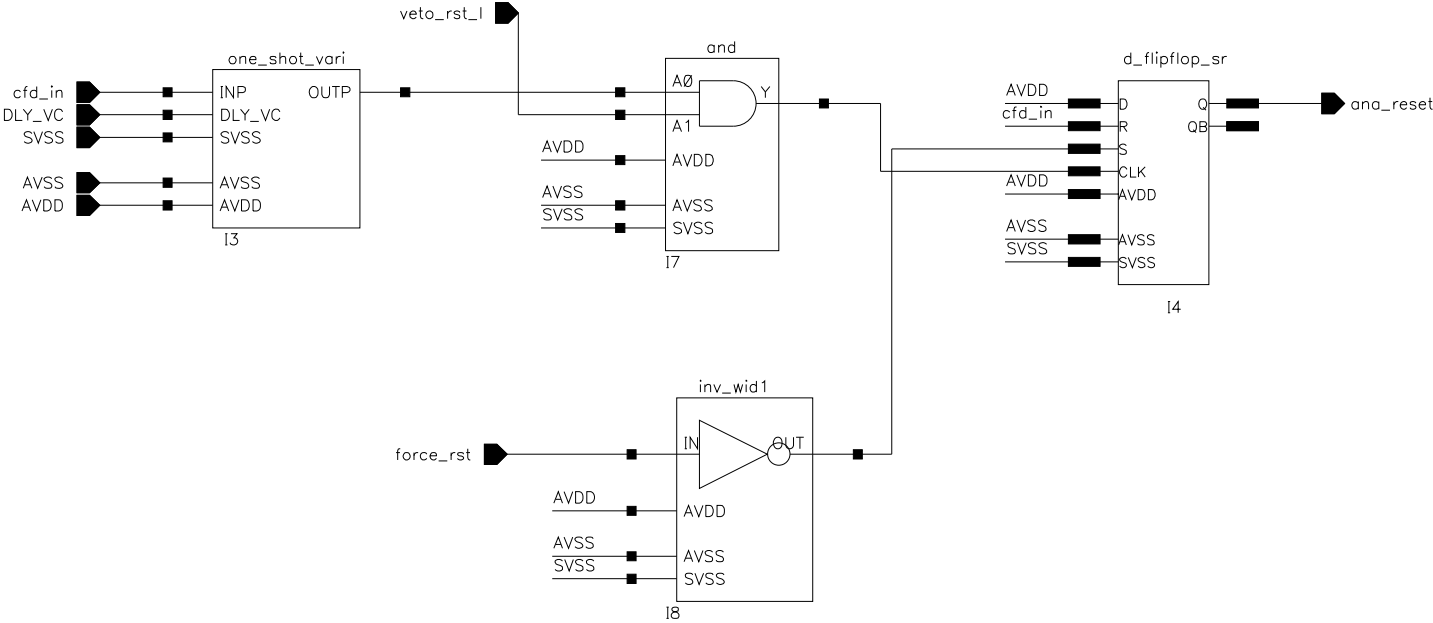
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Jul 11 14:13:50 2007					
DRAWN					
CHECKED					
CHECKED		SIZE	CAGE NO.	DWG NO.	REV
ISSUED		A			
		SCALE		SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



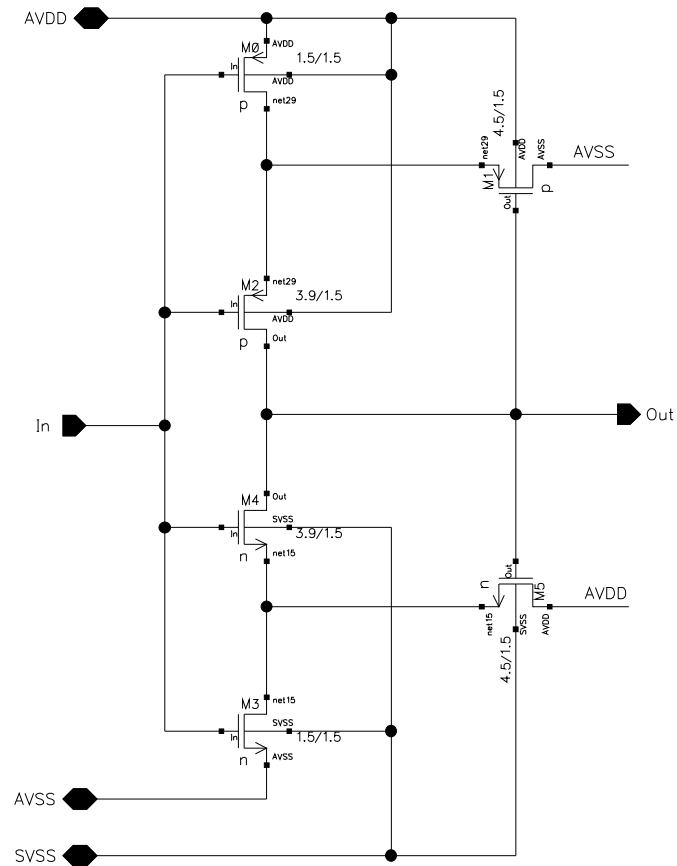
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Aug 13 14:51:32 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

	CAGE NO.		DWG NO.		SH 1	REV A
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



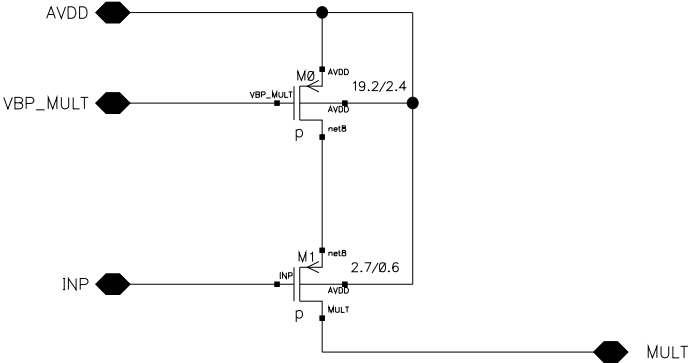
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Sep 11 11:59:16 2007					
DRAWN					
CHECKED					
CHECKED					
ISSUED		SIZE A	CAGE NO.	DWG NO.	REV A
		SCALE		SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



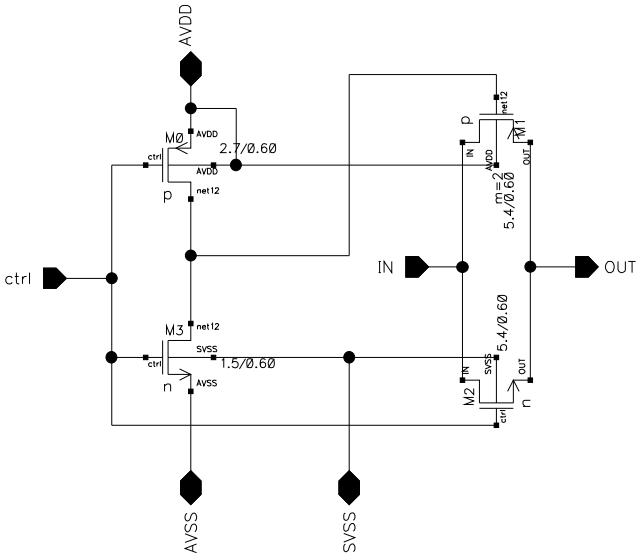
UPDATED	schmitt				
Aug 13 11:29:31 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



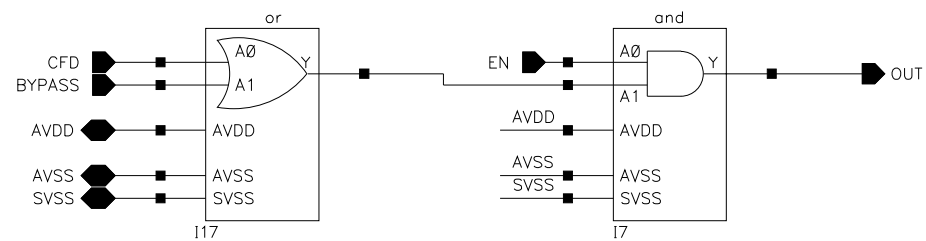
UPDATED	single_mult				
Jun 15 15:32:45 2007					
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CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET 1 OF 1			

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	sw_channel				
Aug 13 15:55:31 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

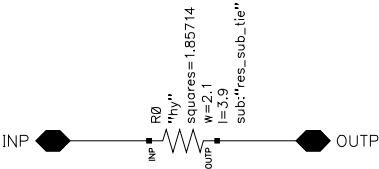
	CAGE NO.		DWG NO.		SH 1	REV A
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



UPDATED	SIUE IC Design Lab Triggering Logic				
Aug 13 11:15:28 2007					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV A	
ISSUED	SCALE	SHEET 1 OF 1			

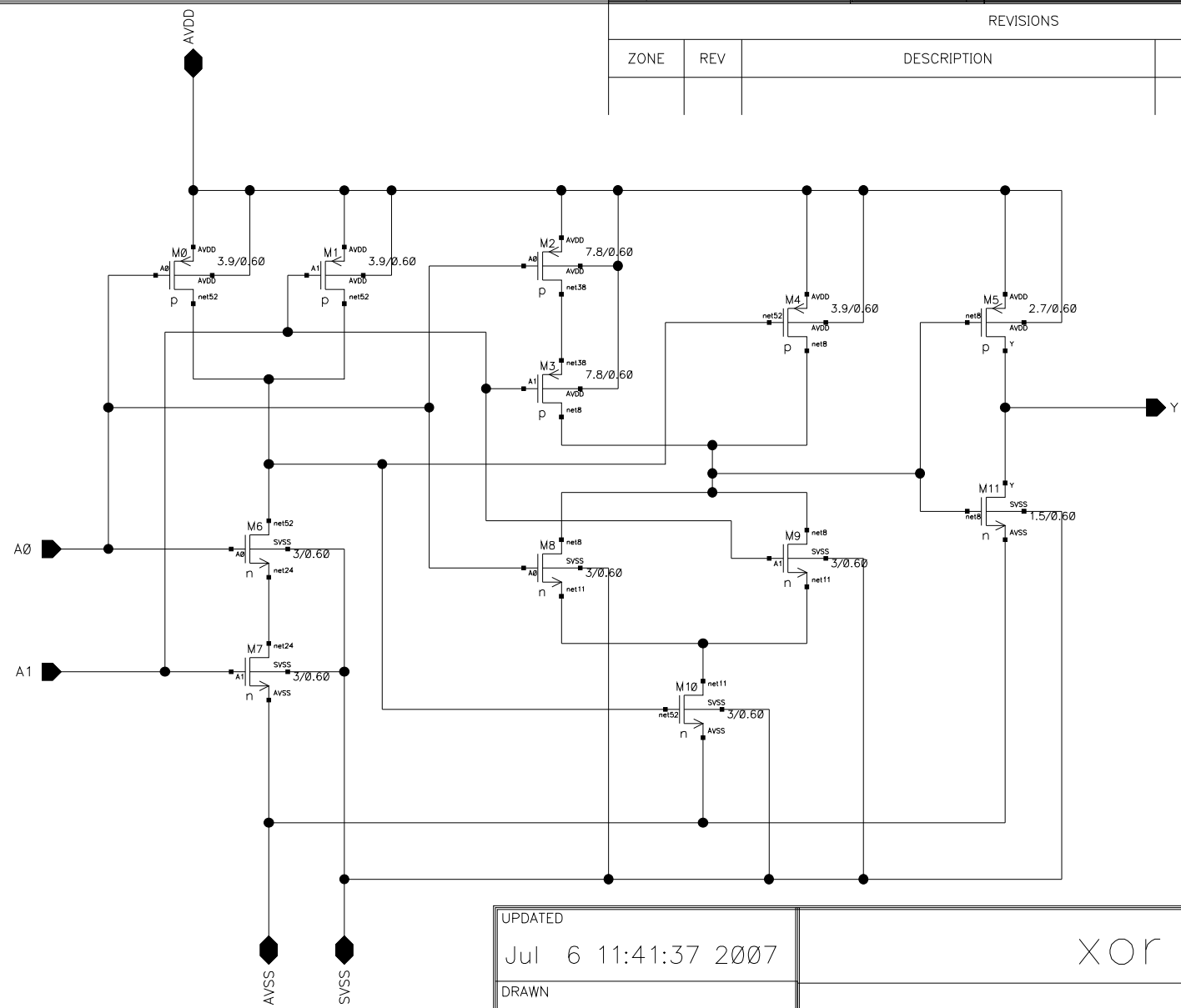
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

Resistor has l=3.9u and w=2.1u



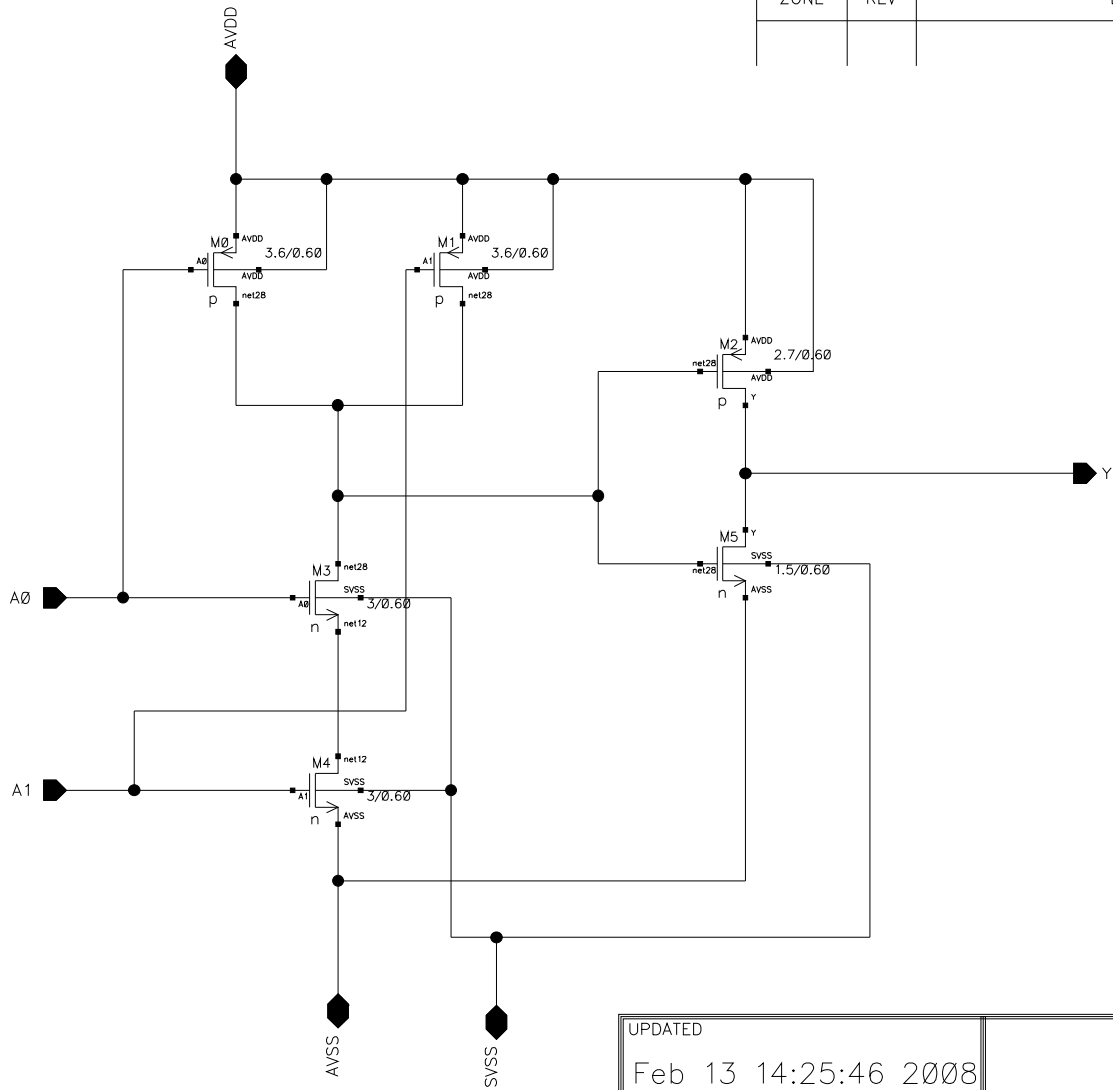
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Jun 30 15:19:07 2005				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



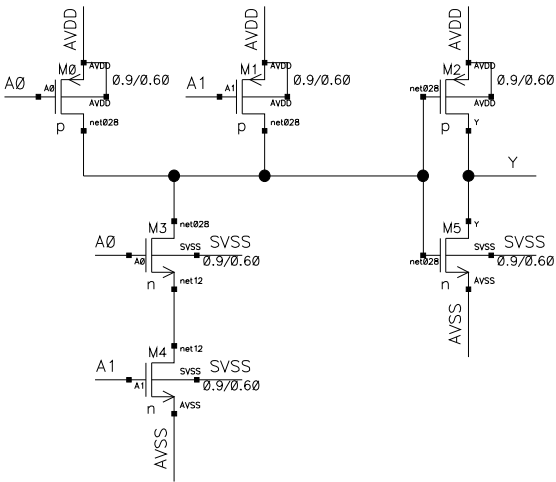
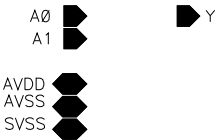
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Jul 6 11:41:37 2007					
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CHECKED					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.		REV
	A				
ISSUED	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	and				
Feb 13 14:25:46 2008					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

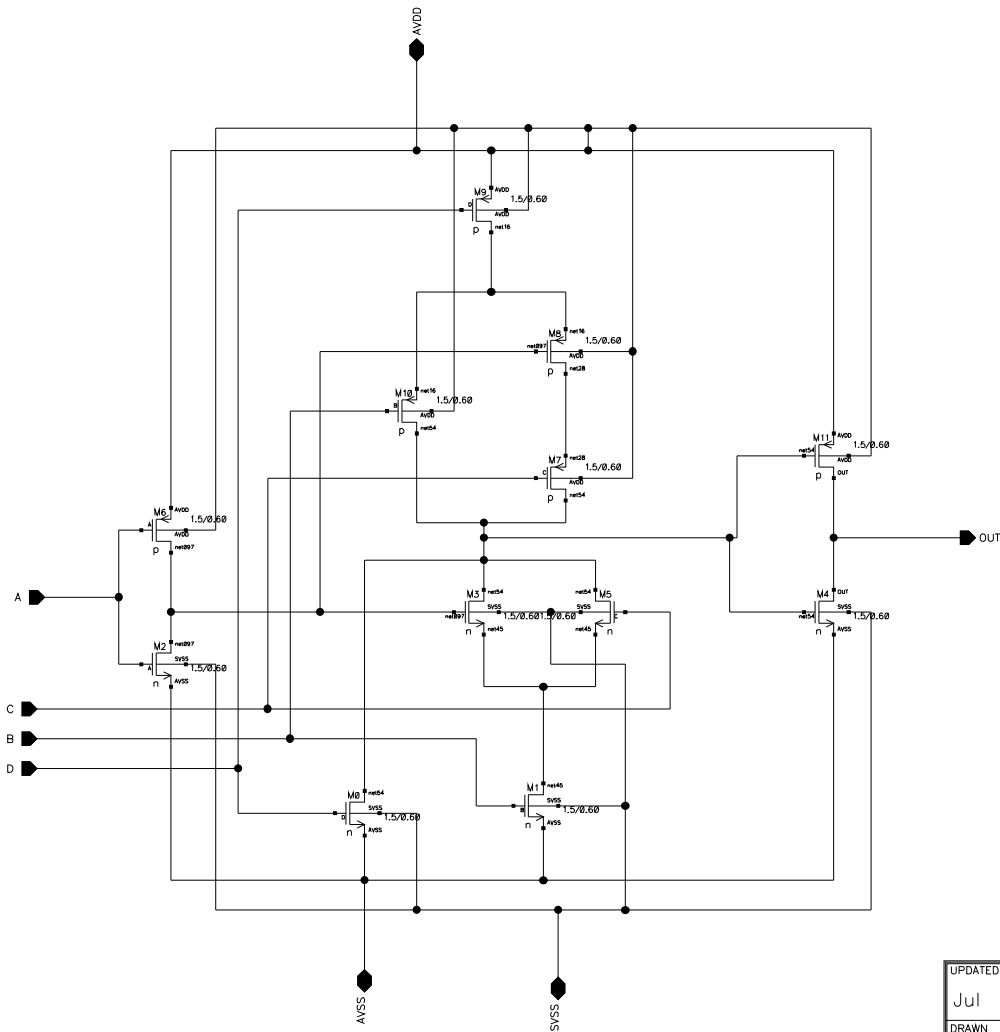
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		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	and				
Aug 8 14:14:18 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jul 9 11:16:30 2007		andor		
DRAWN				
CHECKED				
CHECKED	SIZE B	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

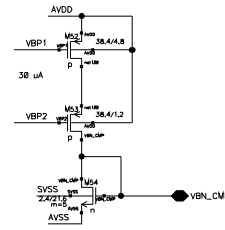
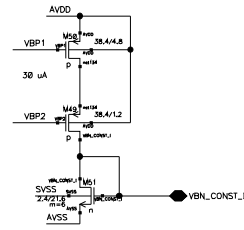
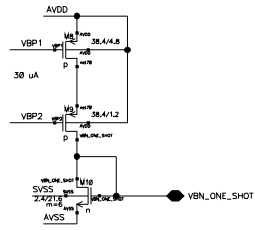
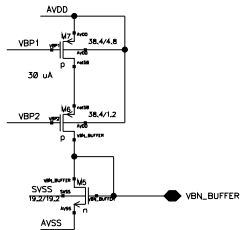
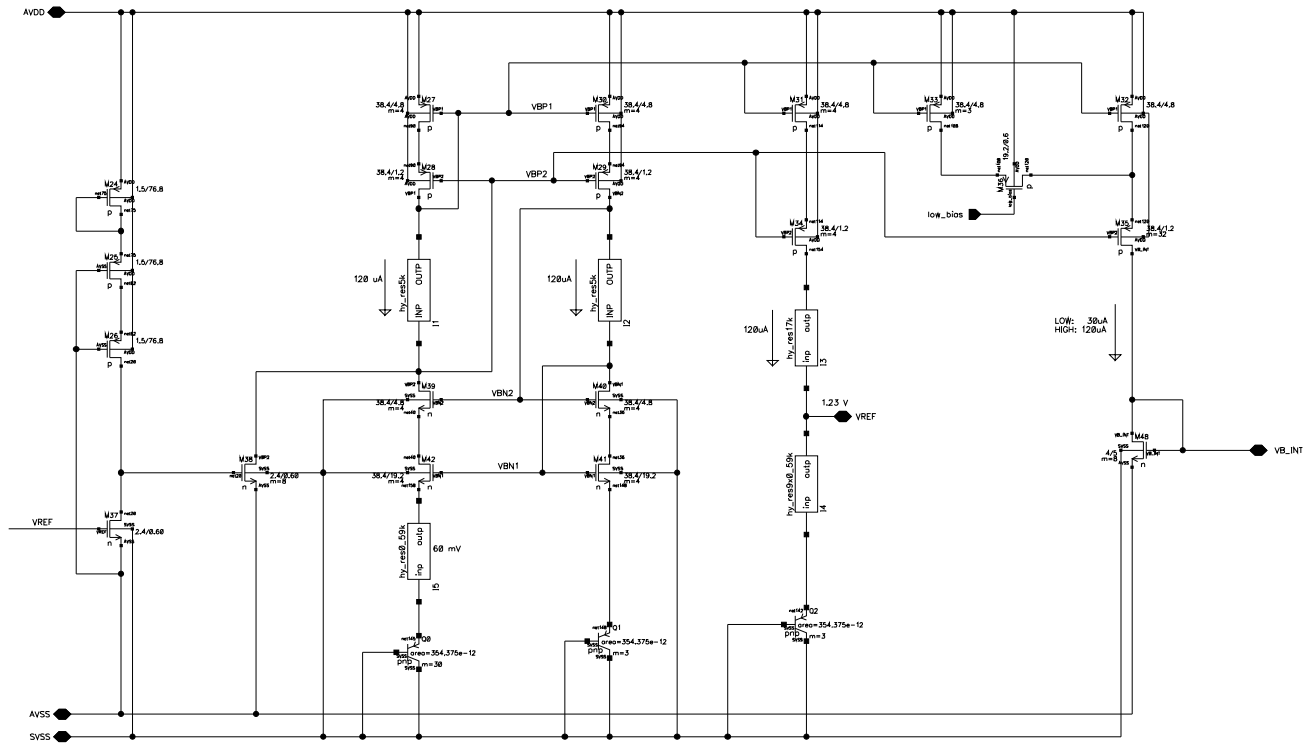
4

3

2

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Oct 30 14:23:38 2007		bias		
DRAWN				
CHECKED				
CHECKED	SIZE C	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		

4

3

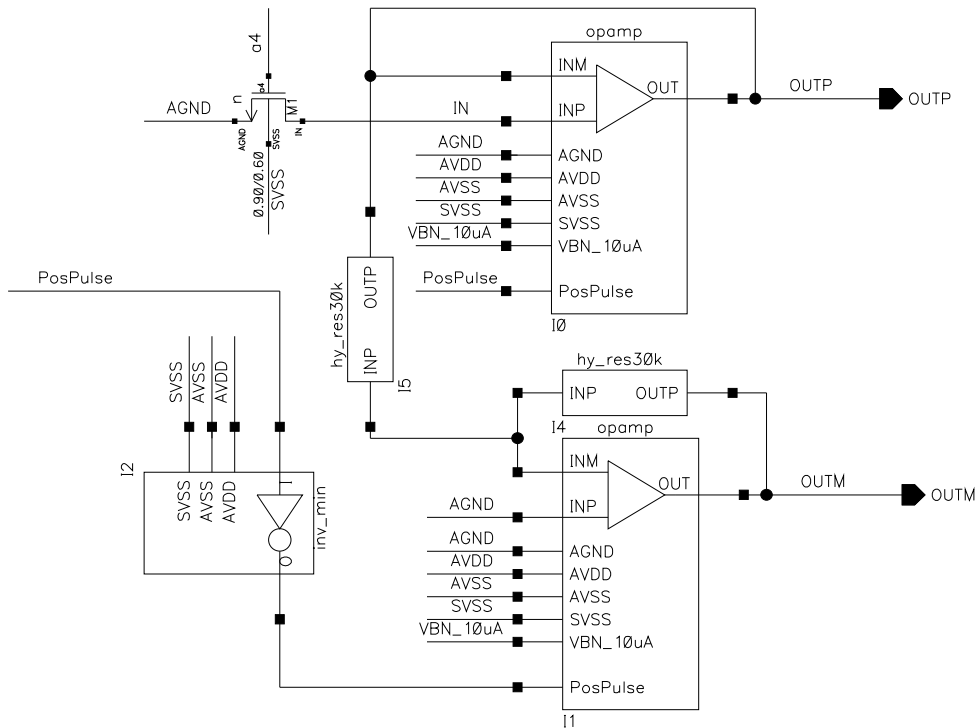
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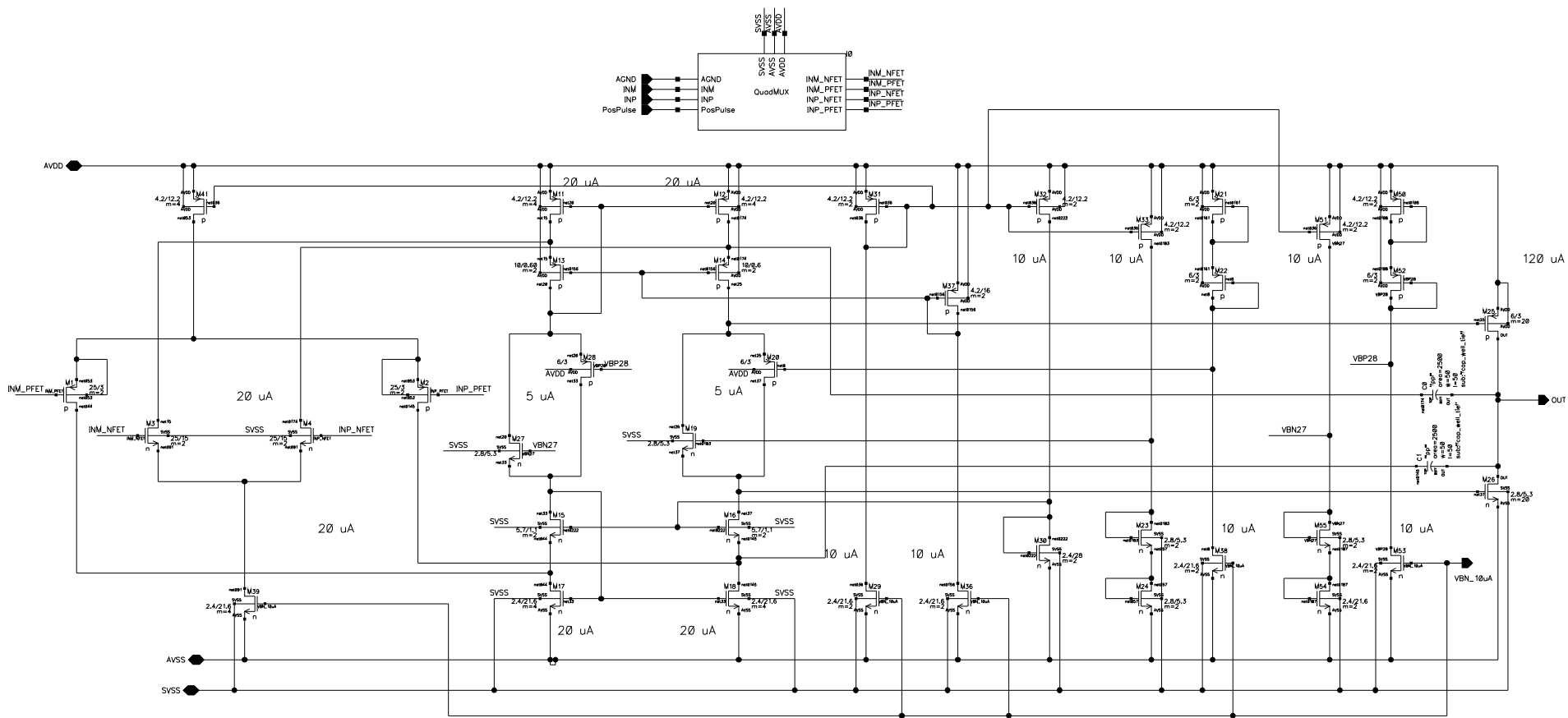
REV
1
CAGE NO.
DWG NO.

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

- a4
- AVDD
- AVSS
- SVSS
- AGND
- VCN_10uA
- PosPulse
- IN



UPDATED					
Oct 30 14:24:26 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET 1 OF 1	



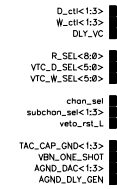
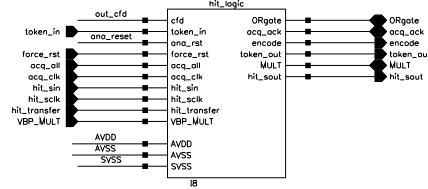
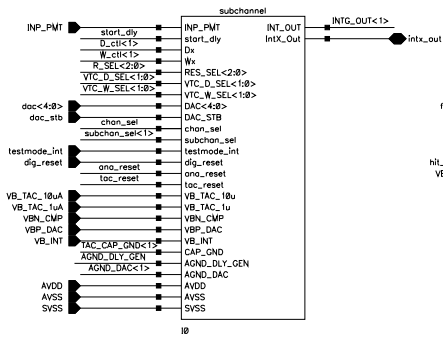
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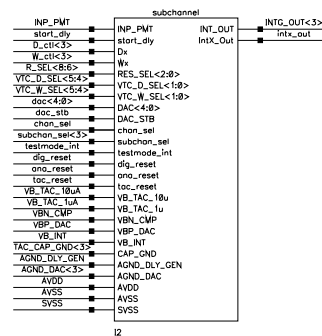
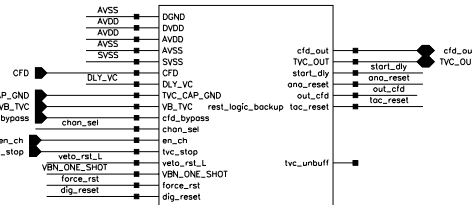
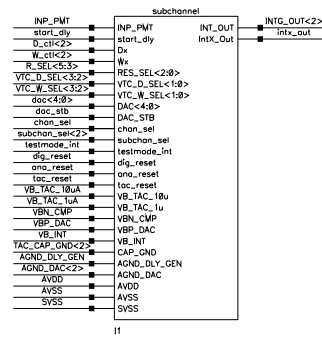
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1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



INTG_OUT<1:3>



UPDATED	SIUE IC Design Lab			
Mar 24 09:53:45 2010	Channel			
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	C			A
SCALE			SHEET	1 OF 1

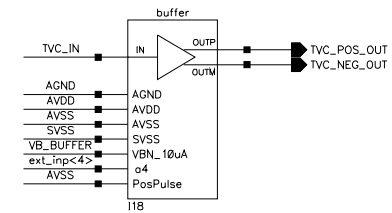
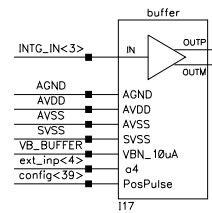
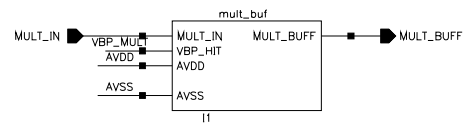
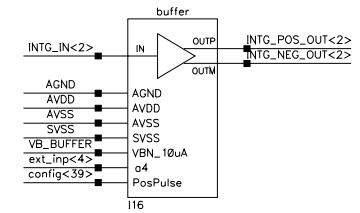
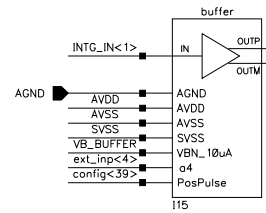
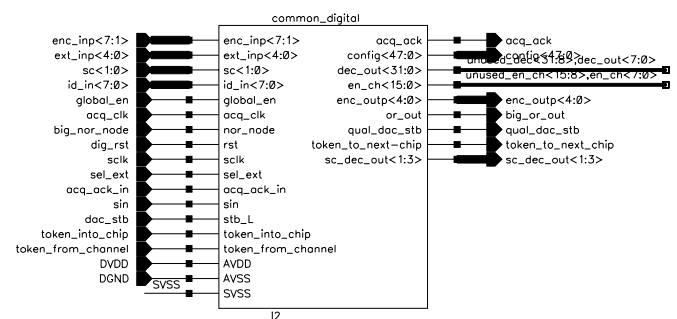
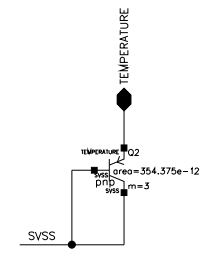
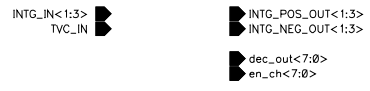
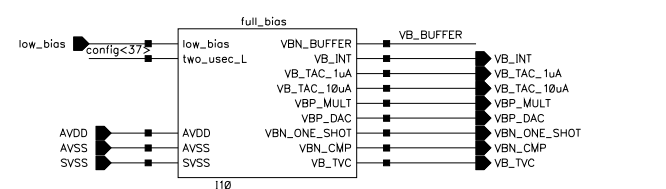
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3

2

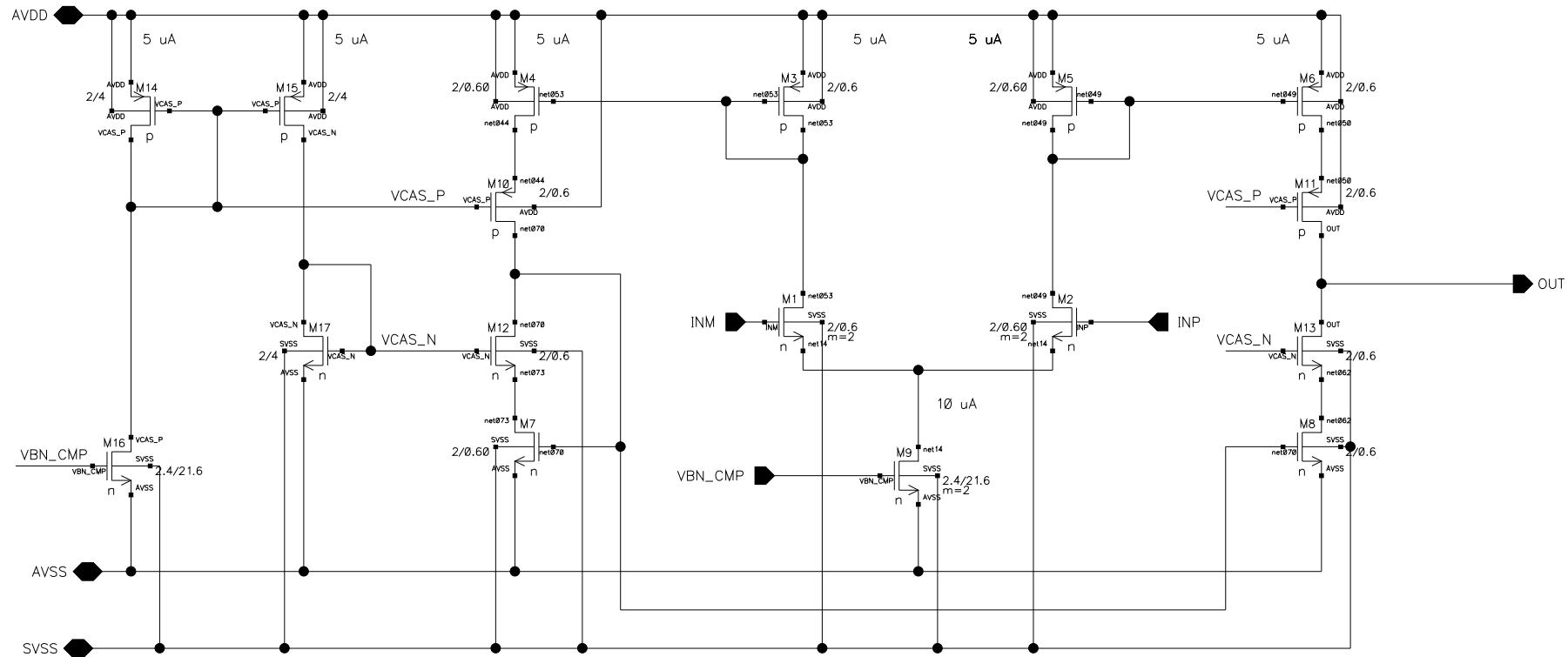
1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Mar 24 14:53:25 2010	SIUE IC Design Lab Common			
DRAWN				
CHECKED				
CHECKED	SIZE B	CAGE NO.	DWG NO.	REV A
ISSUED	SCALE	SHEET 1 OF 1		

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



Supply current is 30 uA.
Power consumption is 150 uWatts.

UPDATED	SIUE IC Design Lab Comparator			
Jul 9 10:40:35 2007				
DRAWN				
CHECKED				
CHECKED				
ISSUED	SIZE A	CAGE NO.	DWG NO.	REV
SCALE			SHEET 1 OF 1	

CAGE NO.

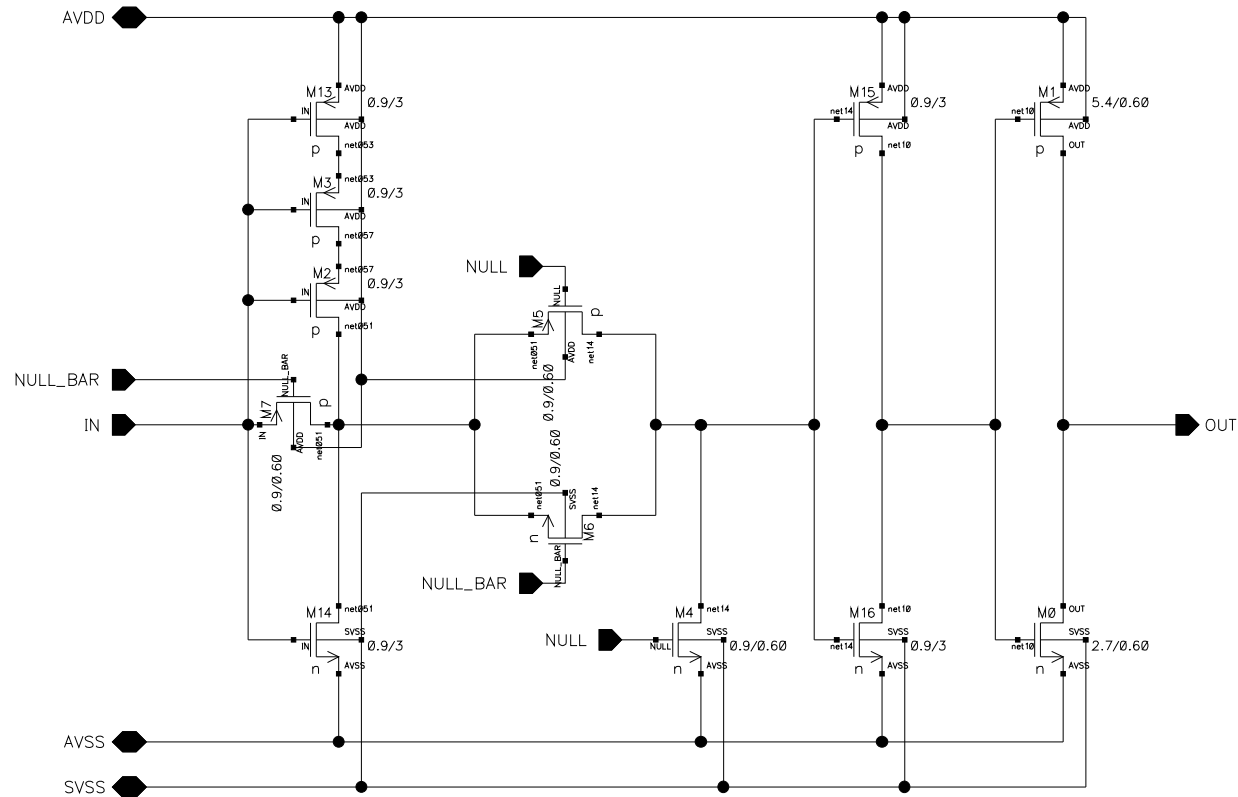
DWG NO.

SH 1

REV A

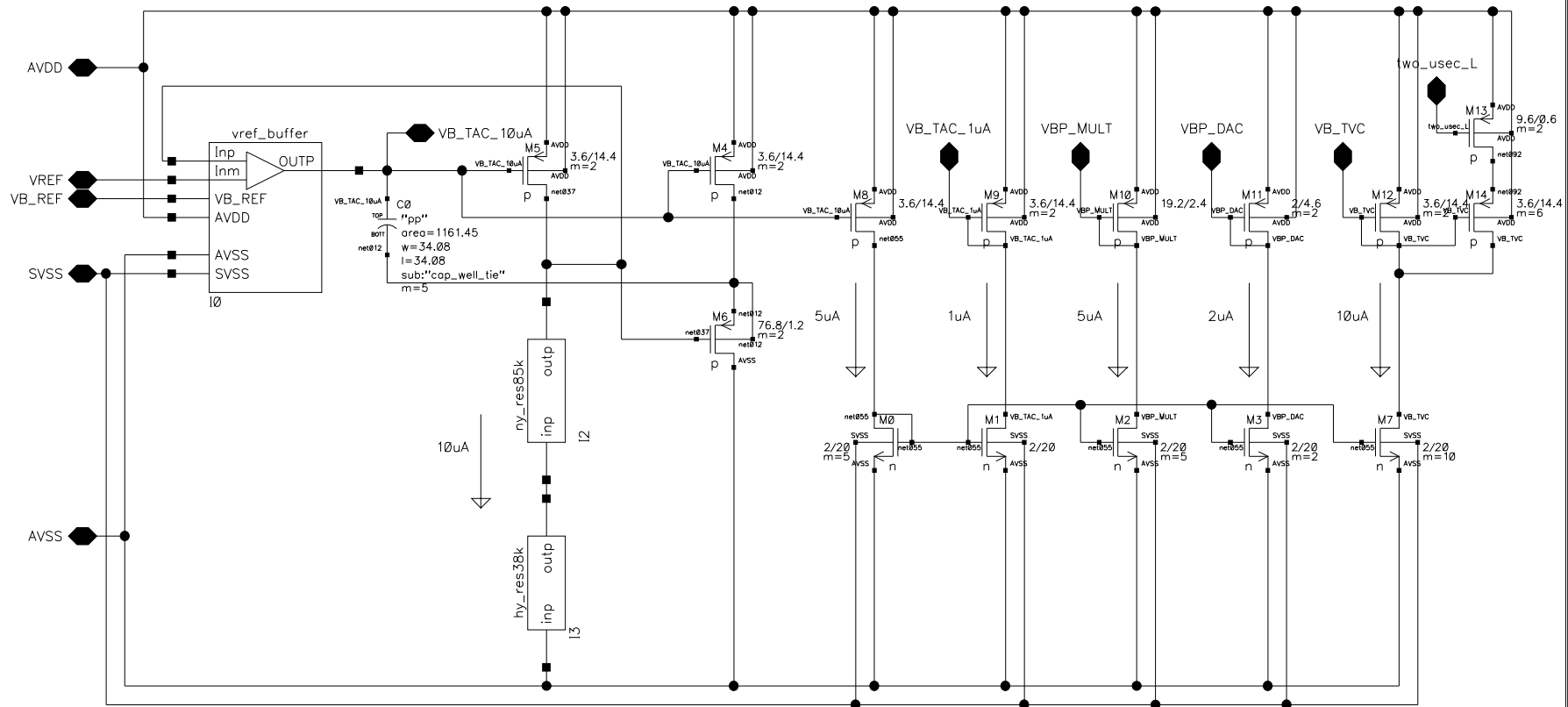
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



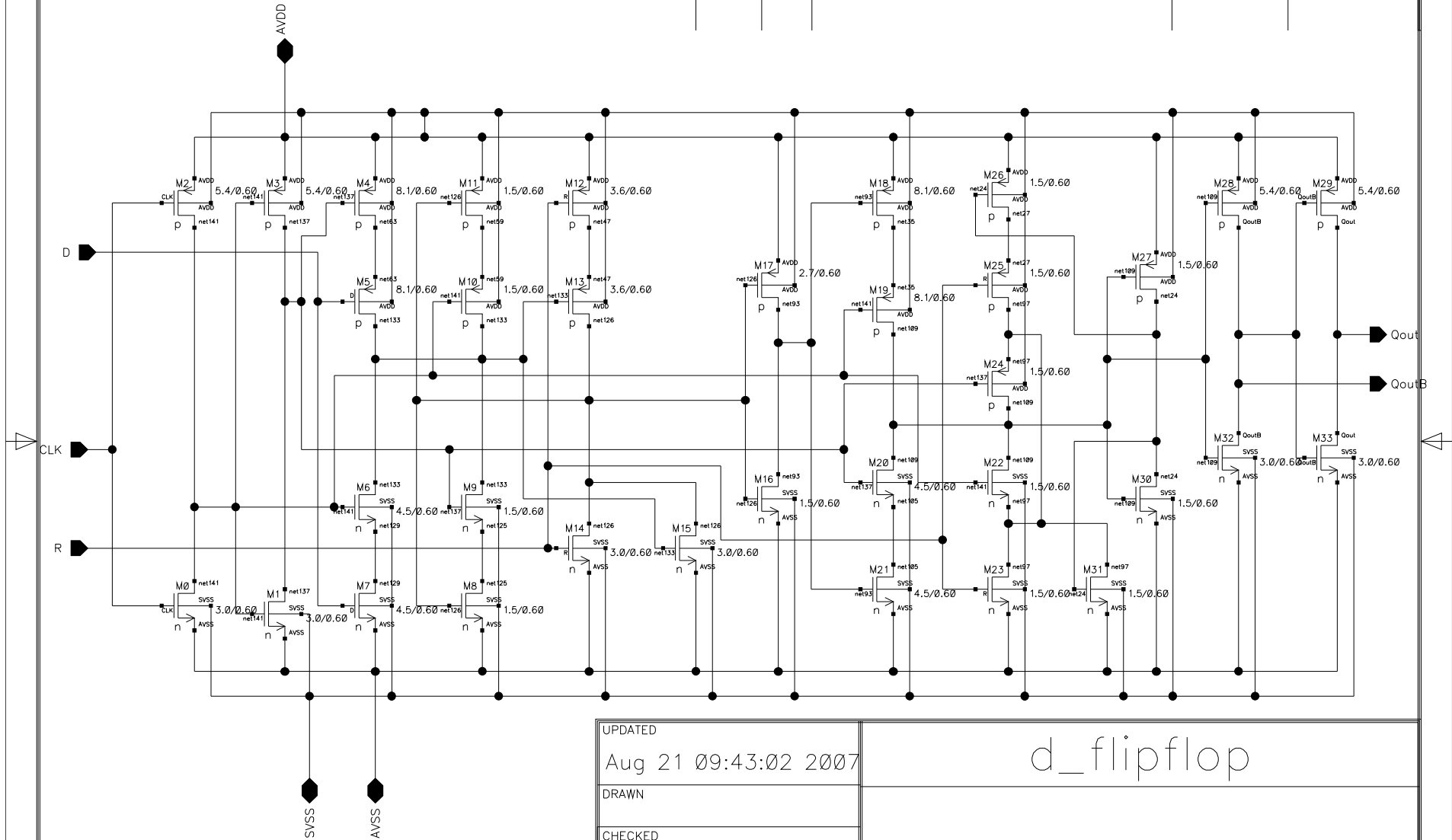
UPDATED		SIUE IC Design Lab Comparator Buffer & Invert			
Jul 10 13:06:58 2007					
DRAWN					
CHECKED					
CHECKED					
ISSUED		SIZE A	CAGE NO.	DWG NO.	REV A
		SCALE		SHEET	1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

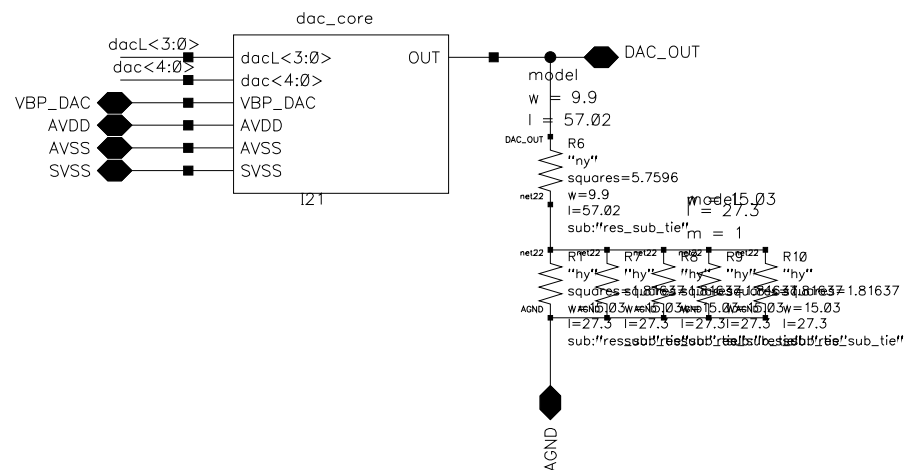
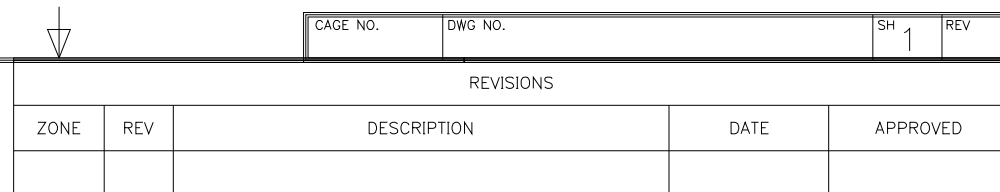


UPDATED		SIUE IC Design Lab Constant Current				
Oct 30 14:23:53 2007						
DRAWN						
CHECKED						
CHECKED		SIZE	CAGE NO.	DWG NO.		REV
		A				A
ISSUED		SCALE				SHEET 1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

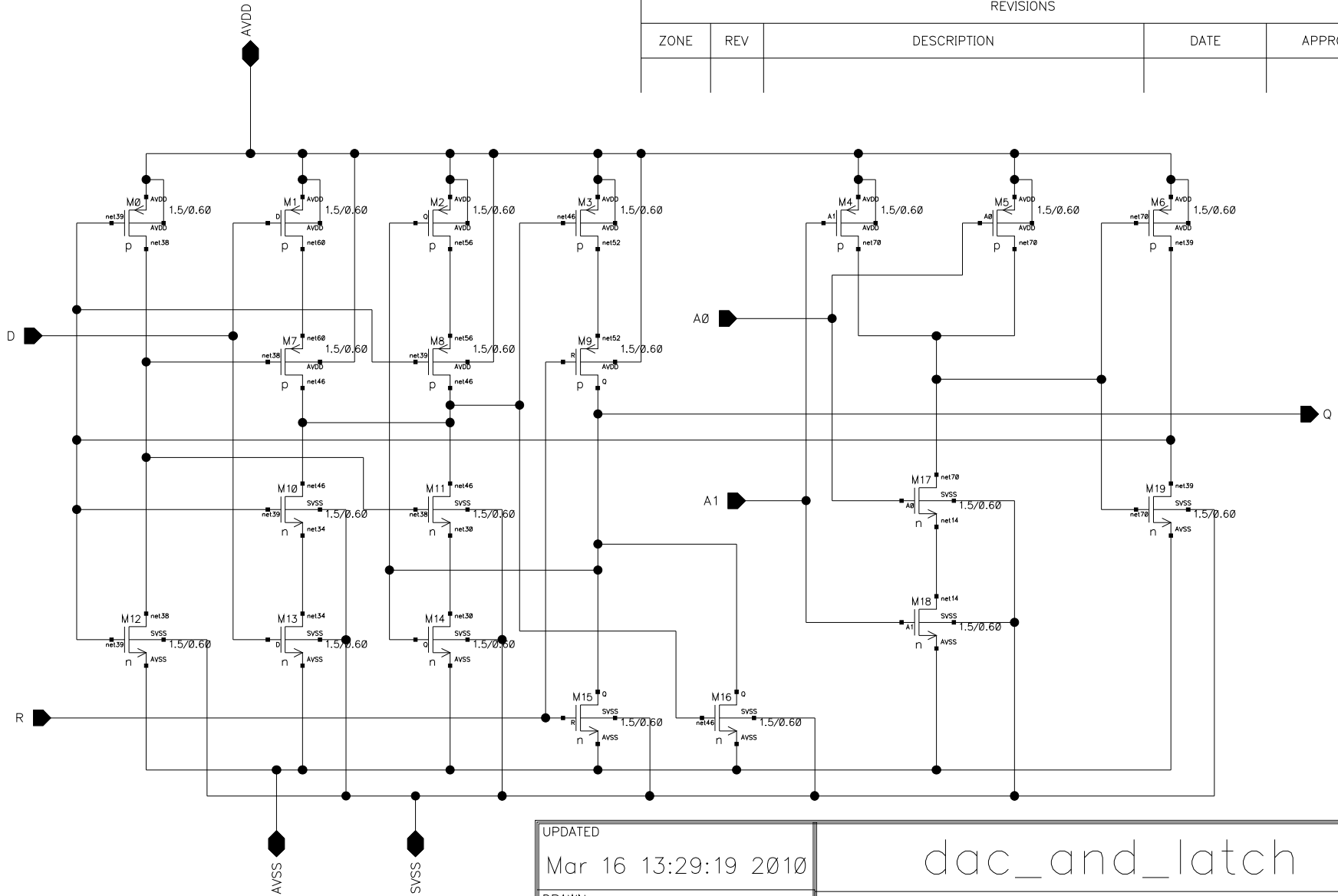


UPDATED Aug 21 09:43:02 2007	d_flipflop			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1



UPDATED				dac	
Mar 16 11:03:26 2010					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.		REV
ISSUED	SCALE			SHEET	1 OF 1

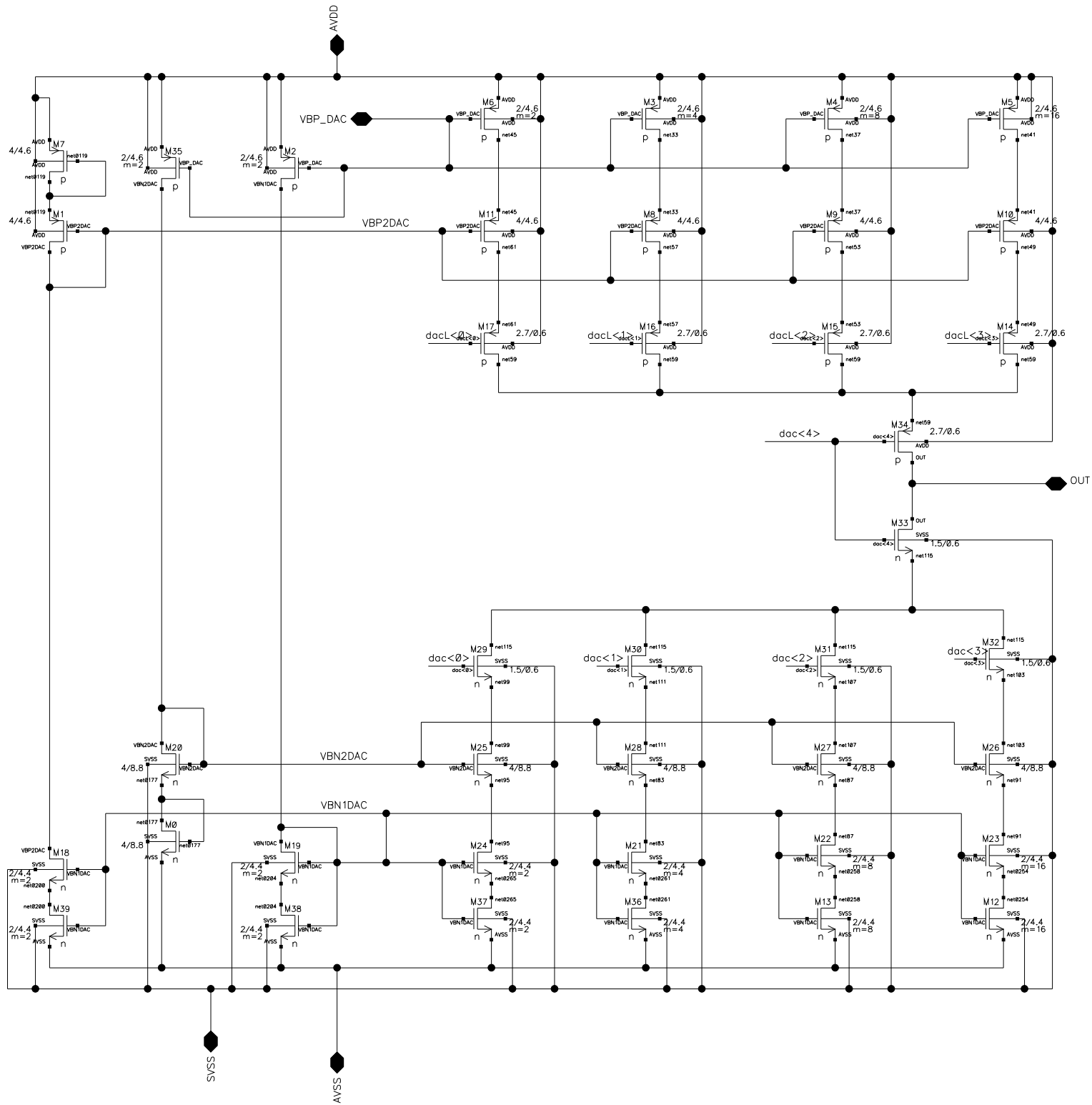
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



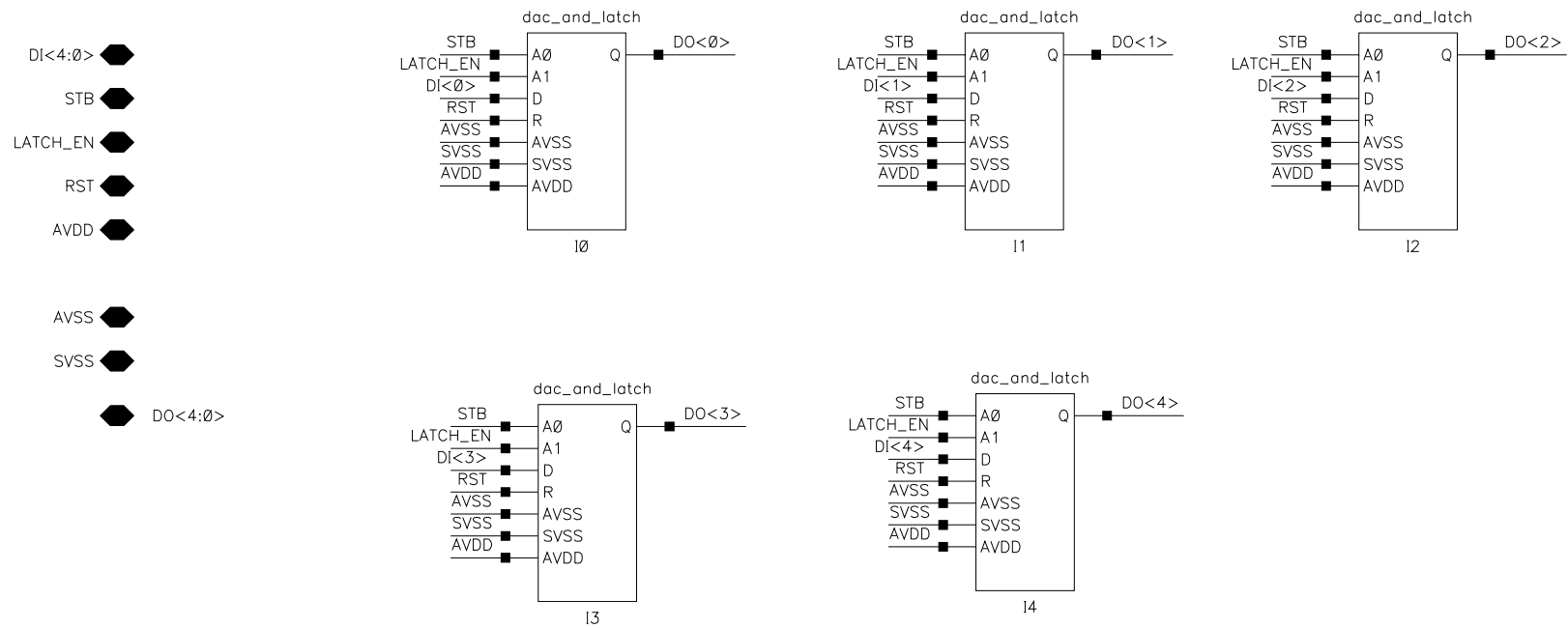
UPDATED Mar 16 13:29:19 2010		dac_and_latch			
DRAWN					
CHECKED					
CHECKED		SIZE A	CAGE NO.	DWG NO.	REV
ISSUED		SCALE	SHEET 1 OF 1		

dacL<3:0>

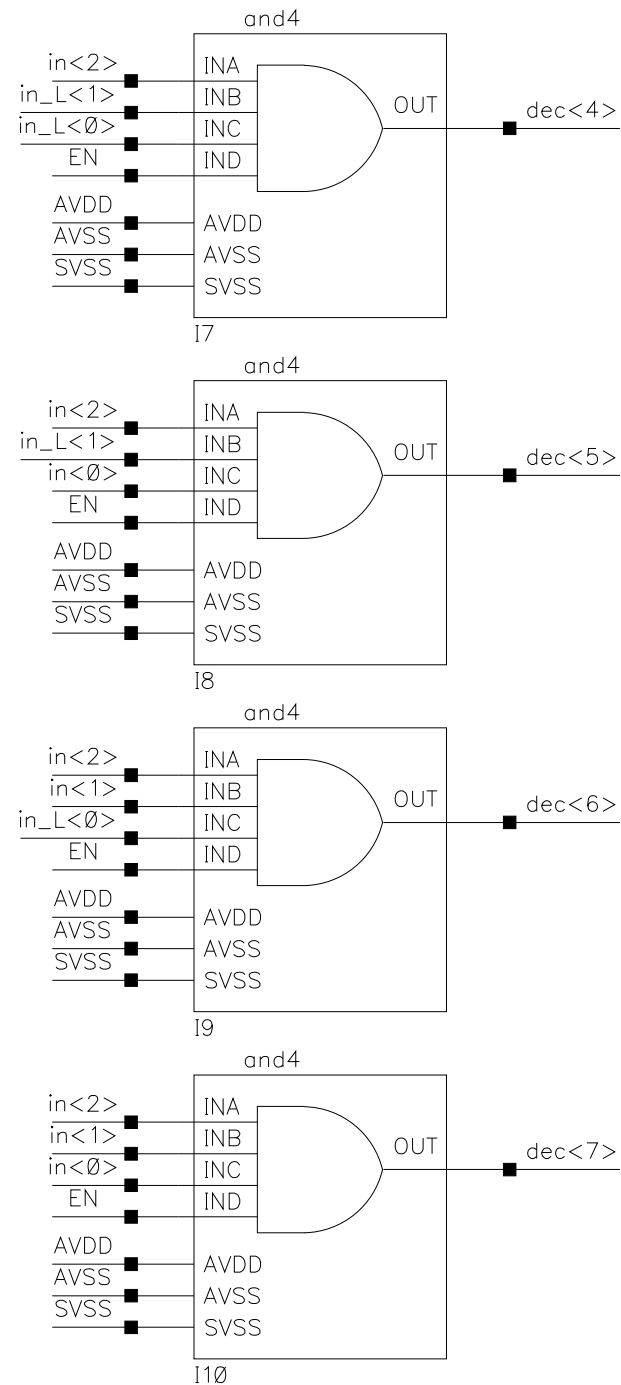
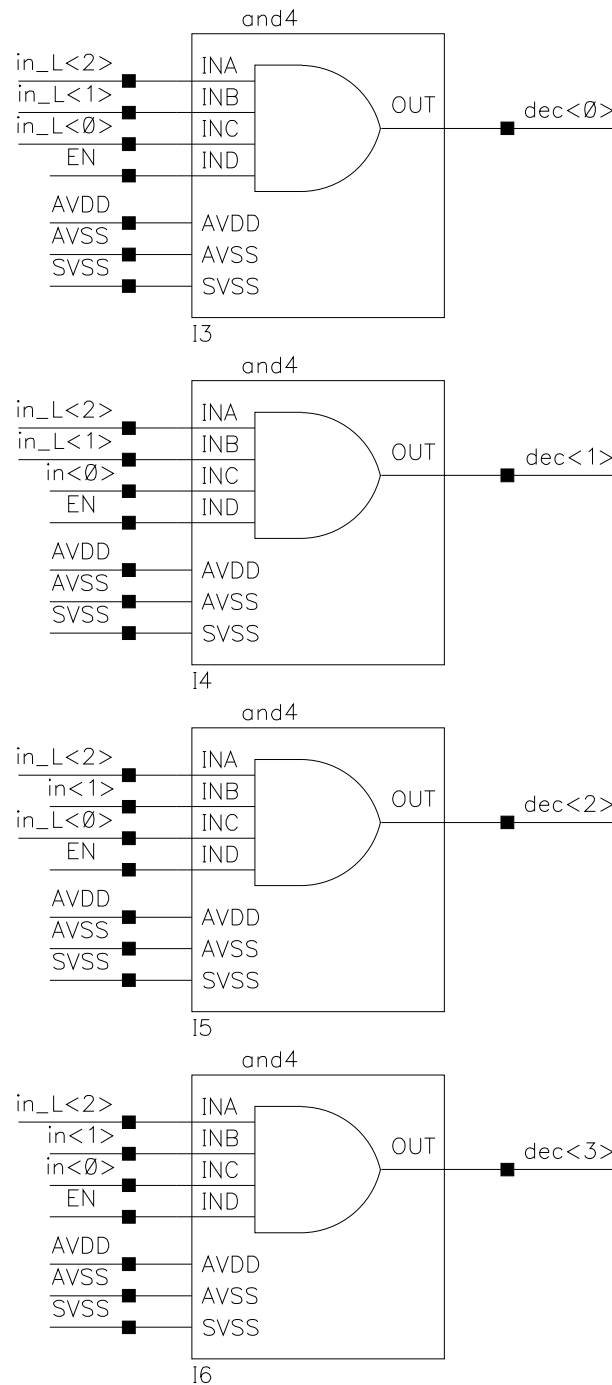
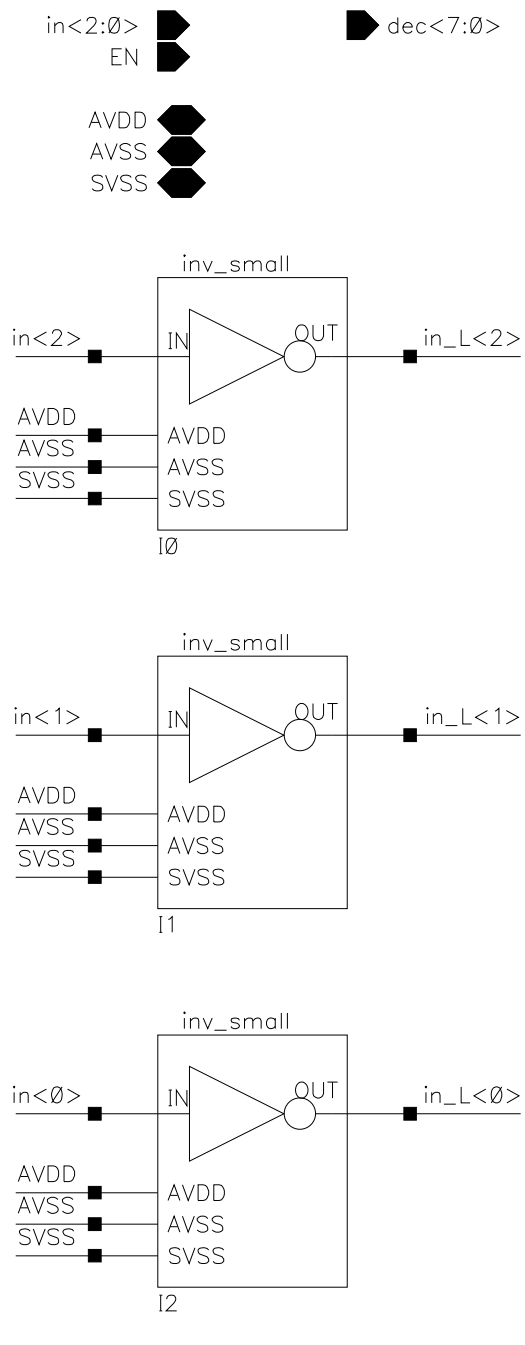
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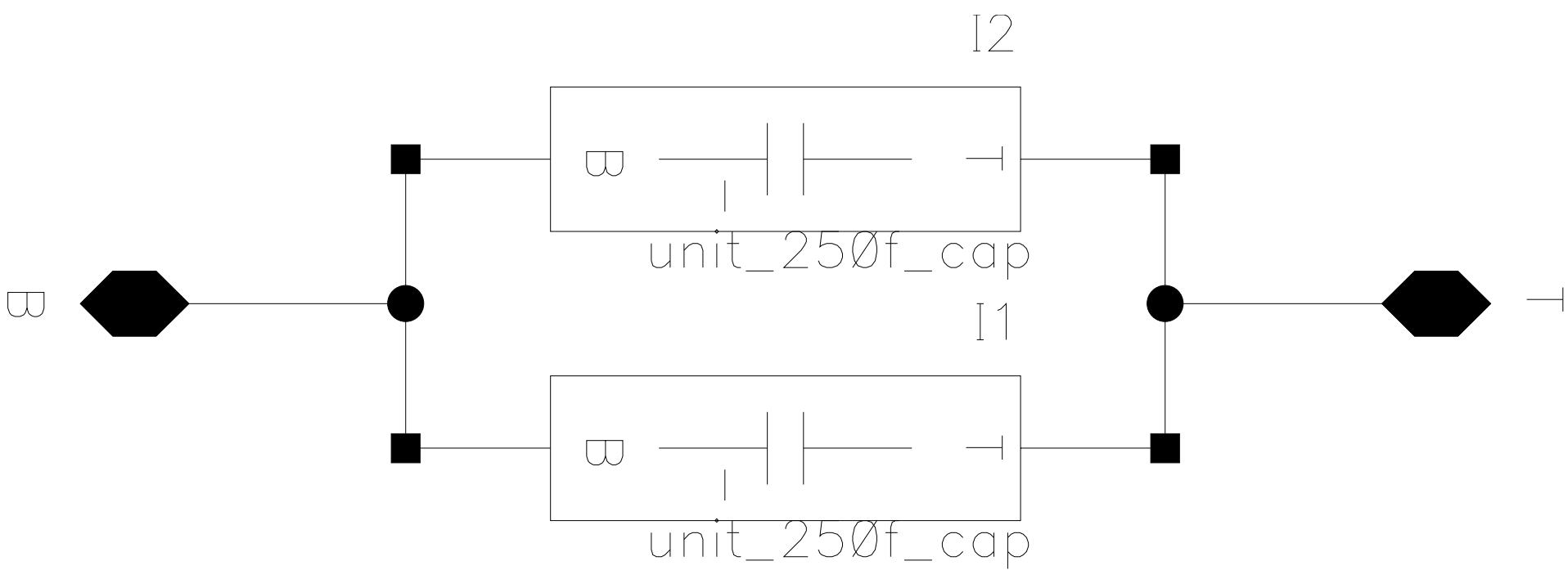


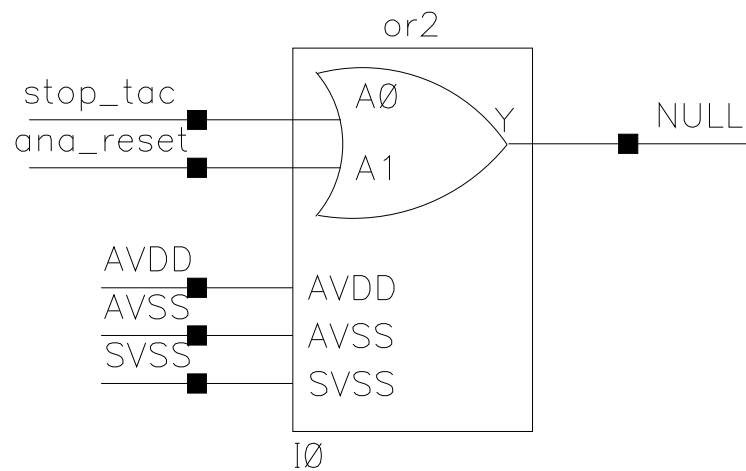
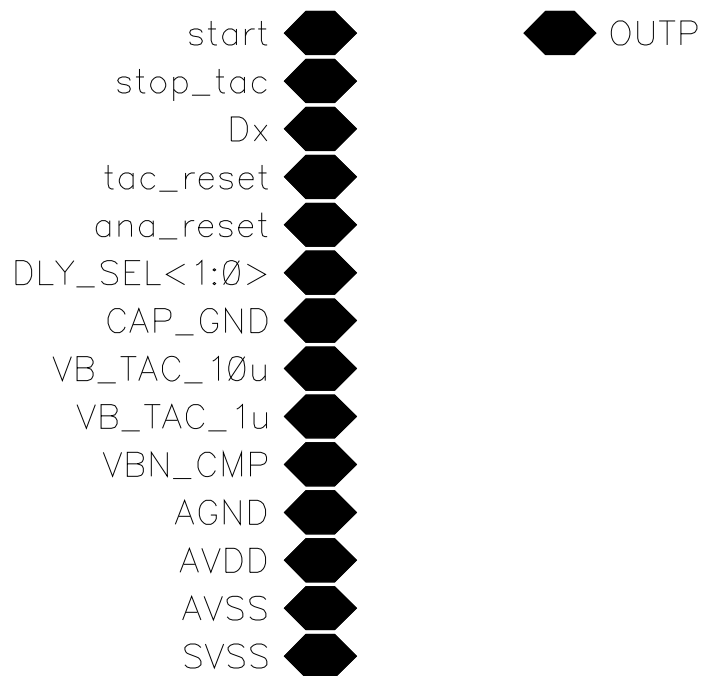
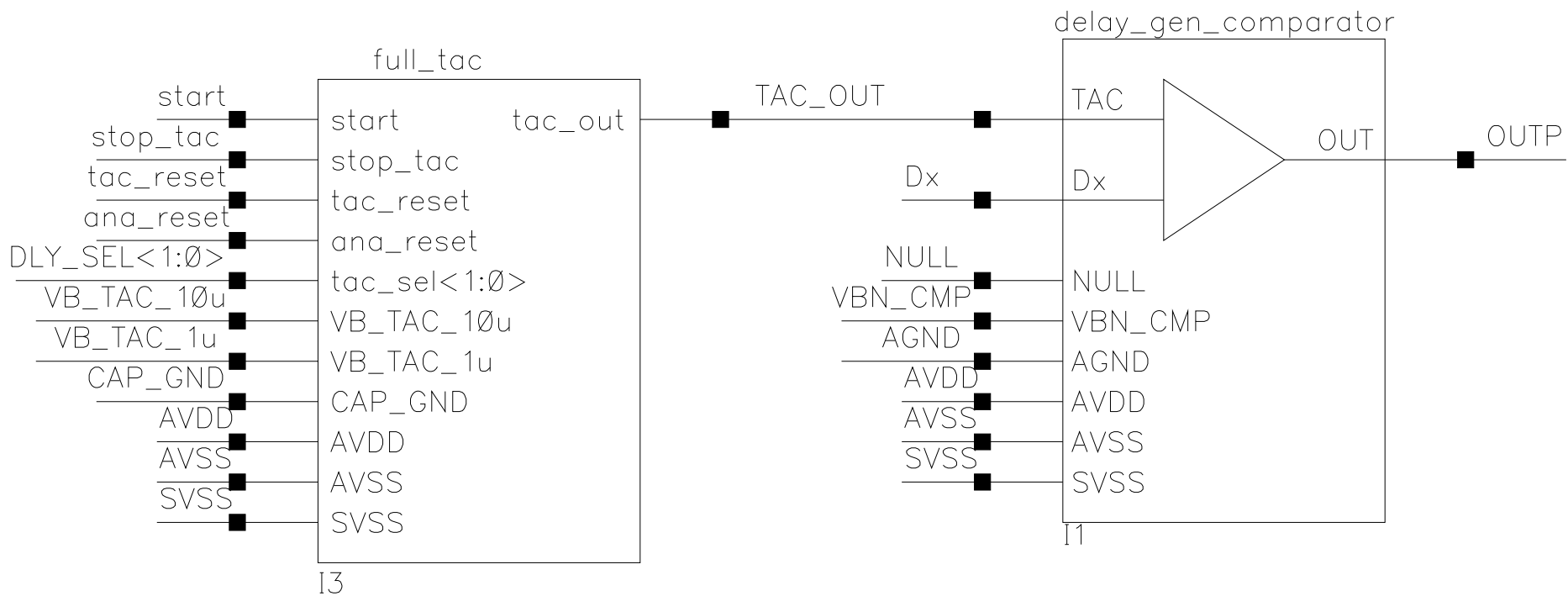
CAGE NO.		DWG NO.		SH 1	REV
REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED



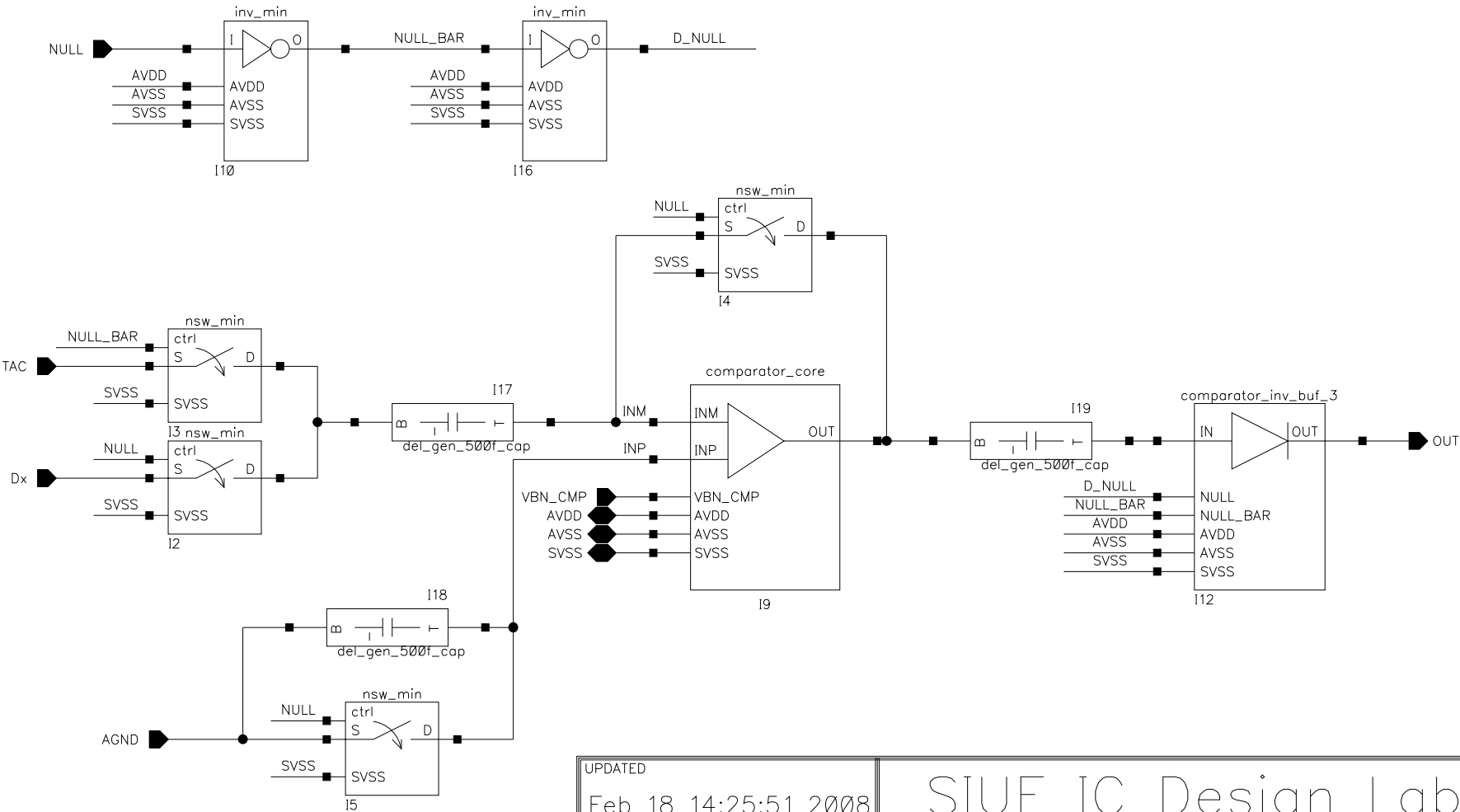
UPDATED		le_dac_reg			
Mar 16 13:32:09 2010					
DRAWN					
CHECKED					
CHECKED		SIZE	CAGE NO.	DWG NO.	REV
ISSUED		A			
		SCALE		SHEET	1 OF 1





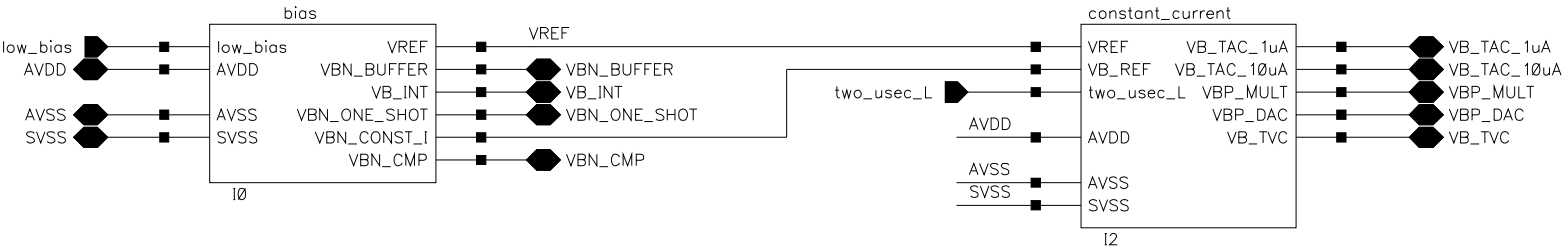


		CAGE NO.	DWG NO.	SH 1	REV A
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



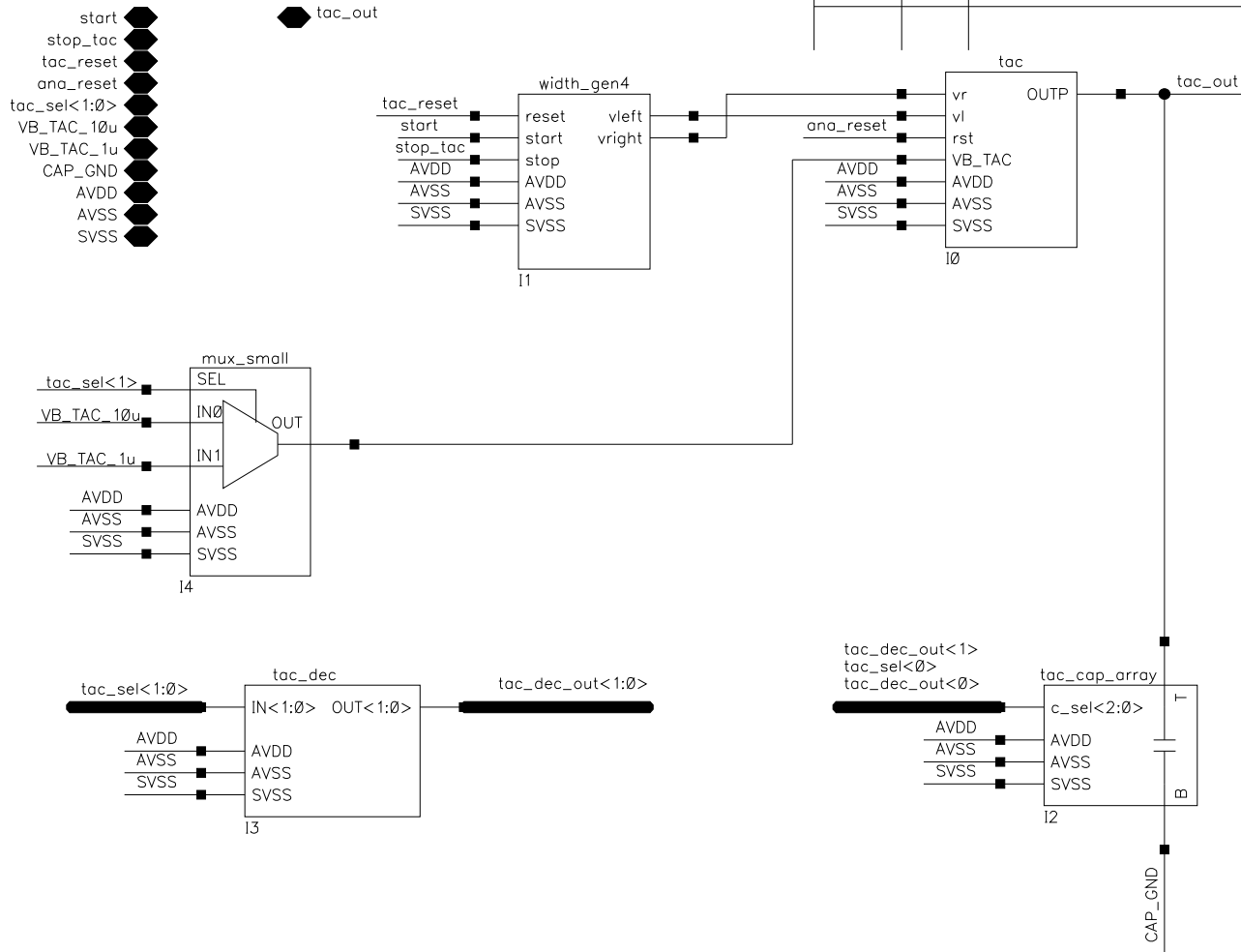
UPDATED		SIUE IC Design Lab Delay Gen Comparator			
Feb 18 14:25:51 2008					
DRAWN					
CHECKED					
CHECKED					
ISSUED		SIZE A	CAGE NO.	DWG NO.	REV A
		SCALE			SHEET 1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	full_bias				
Oct 30 14:17:59 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

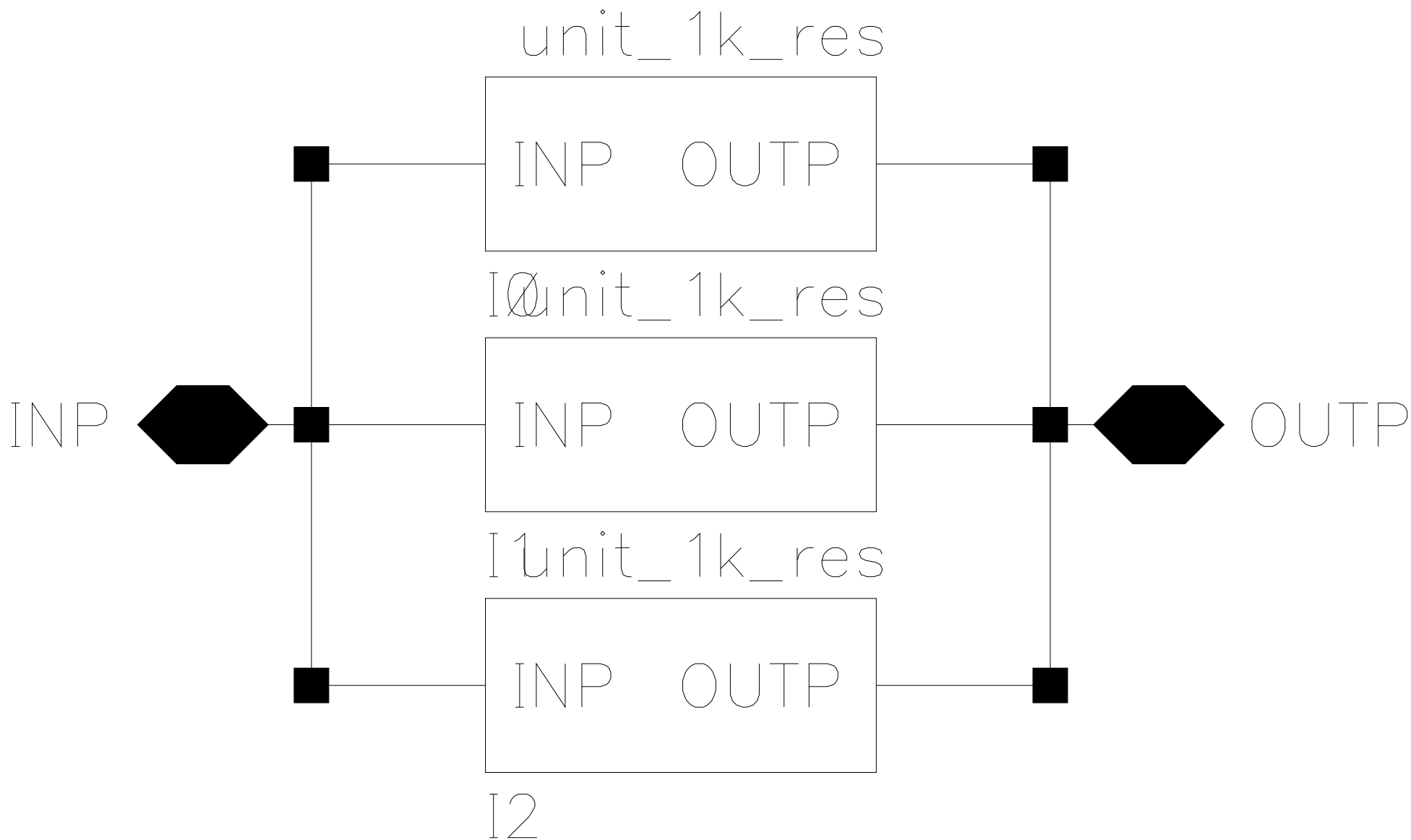
		CAGE NO.	DWG NO.	SH 1	REV
REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED

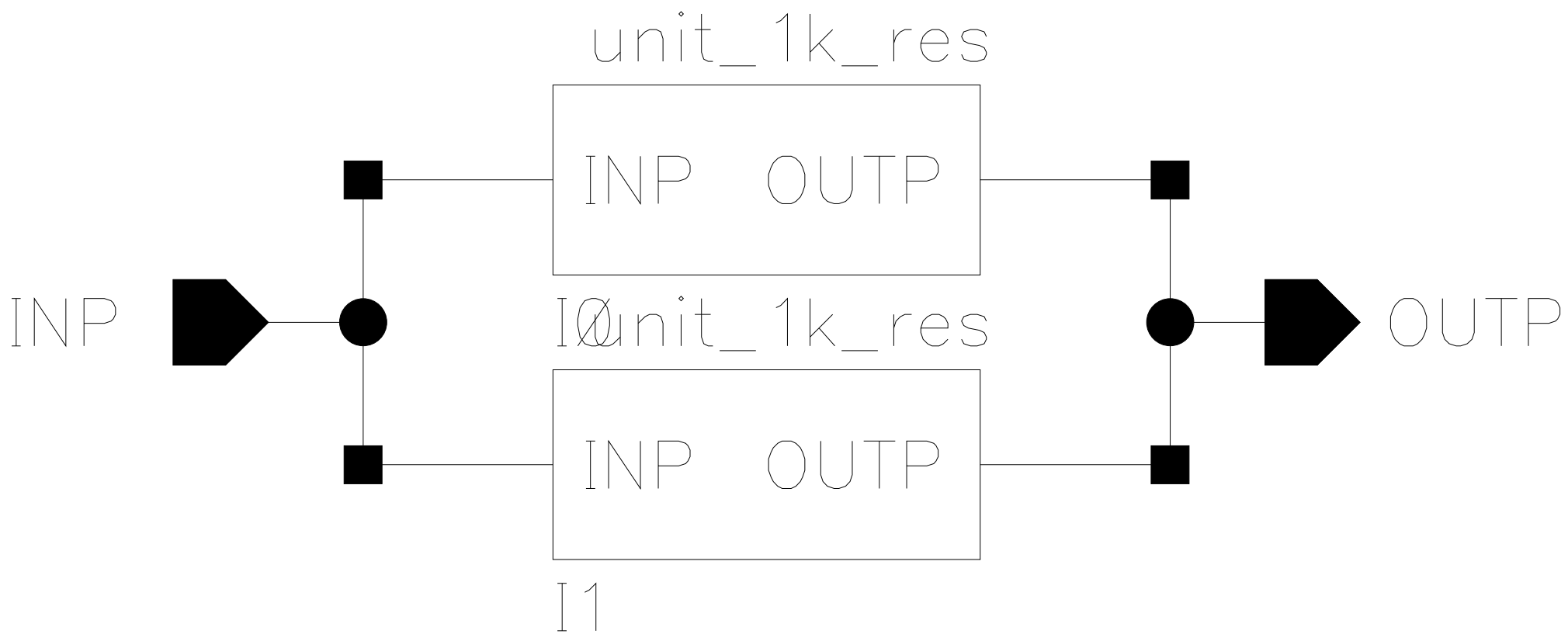


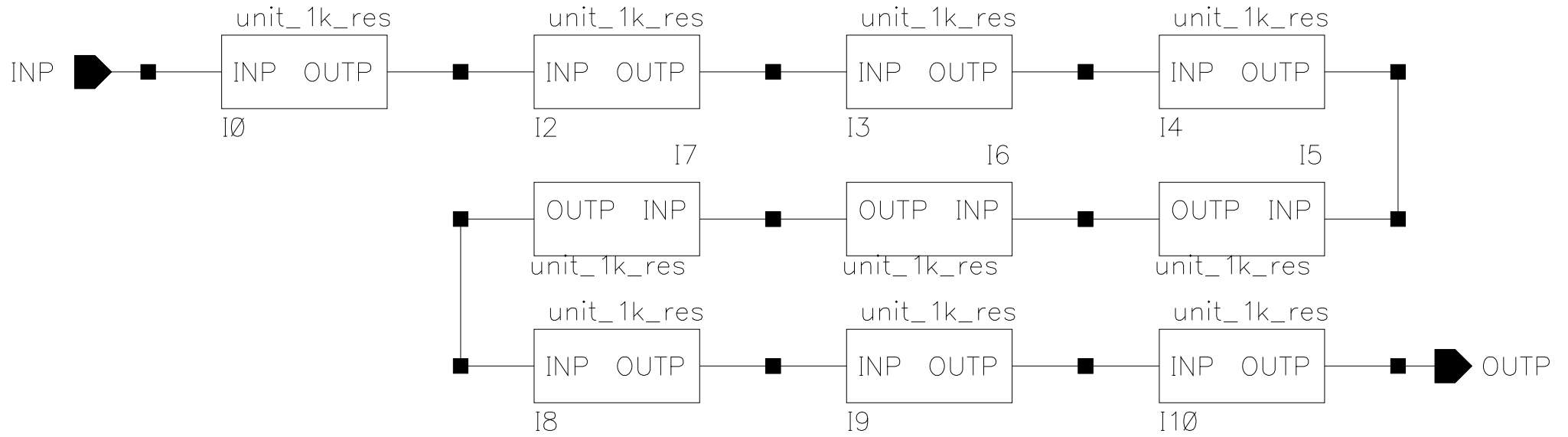
tac_sel	I (uA)	C (pf)	Tmax (ns)	Tmin (ns)
00	10	0.2	50	5
01	10	1.0	250	25
10	1	0.6	1500	150
11	1	4.0	10000	1000

Note: Assume Vmax = 2.5 and Vmin = 0.25

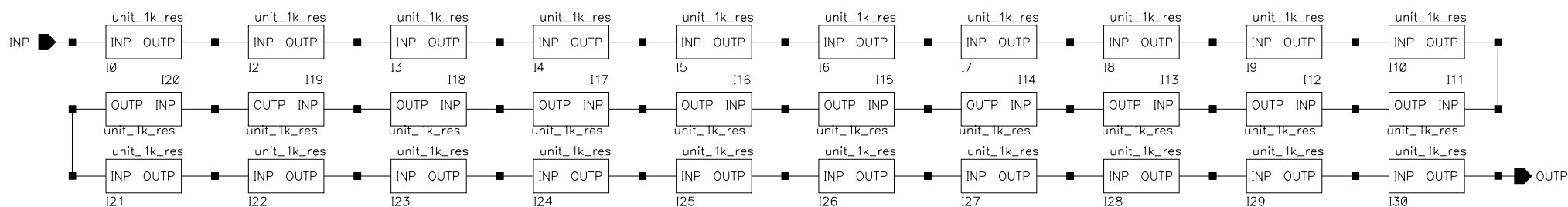
UPDATED	full_tac			
Jul 9 12:33:14 2007				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

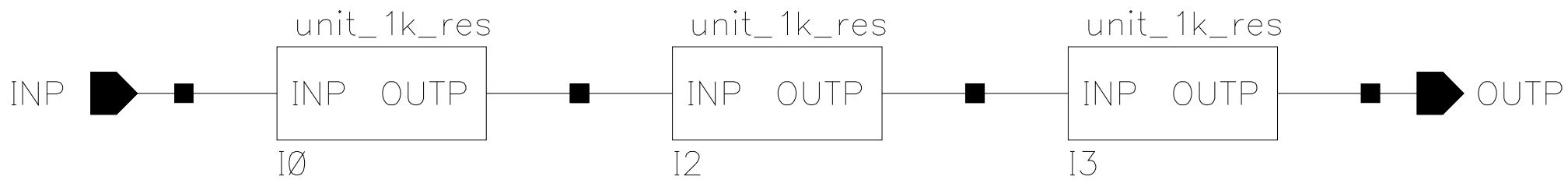


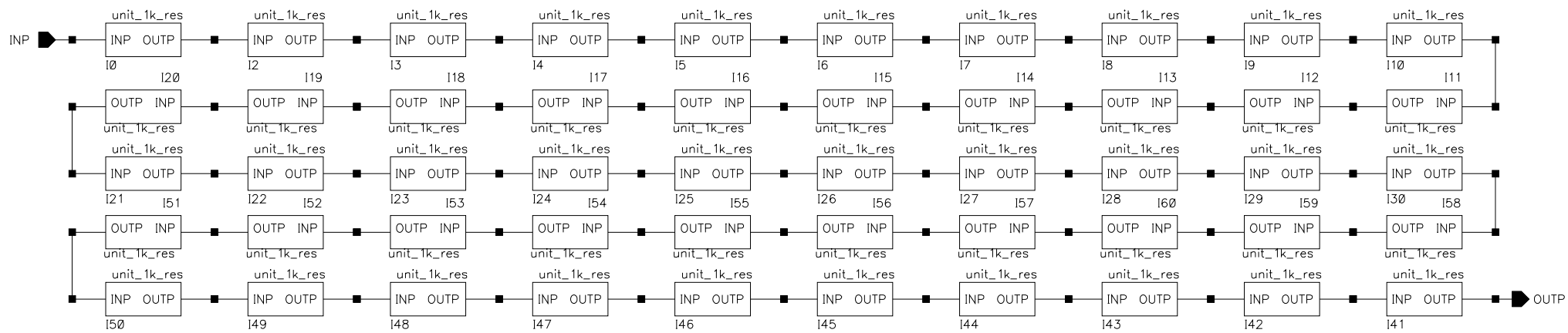


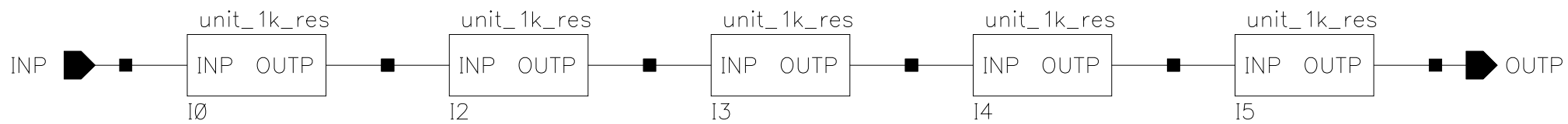








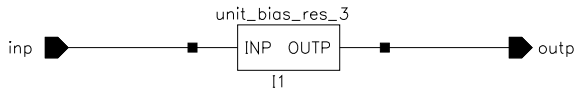






CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



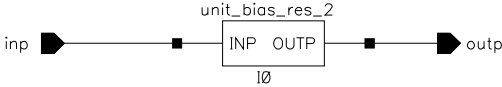
UPDATED	hy_res0_59k			
Oct 30 15:50:11 2007				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	A			
SCALE		SHEET 1 OF 1		





CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



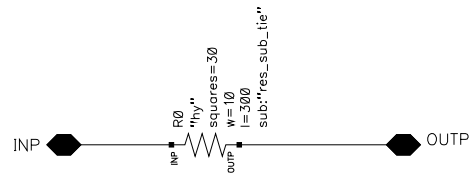
UPDATED	hy_res17k			
Oct 30 15:36:28 2007				
DRAWN				
CHECKED				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	A			
	SCALE		SHEET	1 OF 1





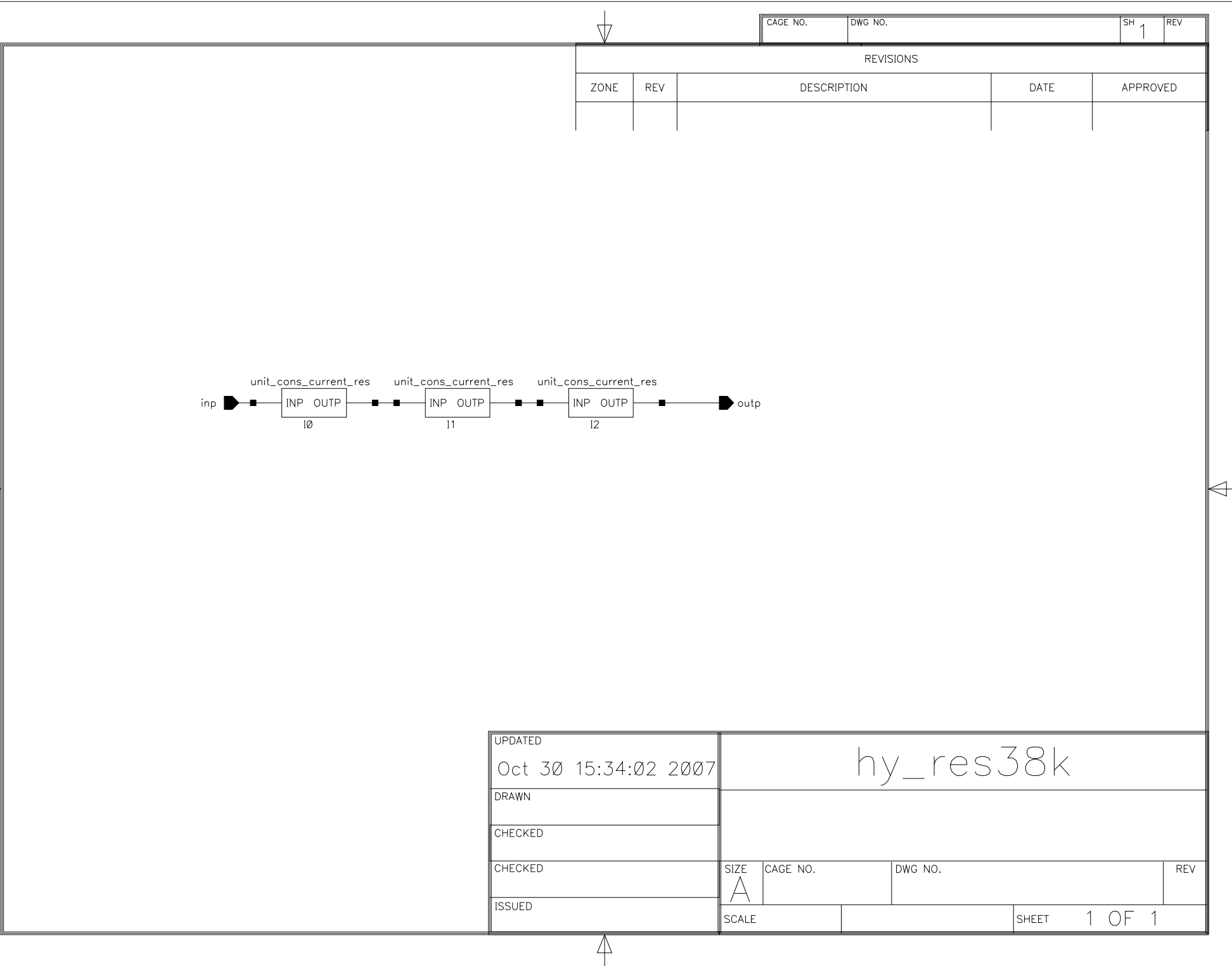
CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	hy_res30k			
Aug 16 14:34:22 2007				
DRAWN				
CHECKED				
CHECKED				
CHECKED				
ISSUED	SIZE A	CAGE NO.	DWG NO.	REV
	SCALE		SHEET	1 OF 1







CAGE NO.

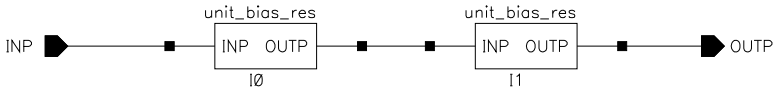
DWG NO.

SH 1

REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

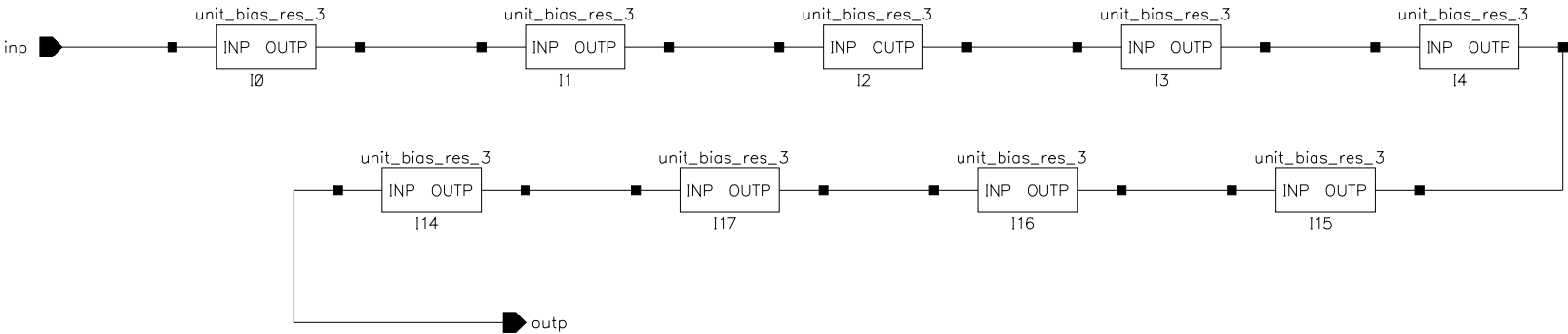


UPDATED
Oct 30 15:36:07 2007
DRAWN
CHECKED
CHECKED
ISSUED

hy_res5k			
SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE			SHEET 1 OF 1

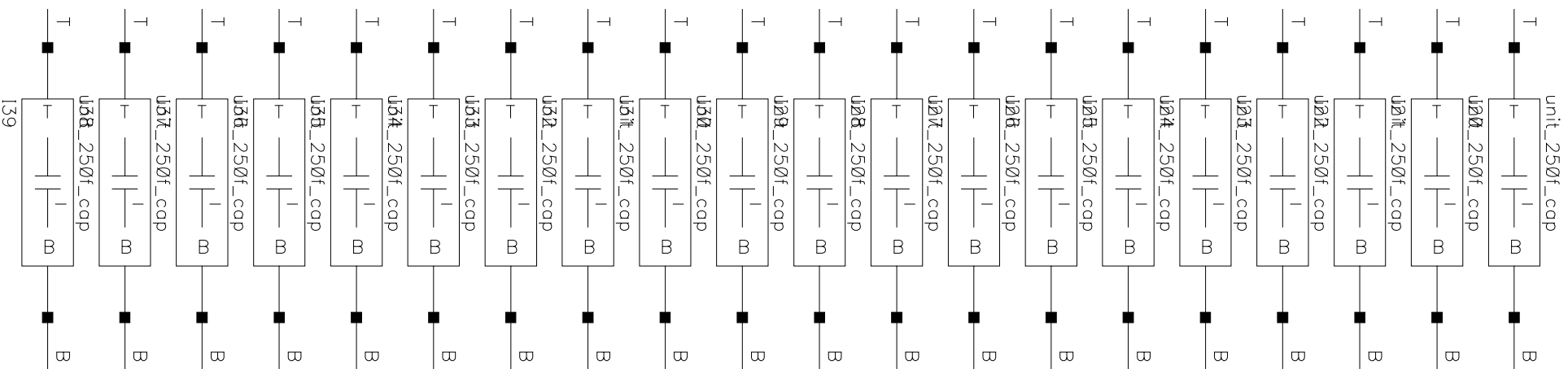
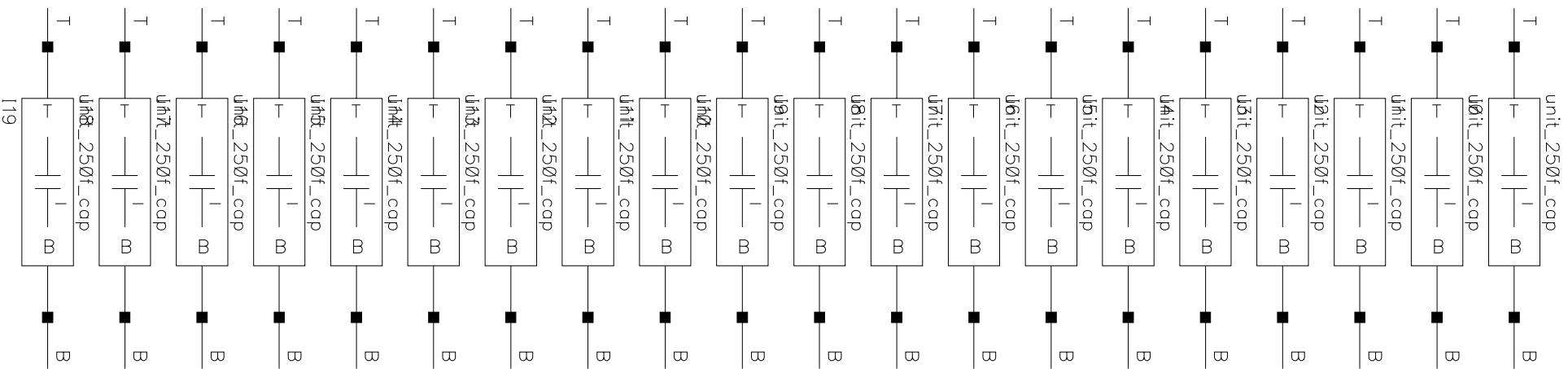


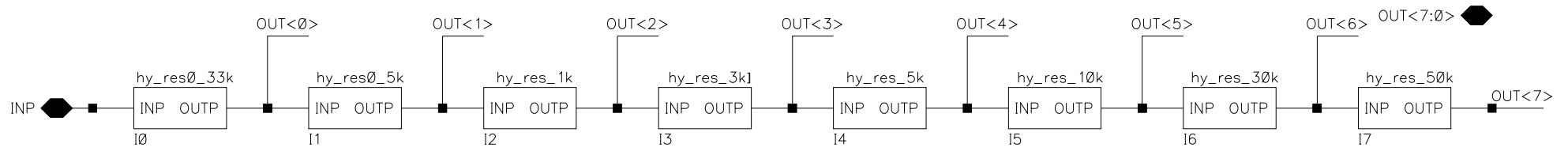
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	hy_res9x0_59k				
Oct 30 15:37:15 2007					
DRAWN					
CHECKED					
CHECKED					
ISSUED	SIZE A	CAGE NO.	DWG NO.	REV	
SCALE		SHEET 1 OF 1			





Output	Resistance
OUT<0>	0.5 K
OUT<1>	1 K
OUT<2>	2 K
OUT<3>	5 K
OUT<4>	10 K
OUT<5>	20 K
OUT<6>	50 K
OUT<7>	100 K

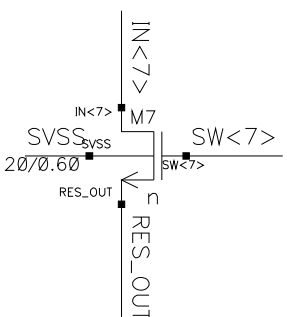
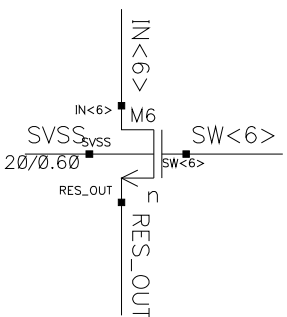
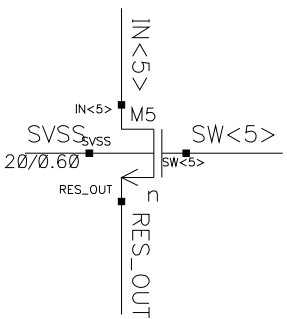
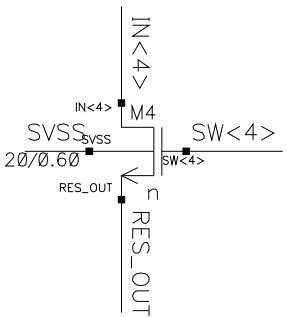
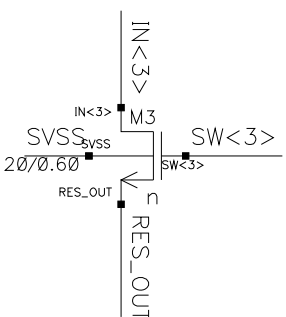
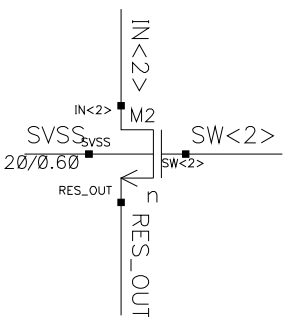
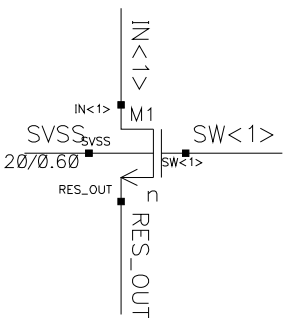
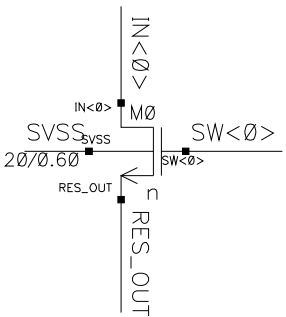
Resistances include the switch resistance following the resistor array.

IN<7:0>
SW<7:0>
chan_sel
DUMP
AVDD
AVSS
SVSS

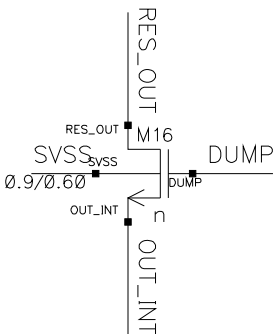
OUT_INT
RES_OUT
INT_OUT

Switch	Resistance
SW<0>	0.5 K
SW<1>	1 K
SW<2>	2 K
SW<3>	5 K
SW<4>	10 K
SW<5>	20 K
SW<6>	50 K
SW<7>	100 K

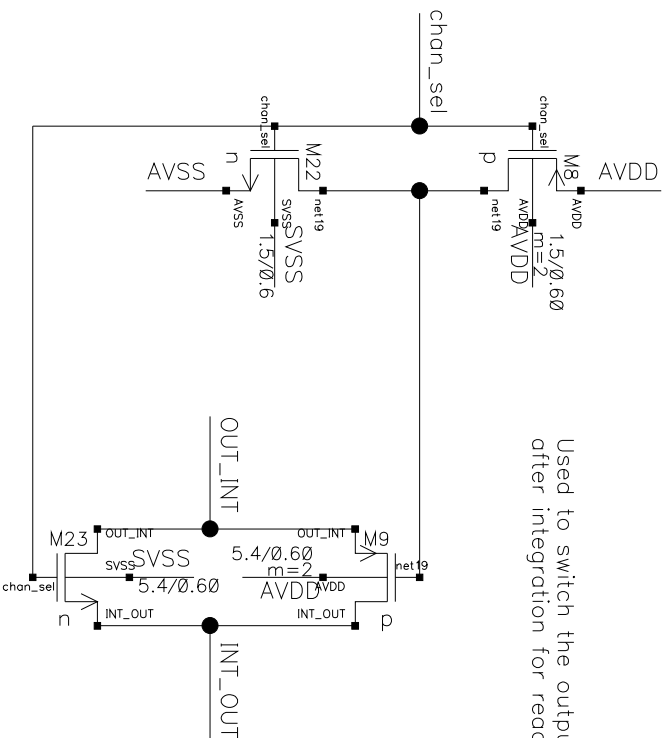
Resistances include the switch resistance and the resistor array preceding the switch.

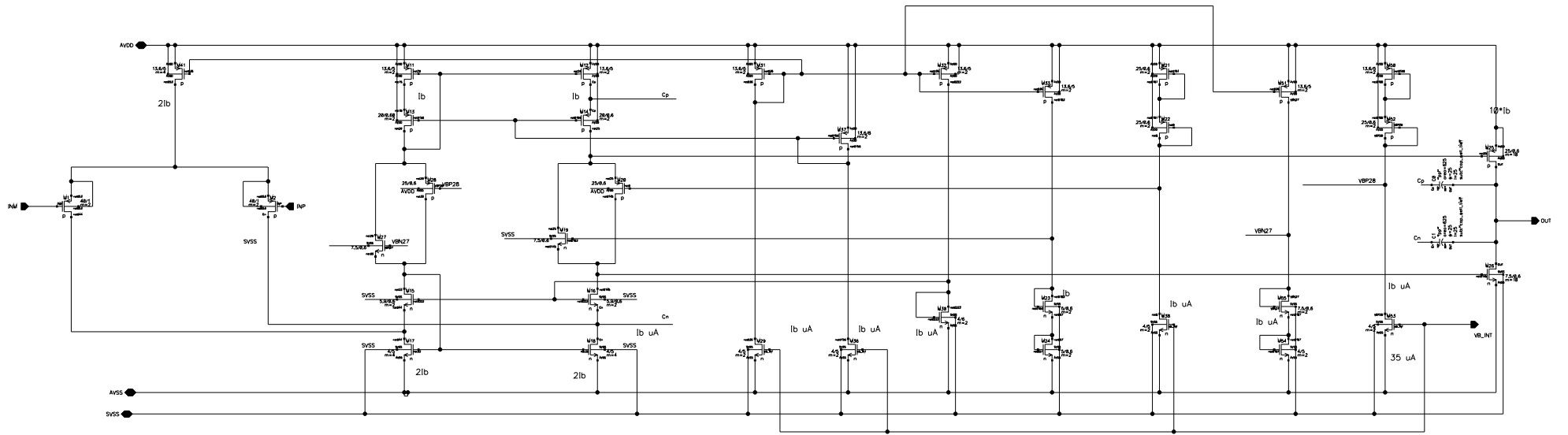


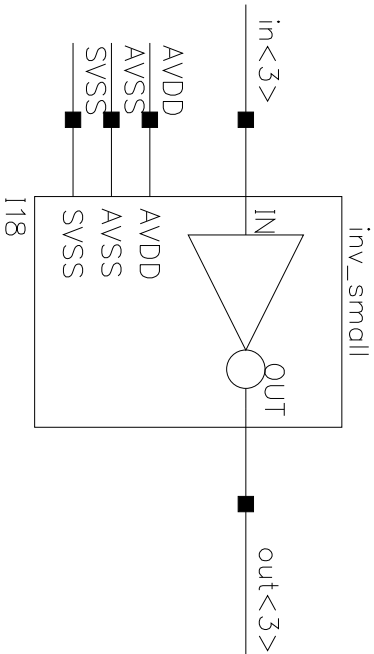
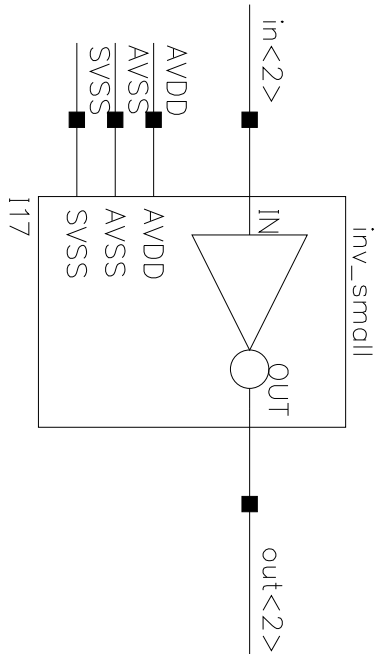
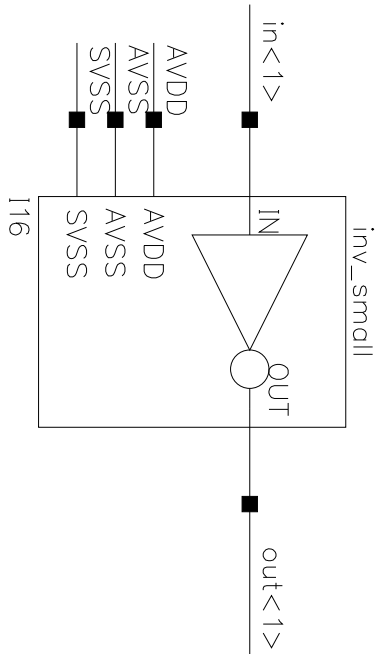
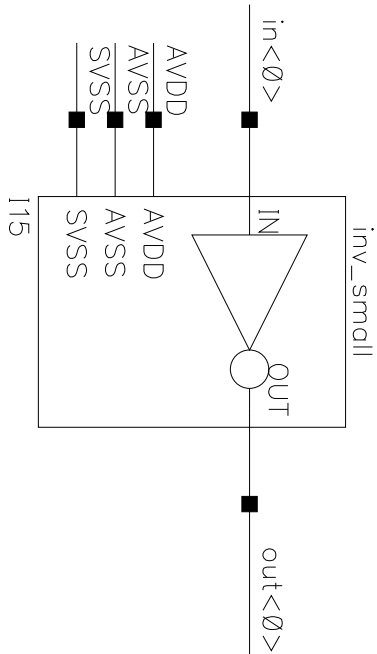
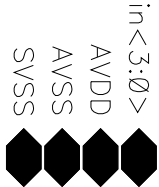
Used to short the integrating capacitor



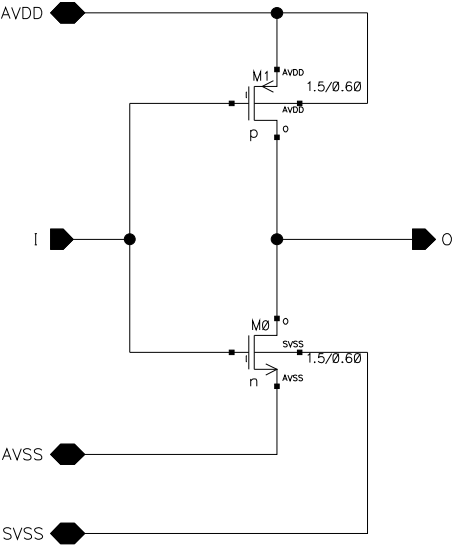
Used to switch the output of the OTA after integration for reading purposes.





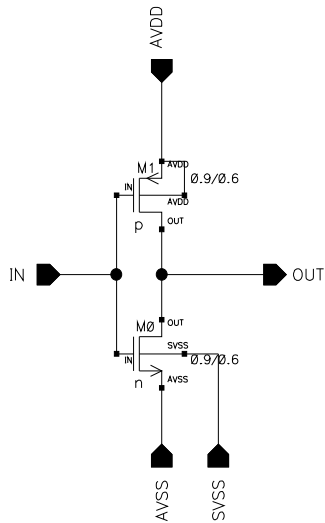


		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



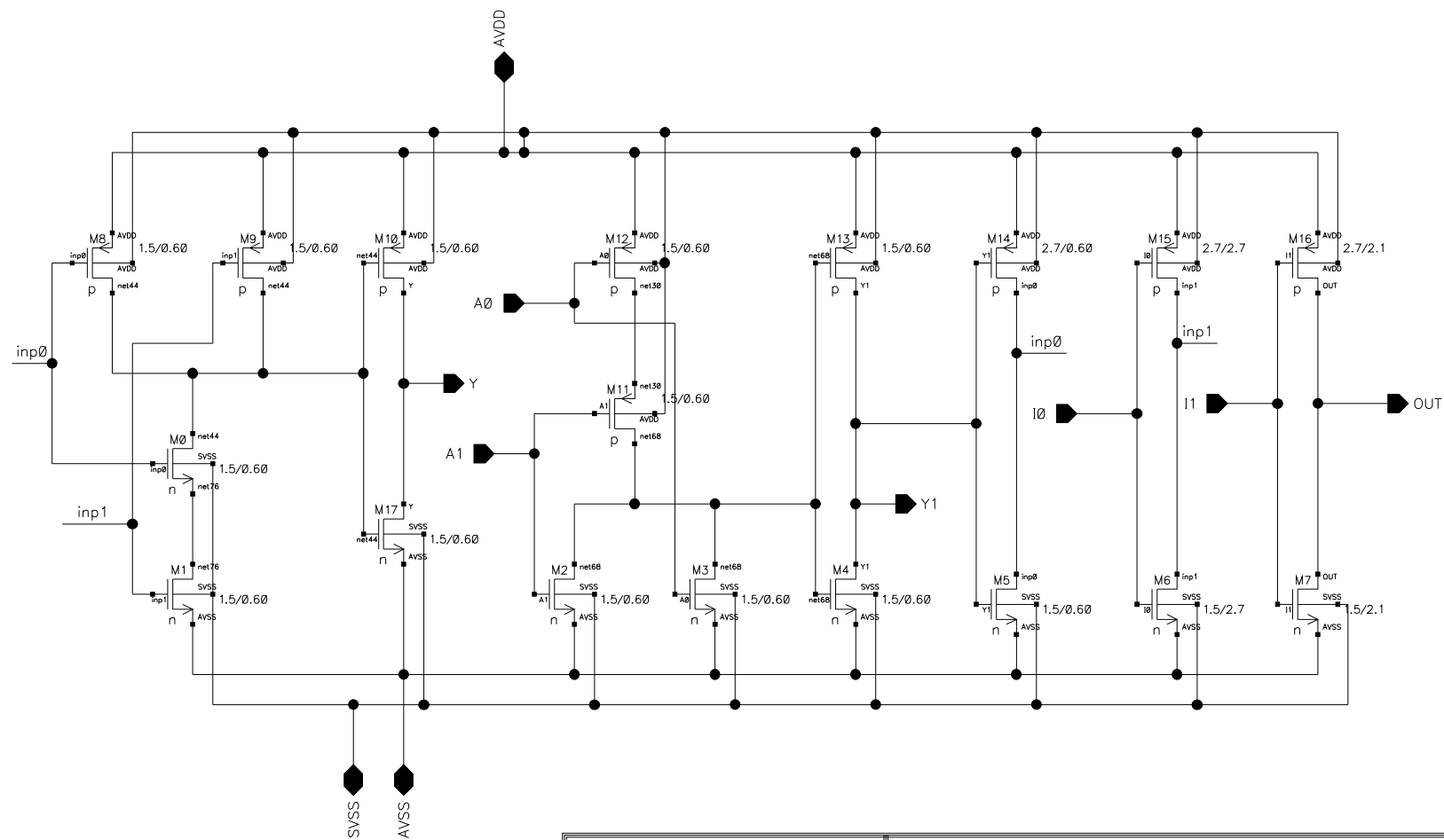
UPDATED	inv_min				
Jul 9 15:23:25 2007					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET 1 OF 1			

		CAGE NO.	DWG NO.		SH 1	REV
		REVISIONS				
ZONE	REV	DESCRIPTION		DATE	APPROVED	



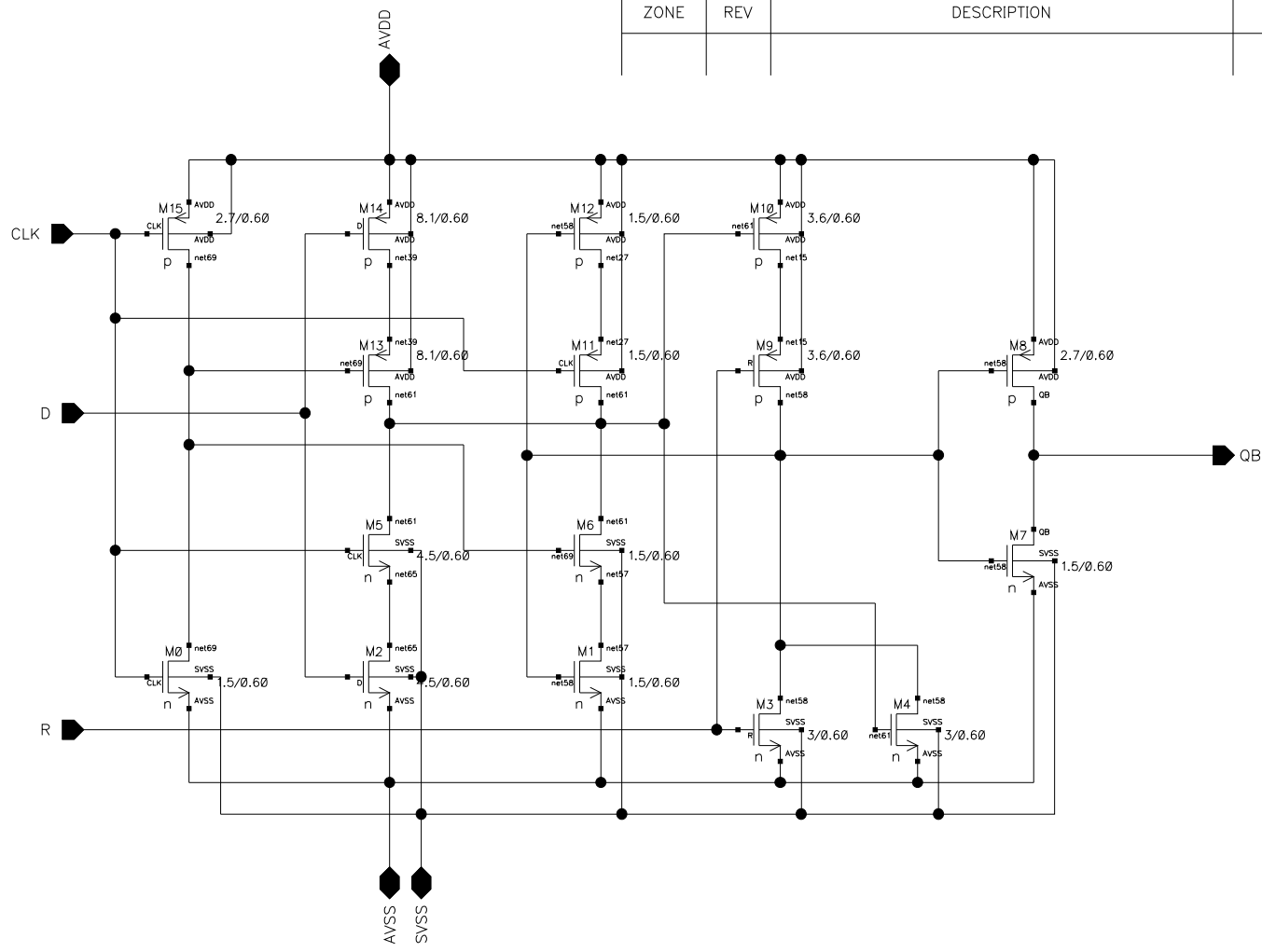
UPDATED	inverter				
Feb 15 18:52:17 2008					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



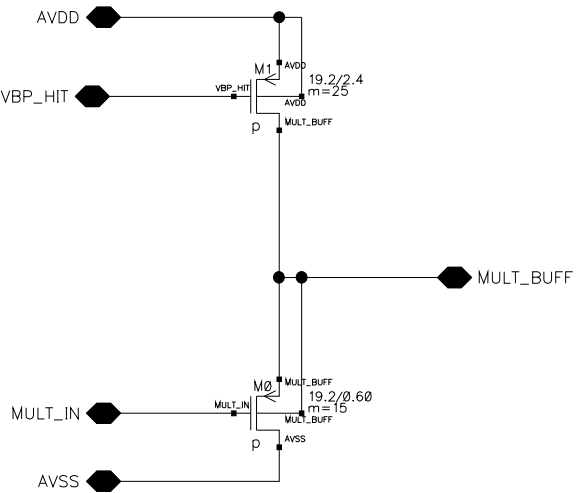
UPDATED					
Jul 9 10:40:23 2007					
DRAWN					
CHECKED					
CHECKED		SIZE	CAGE NO.	DWG NO.	REV
ISSUED		A			
		SCALE		SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



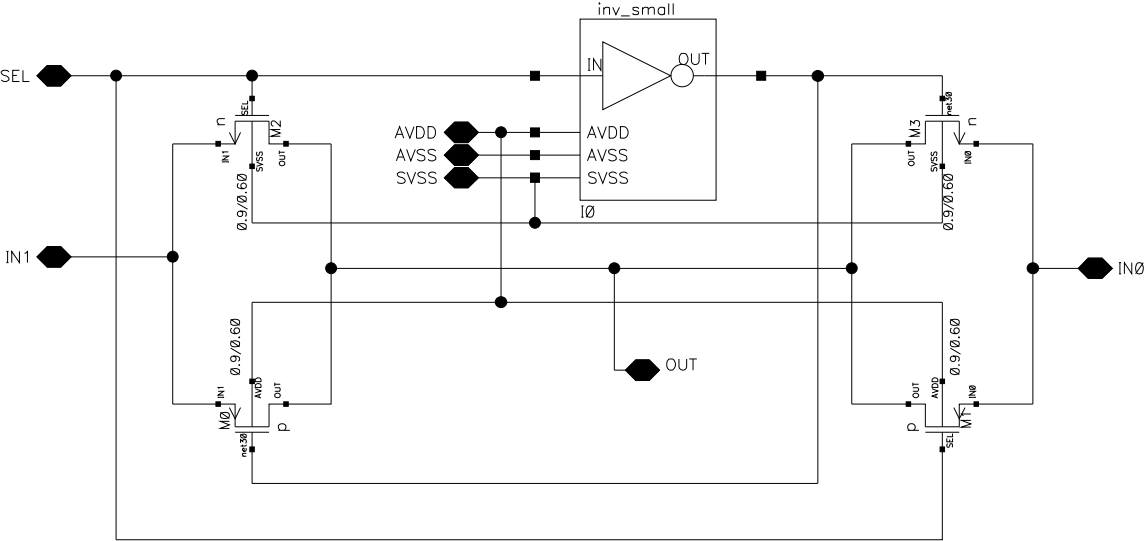
UPDATED		latch				
Jul 9 10:44:29 2007						
DRAWN						
CHECKED						
CHECKED		SIZE	CAGE NO.	DWG NO.		REV
		A				
ISSUED		SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	MULT_BUF				
Sep 12 17:19:01 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



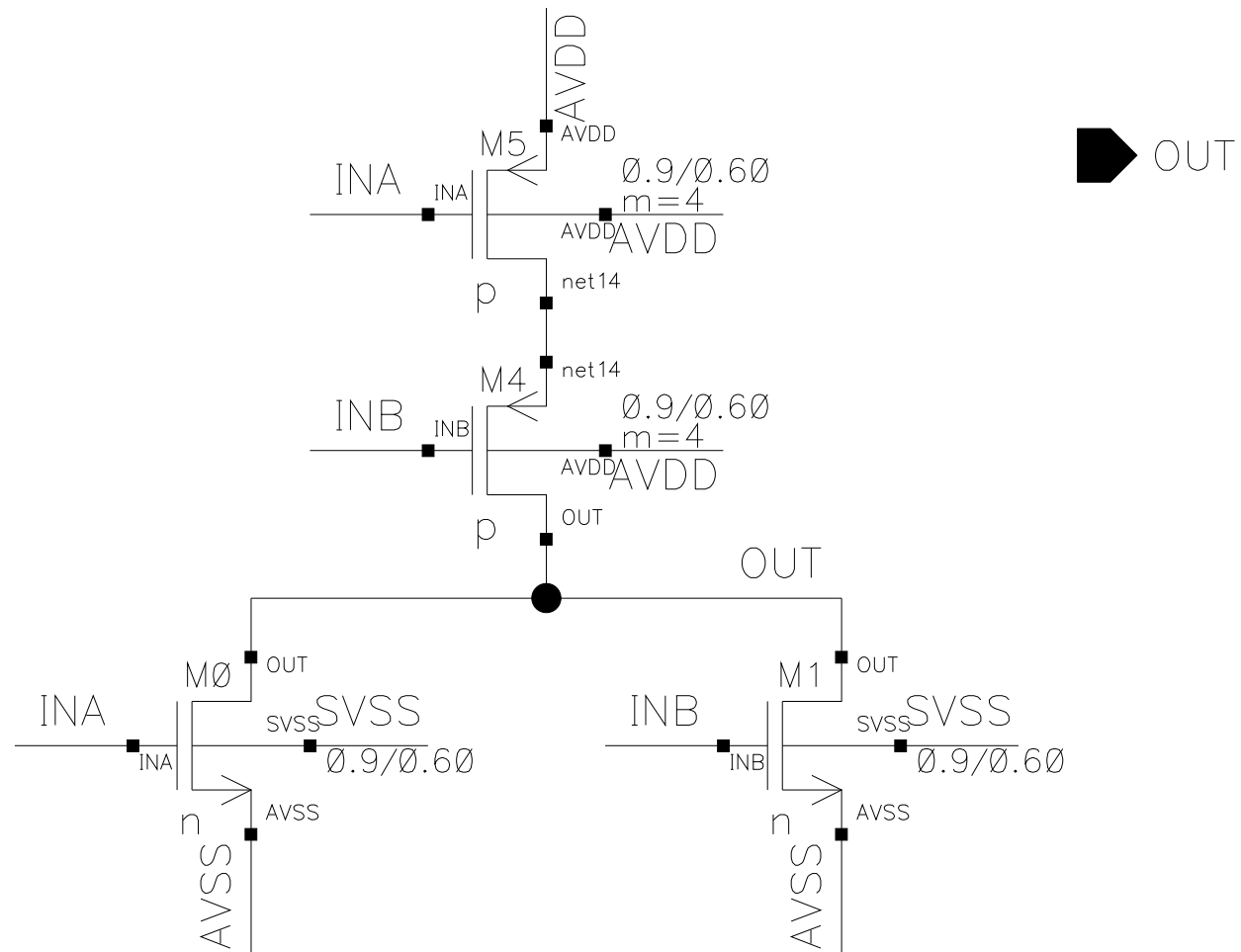
UPDATED	mux_min				
Jun 5 11:38:02 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

AVDD

AVSS

SVSS

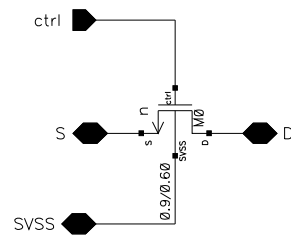
INA
INB





CAGE NO.	DWG NO.	SH 1	REV A
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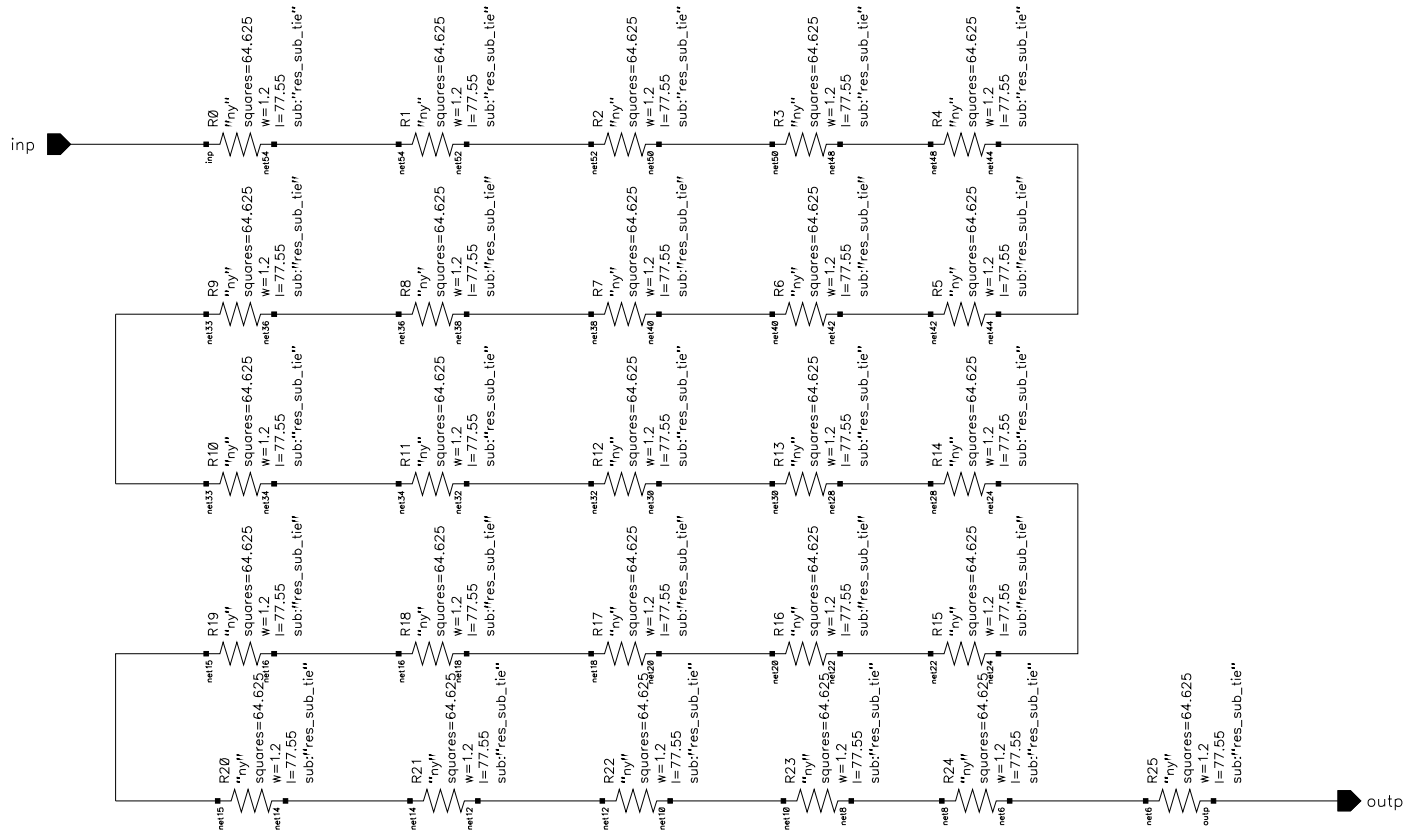
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	SIUE IC Design Lab n-FET Switch			
Apr 1 21:23:24 2007				
DRAWN				
CHECKED	SIZE A CAGE NO. DWG NO. REV A			
CHECKED				
ISSUED				
SCALE	SHEET 1 OF 1			

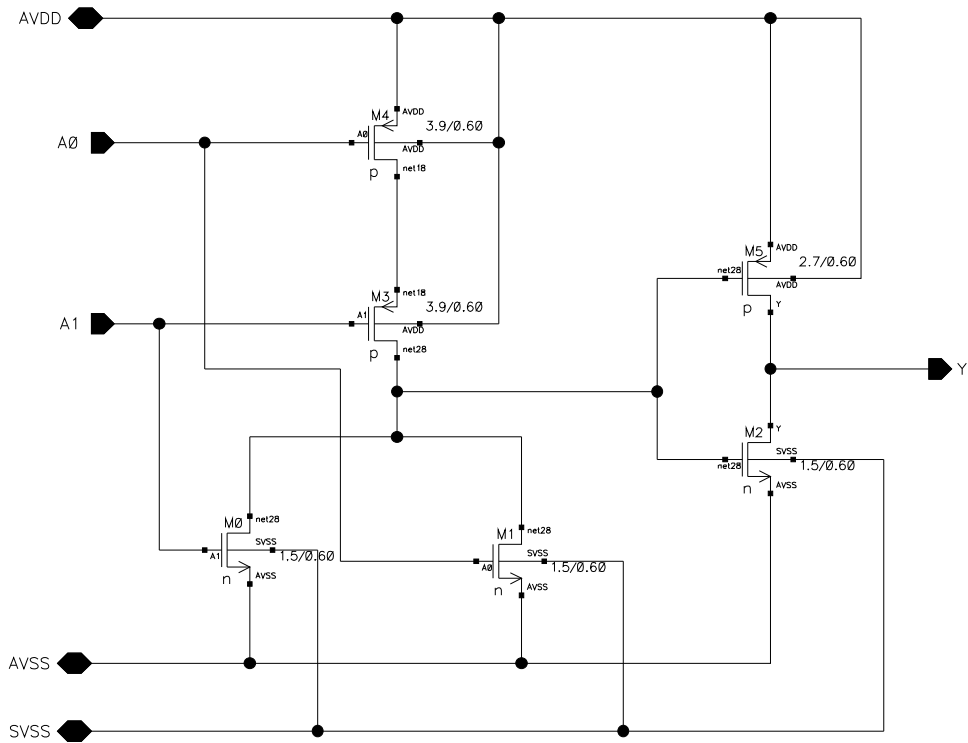


REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

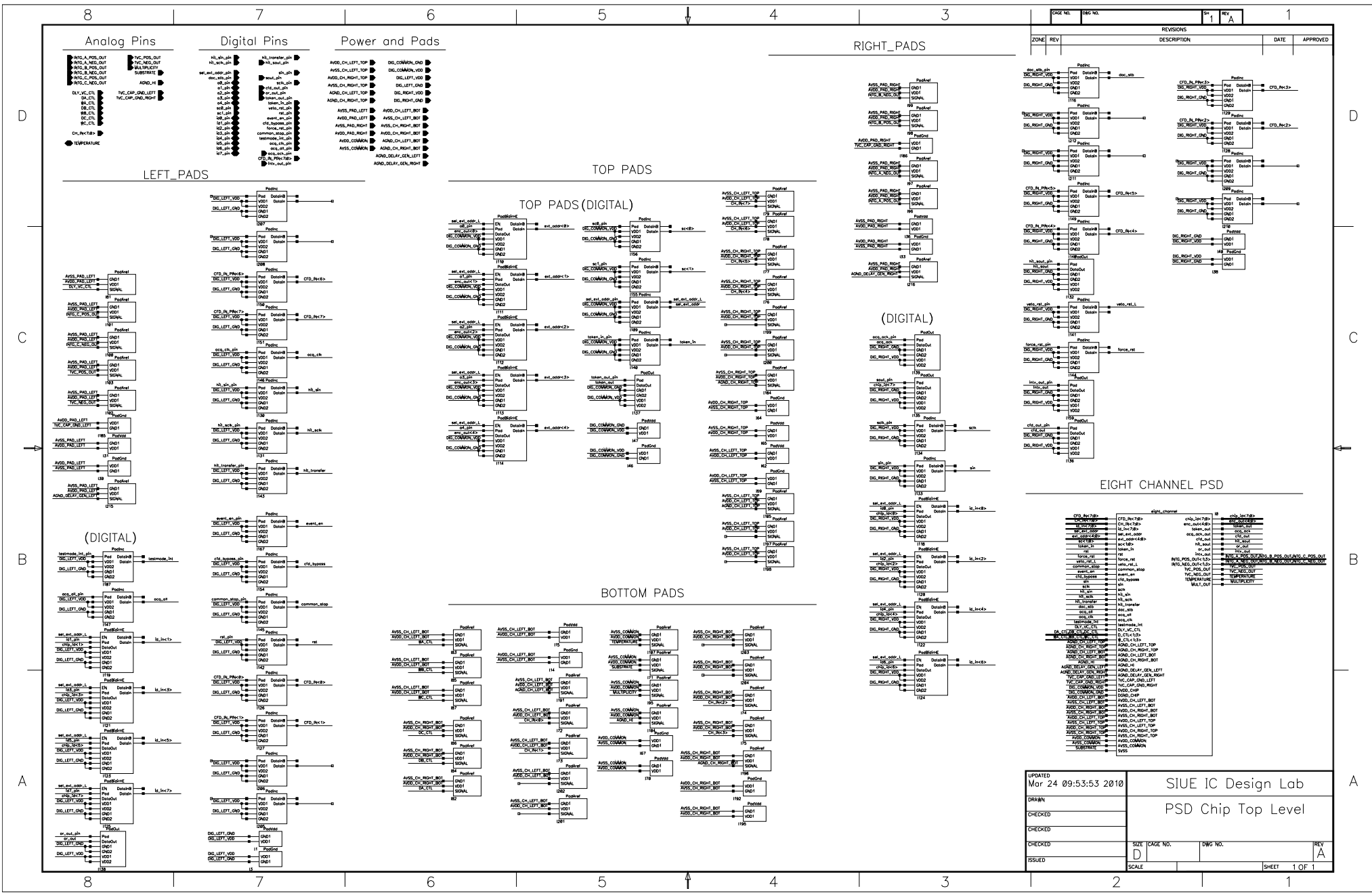


UPDATED	ny_res85k			
Sep 6 14:10:53 2002				
DRAWN				
CHECKED				
CHECKED	SIZE	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	

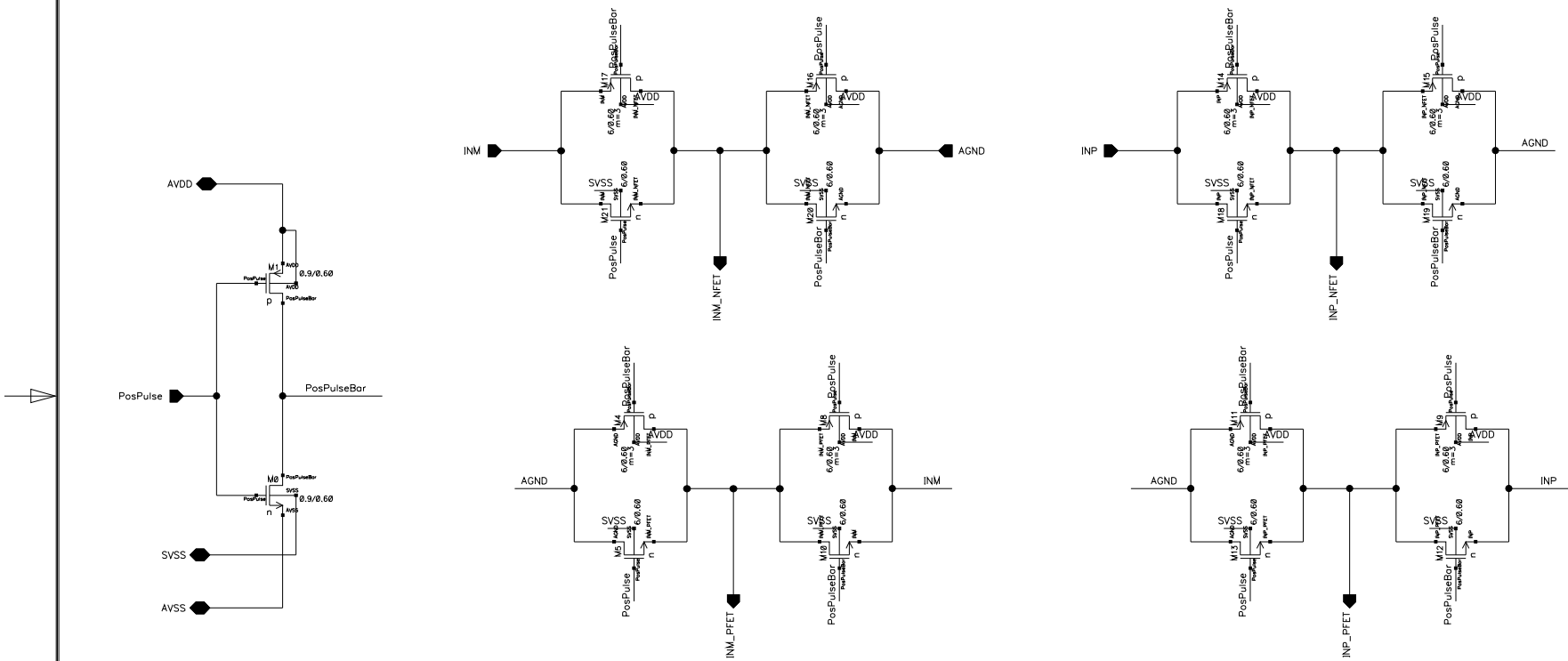


UPDATED	or				
Jul 6 11:07:39 2007					
DRAWN					
CHECKED	SIZE CAGE NO. DWG NO. REV				
CHECKED					
ISSUED					
SCALE		SHEET 1 OF 1			

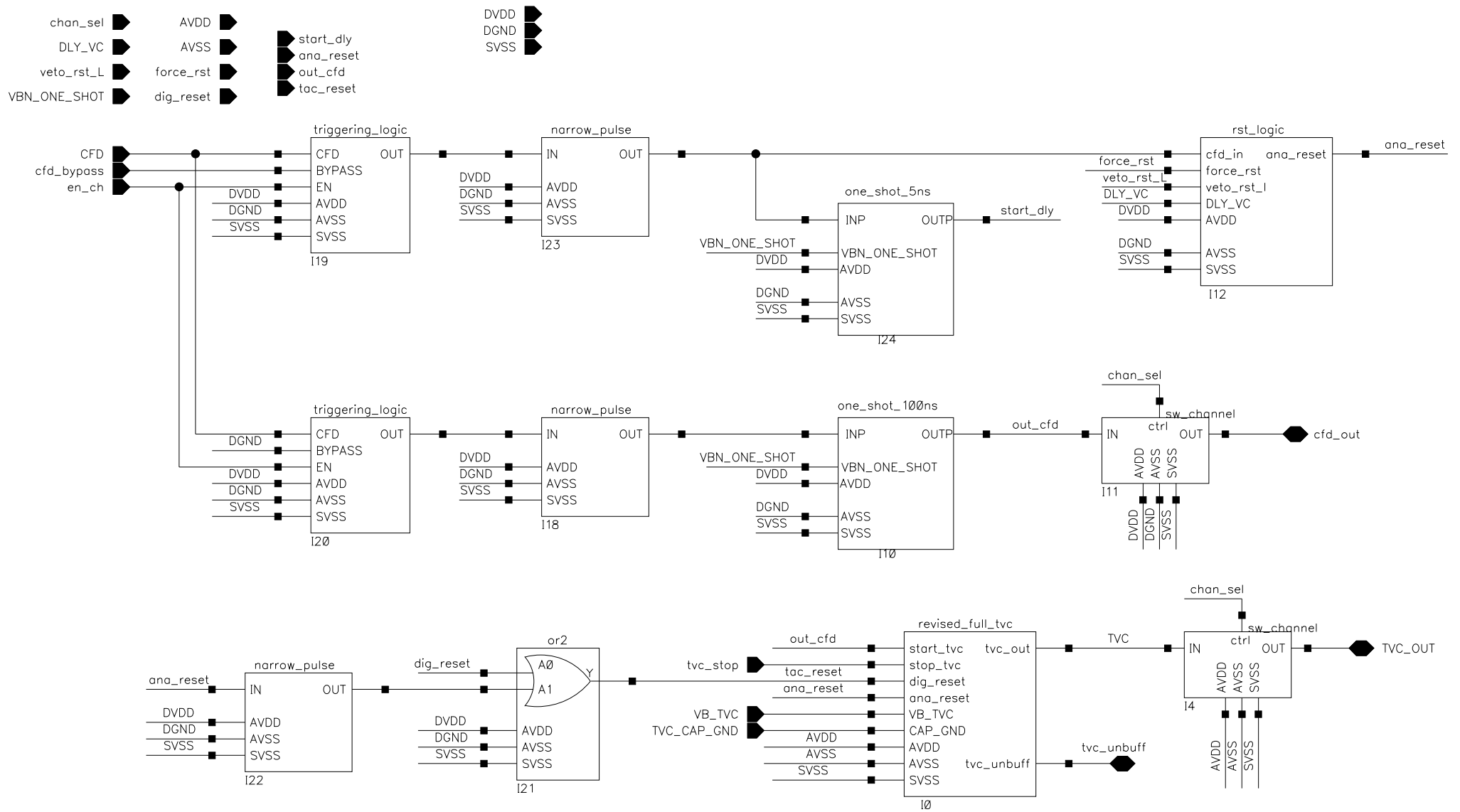


CAGE NO.	DWG NO.	SH 1	REV
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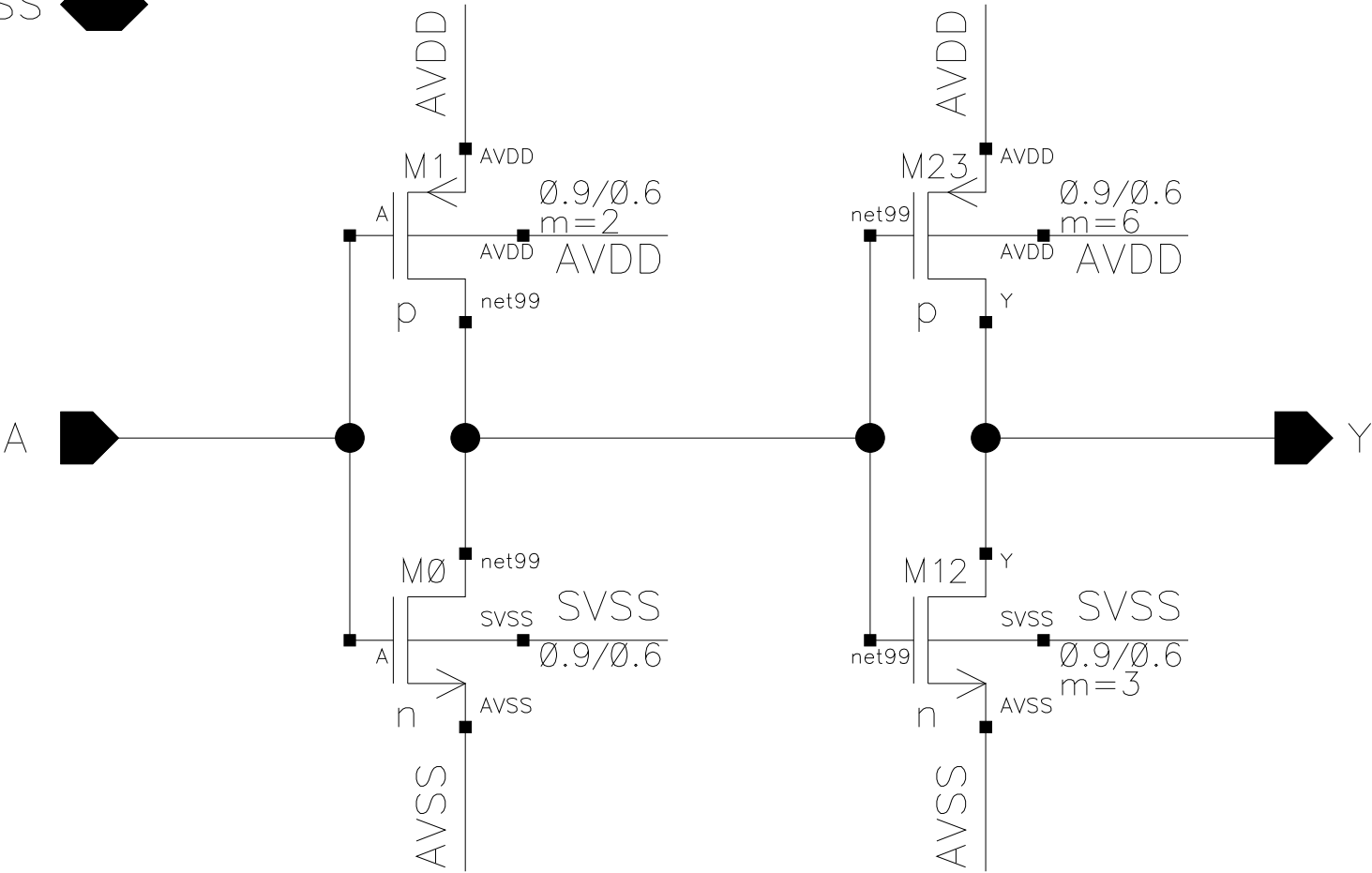
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



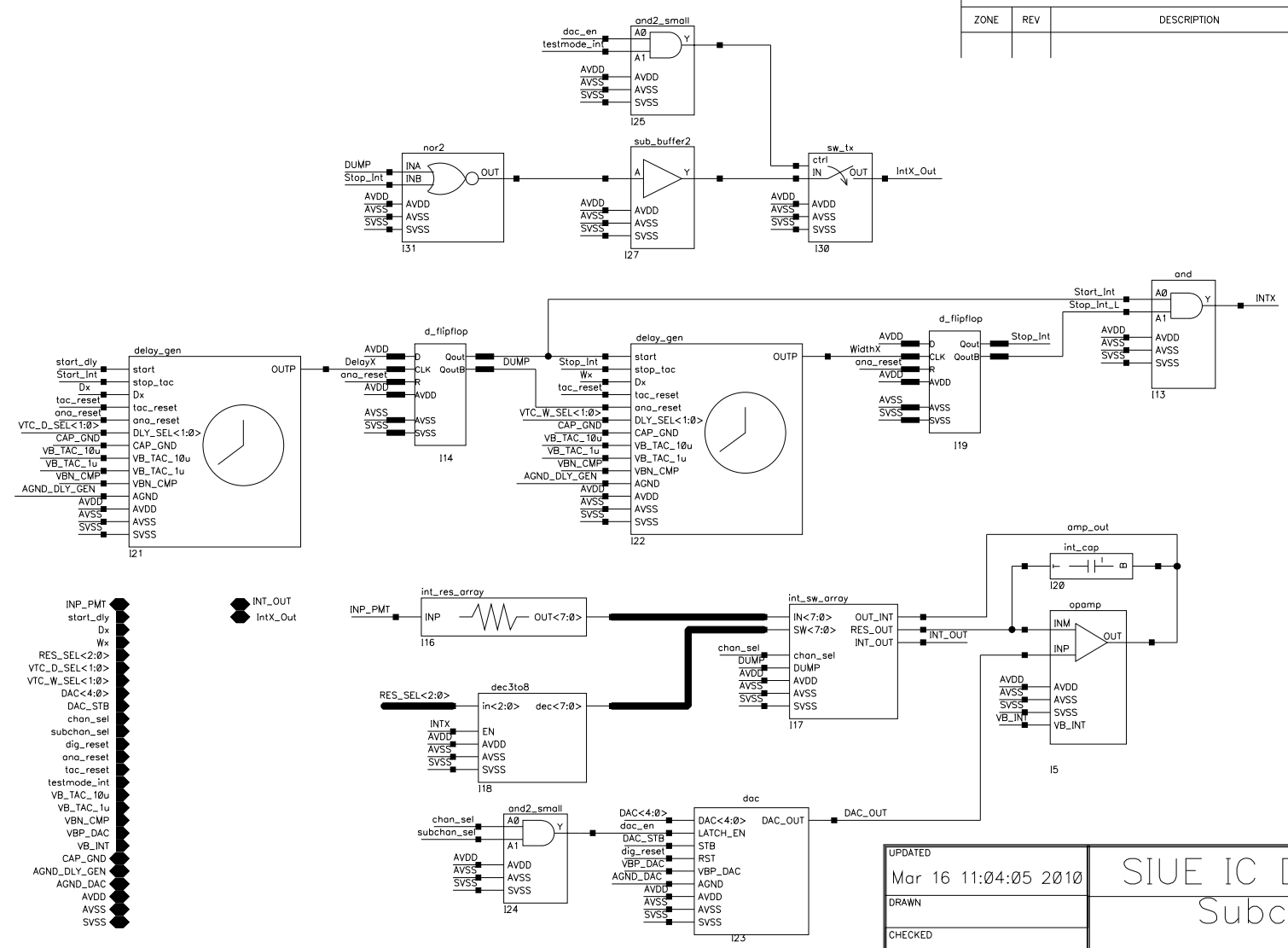
UPDATED Aug 7 16:55:04 2007				
DRAWN				
CHECKED				
CHECKED	SIZE B	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		



AVDD
AVSS
SVSS



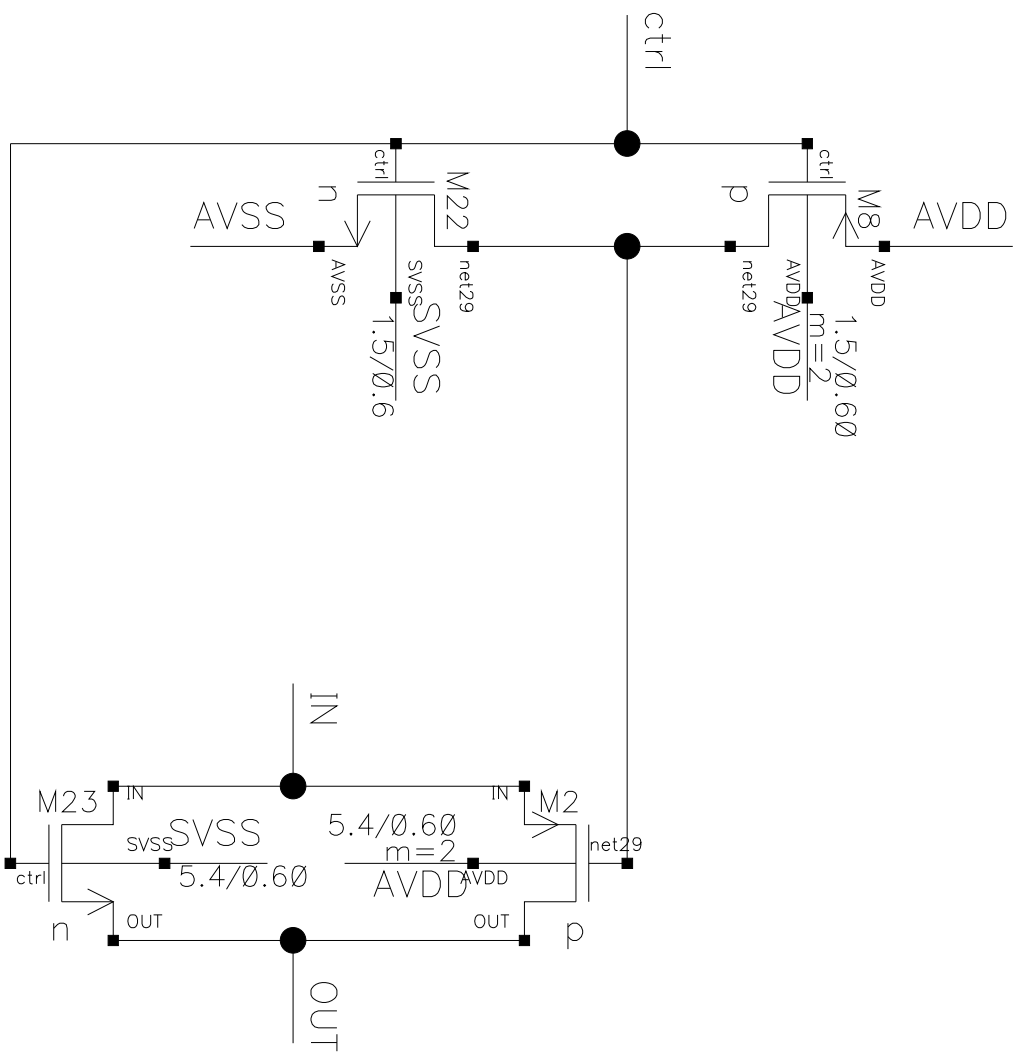
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



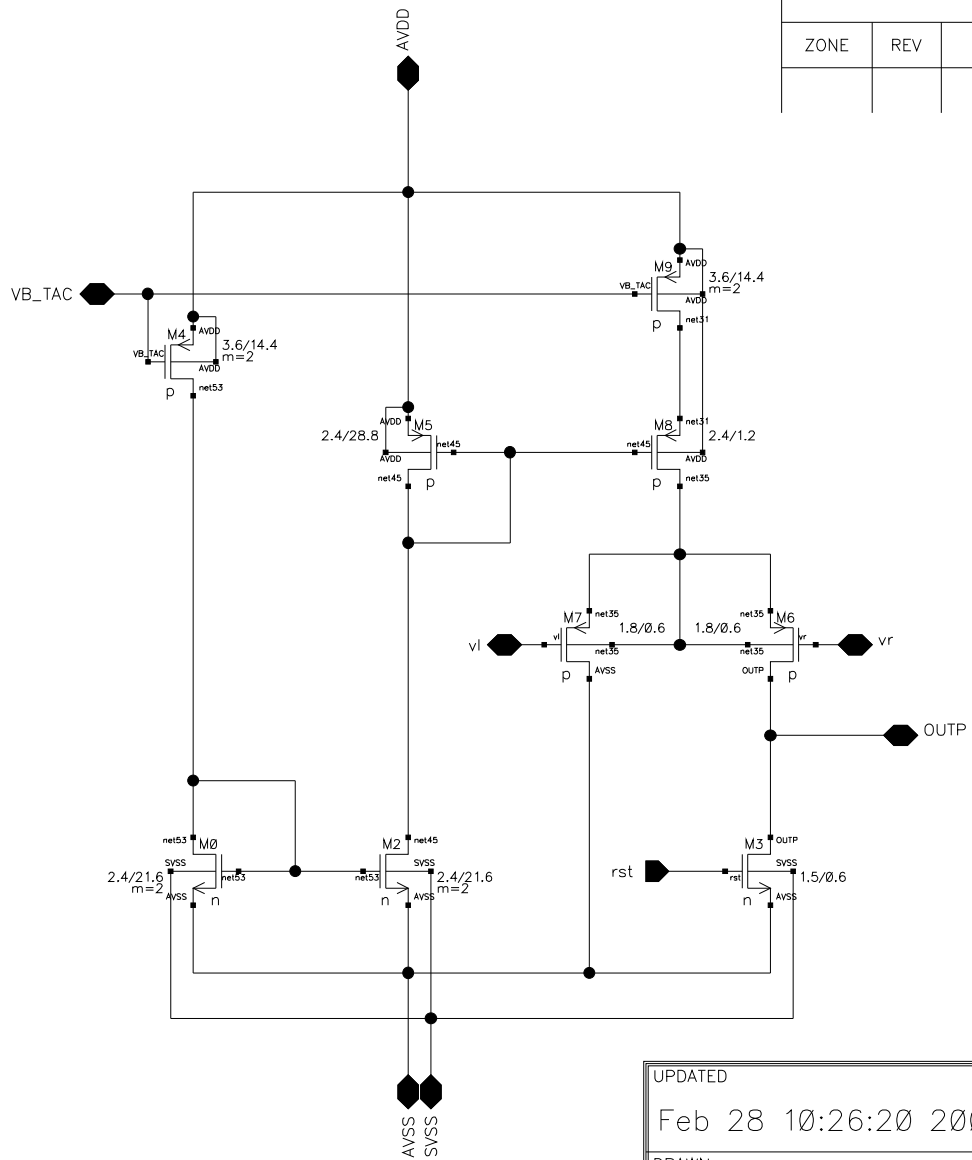
UPDATED Mar 16 11:04:05 2010		SIUE IC Design Lab Subchannel		
DRAWN				
CHECKED				
CHECKED		SIZE B	CAGE NO.	DWG NO.
ISSUED		SCALE	SHEET 1 OF 1	

IN
ctrl
AVDD
AVSS
SVSS

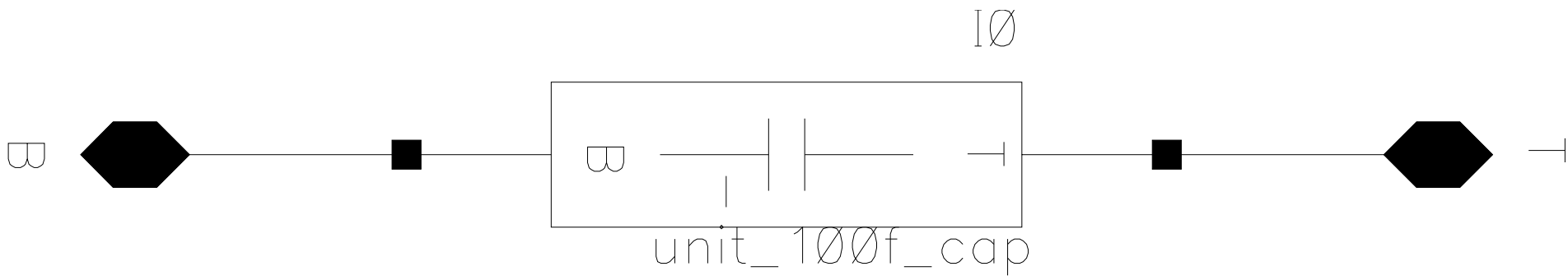
OUT

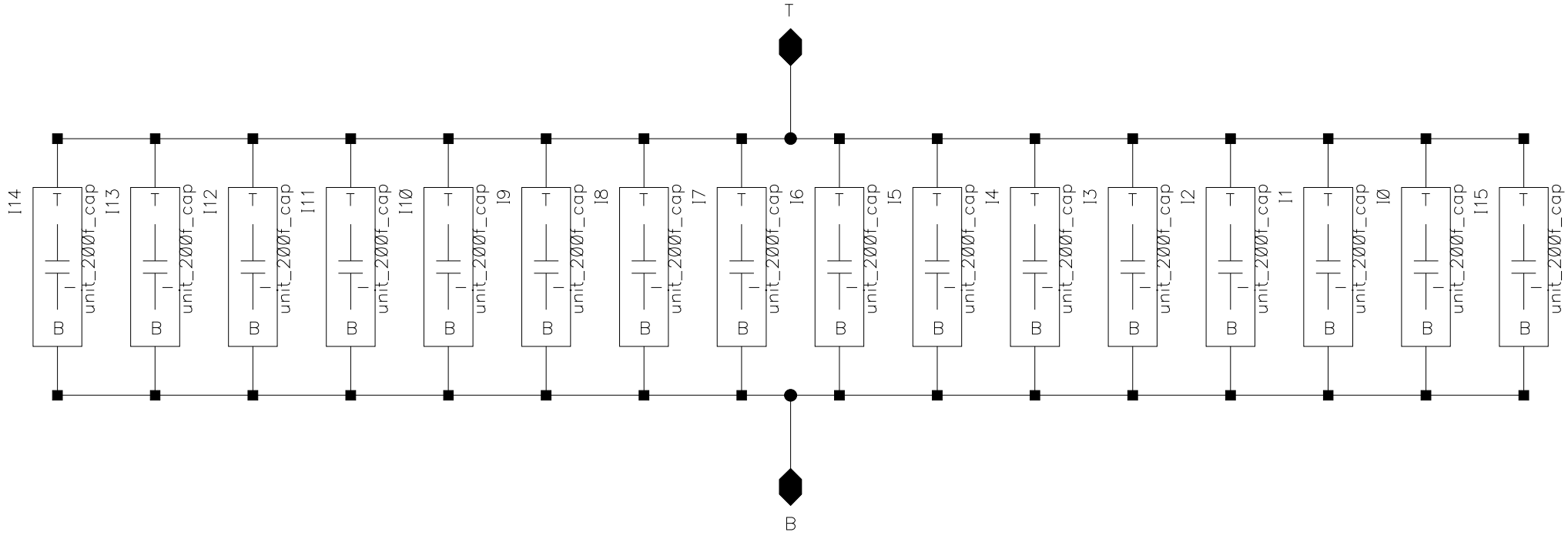


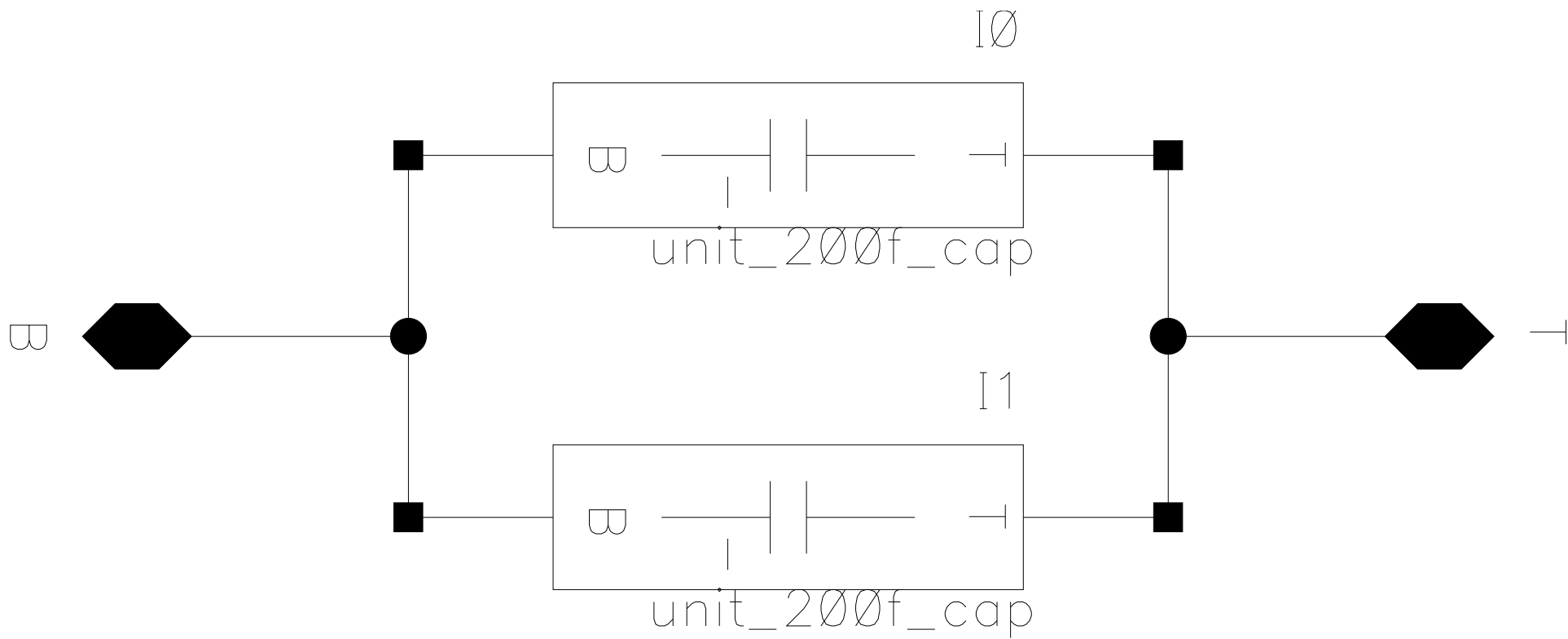
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

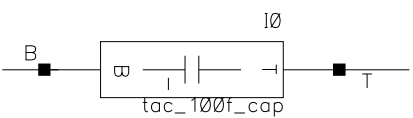
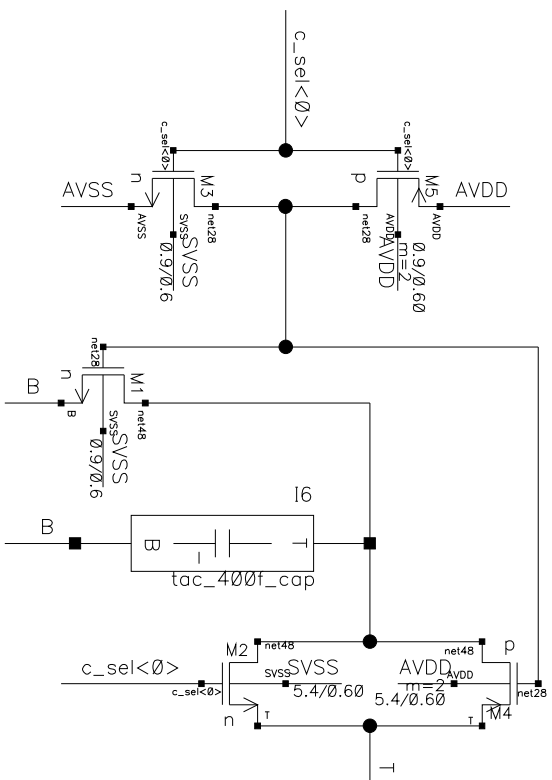
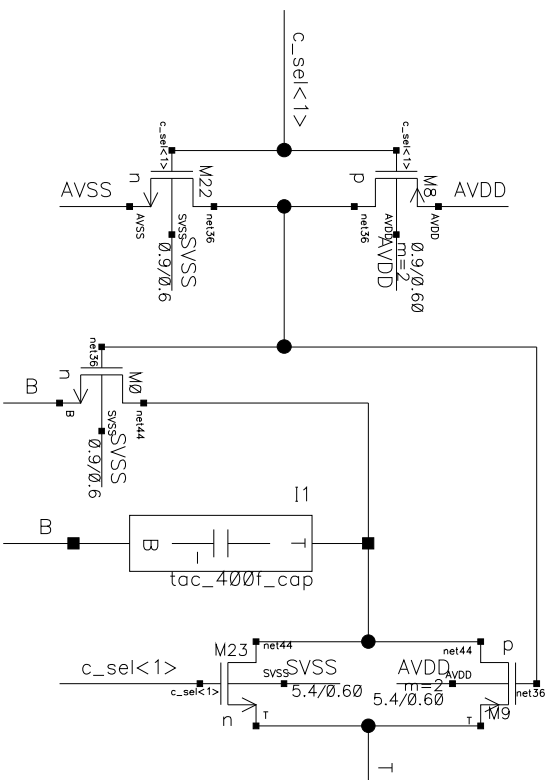
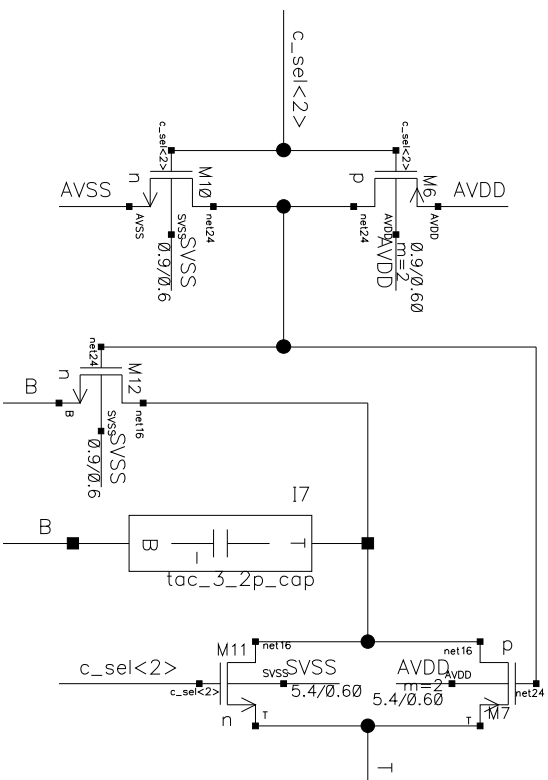
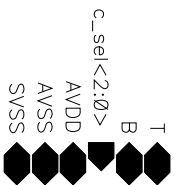


UPDATED Feb 28 10:26:20 2007		tac			
DRAWN					
CHECKED					
CHECKED		SIZE A	CAGE NO.	DWG NO.	REV
ISSUED		SCALE		SHEET 1 OF 1	







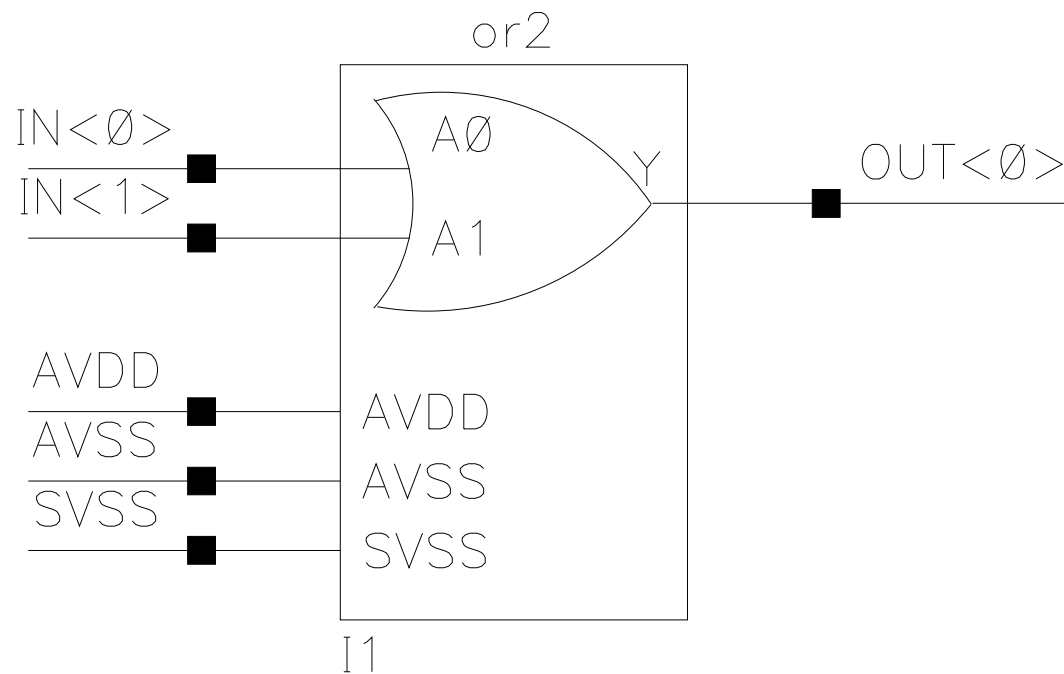
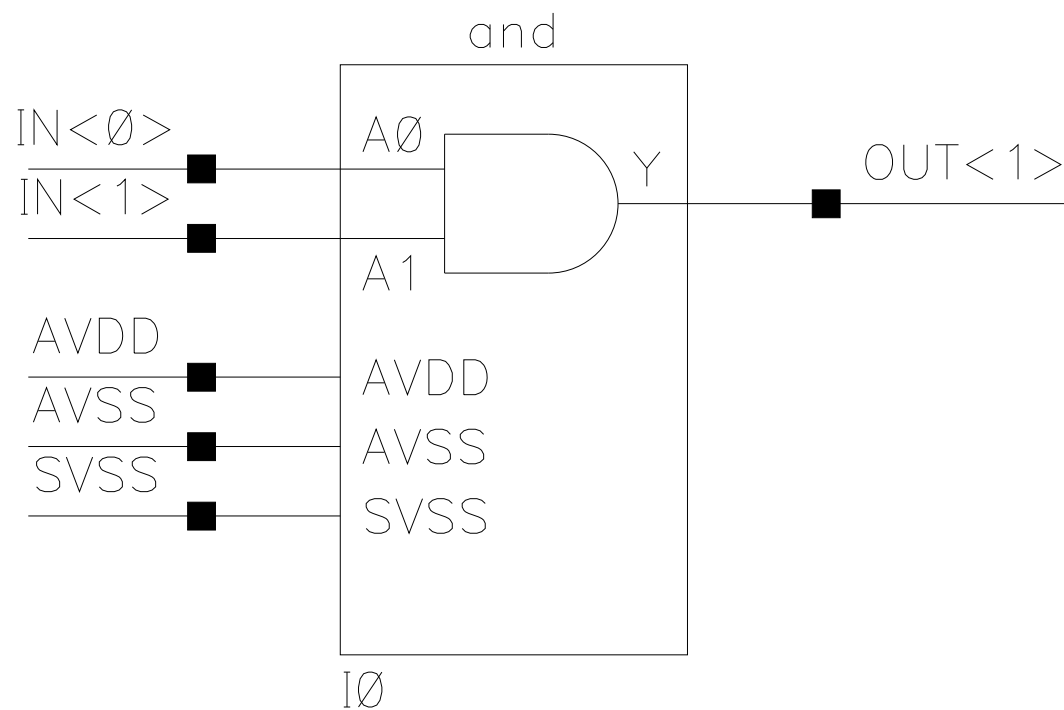
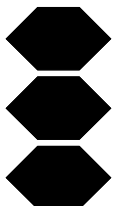


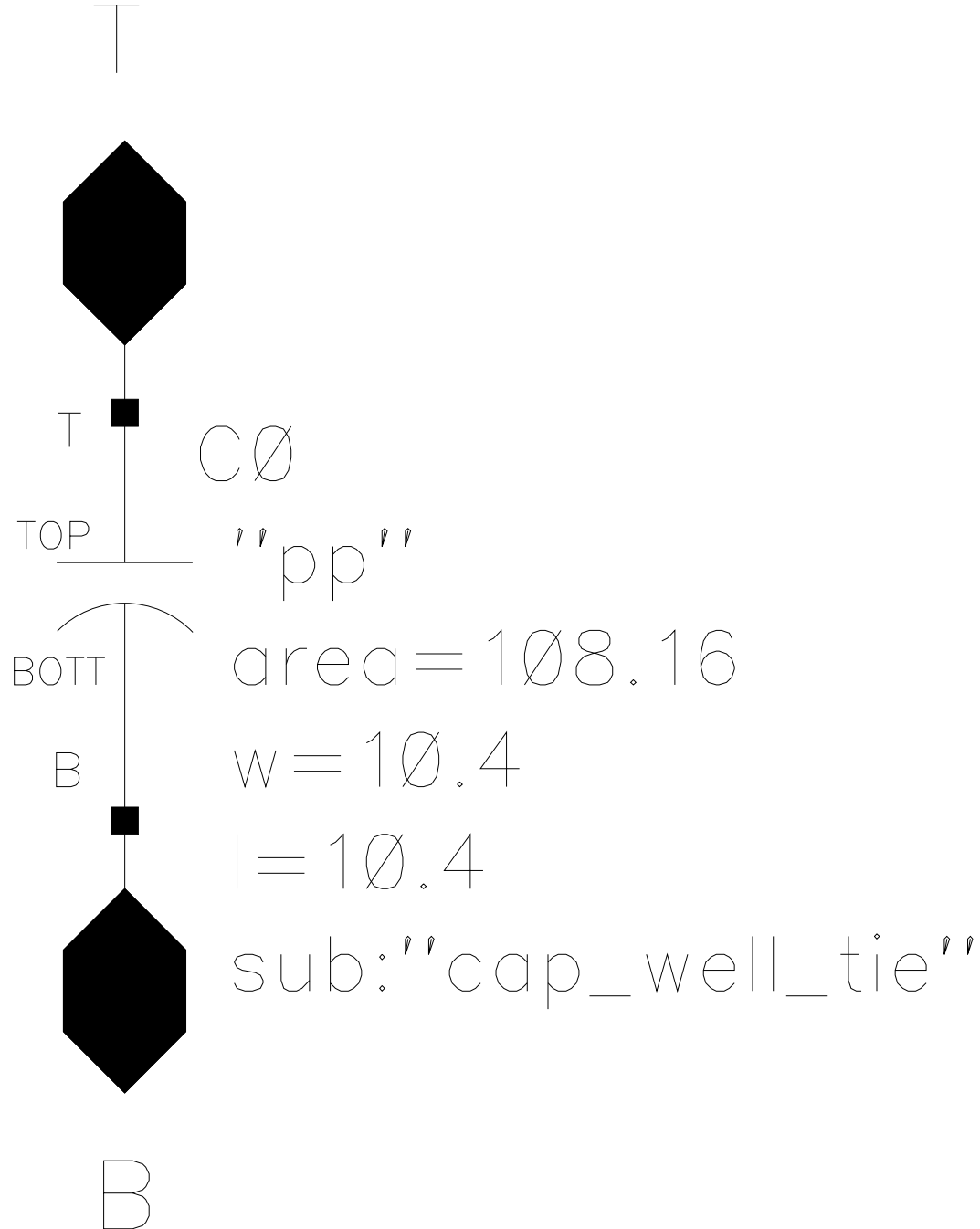
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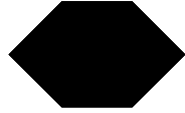
OUT<1:0>

AVDD
AVSS
SVSS





INP



INP

R_0

"hy"

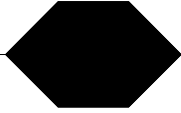
squares=1.28333

w=6

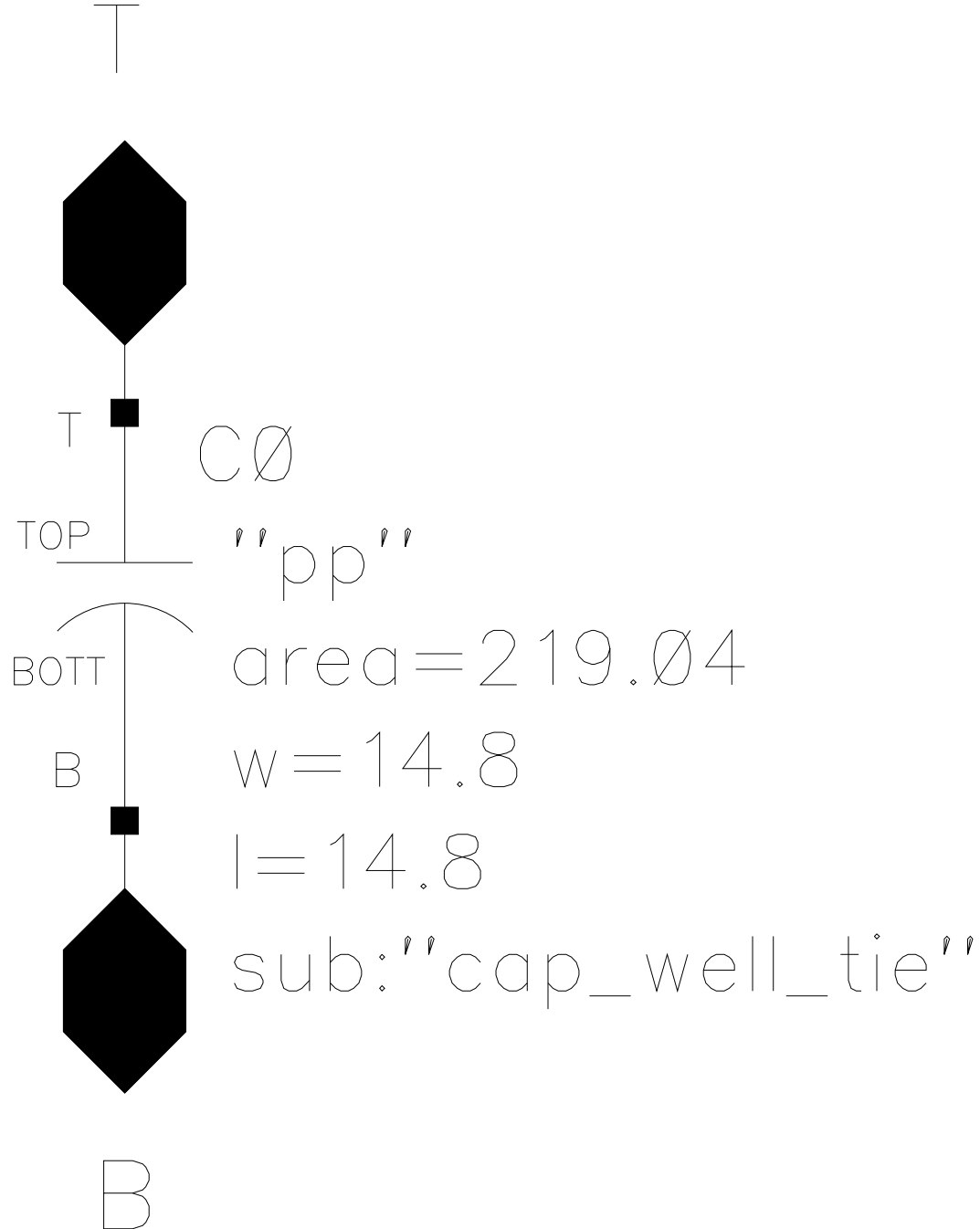
l=7.7

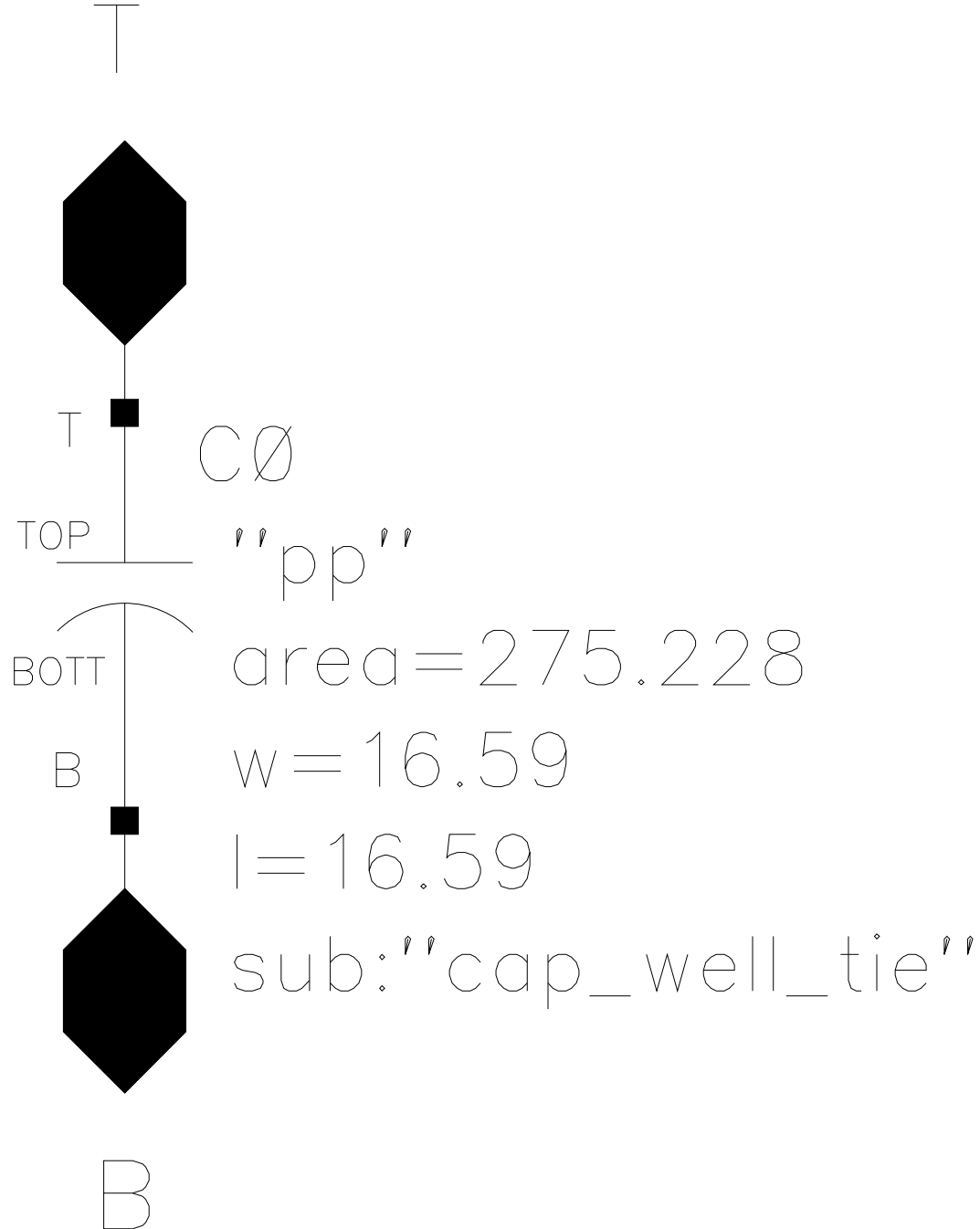
sub:"res_sub_tie"

OUTP



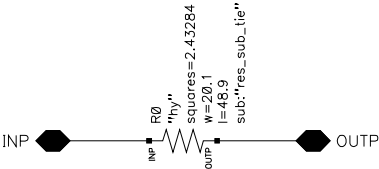
OUTP





		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

Resistor has l=48.9u and w=20.1u



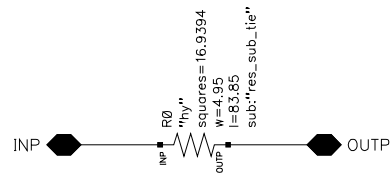
UPDATED	unit_bias_res				
Jun 20 16:17:28 2005					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET 1	OF 1



CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

Resistor has l=83.85u and w=4.95u

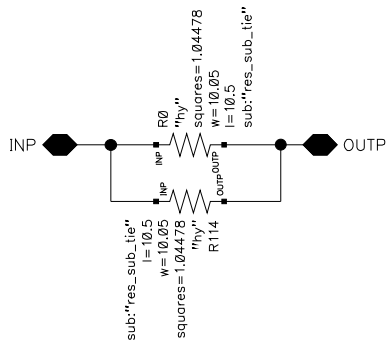


UPDATED	unit_bias_res_2			
Jun 20 16:20:31 2005				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE	SHEET 1 OF 1		



		CAGE NO.	DWG NO.		SH 1	REV
		REVISIONS				
ZONE	REV	DESCRIPTION			DATE	APPROVED

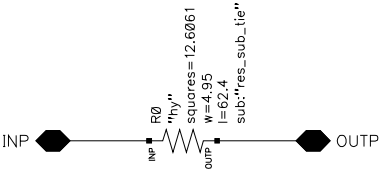
Resistor has l=10.5u and w=10.05u m=2



UPDATED	unit_bias_res_3				
Aug 14 14:19:17 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

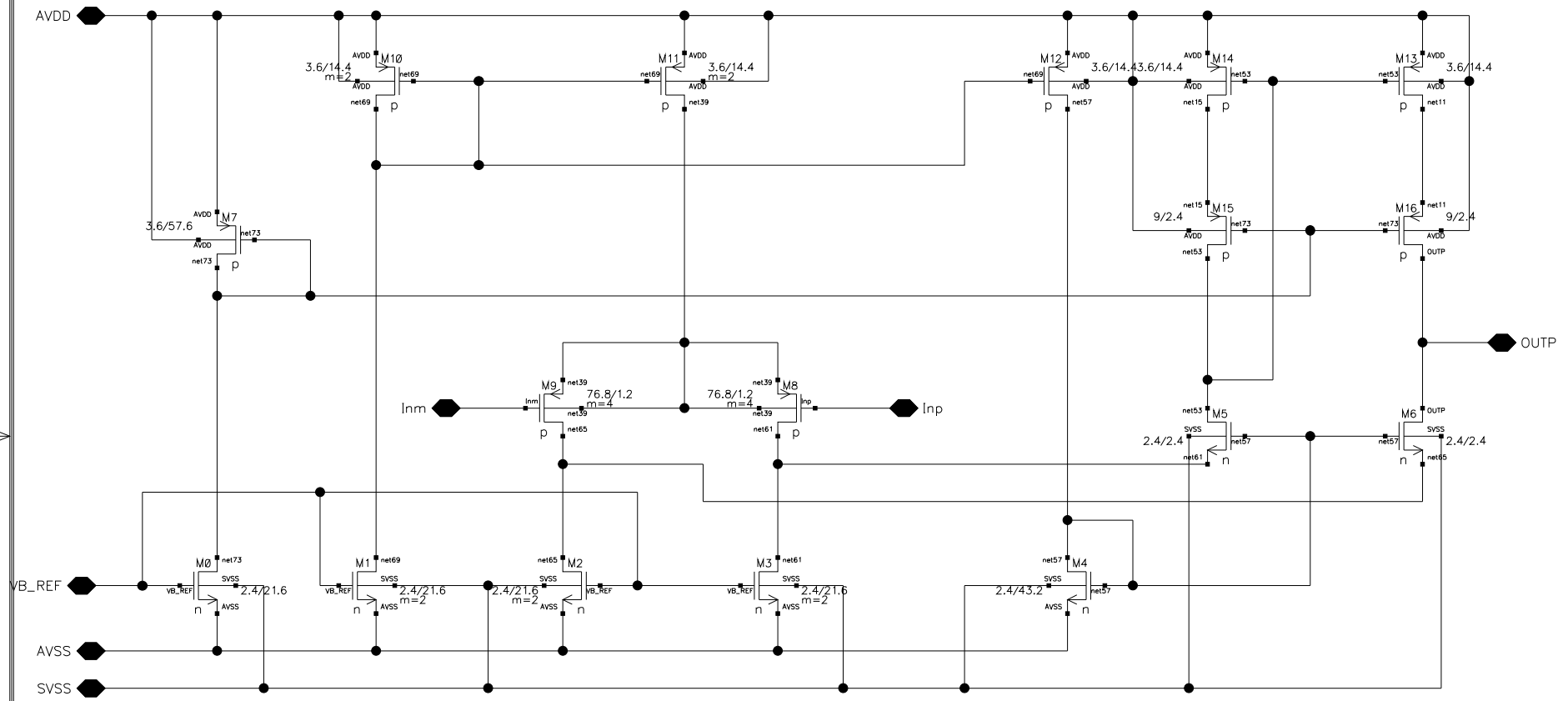
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED

Resistor has l=62.4u and w=4.95u



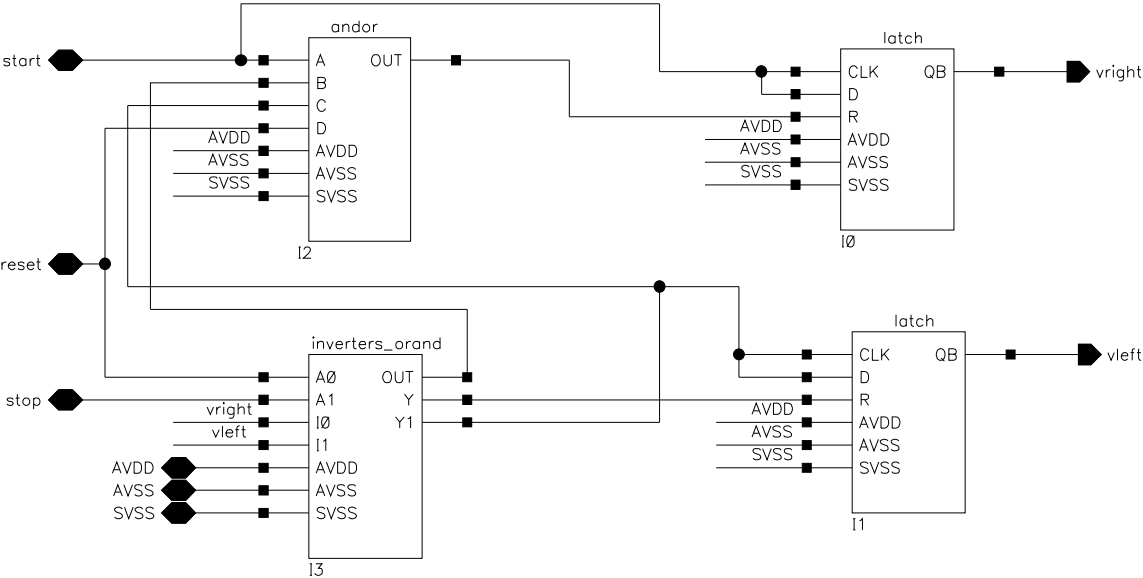
UPDATED	unit_cons_current_res				
Jun 20 16:13:09 2005					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED



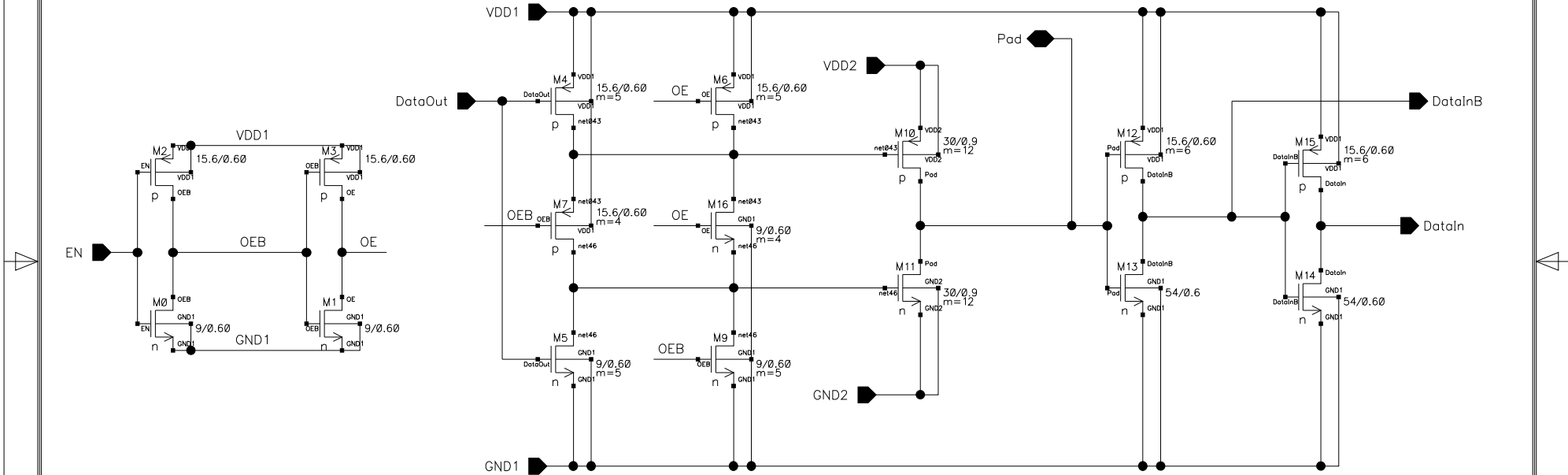
UPDATED Jul 16 13:51:14 2007		vref_buffer			
DRAWN					
CHECKED					
CHECKED		SIZE A	CAGE NO.	DWG NO.	REV
ISSUED		SCALE		SHEET 1 OF 1	

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



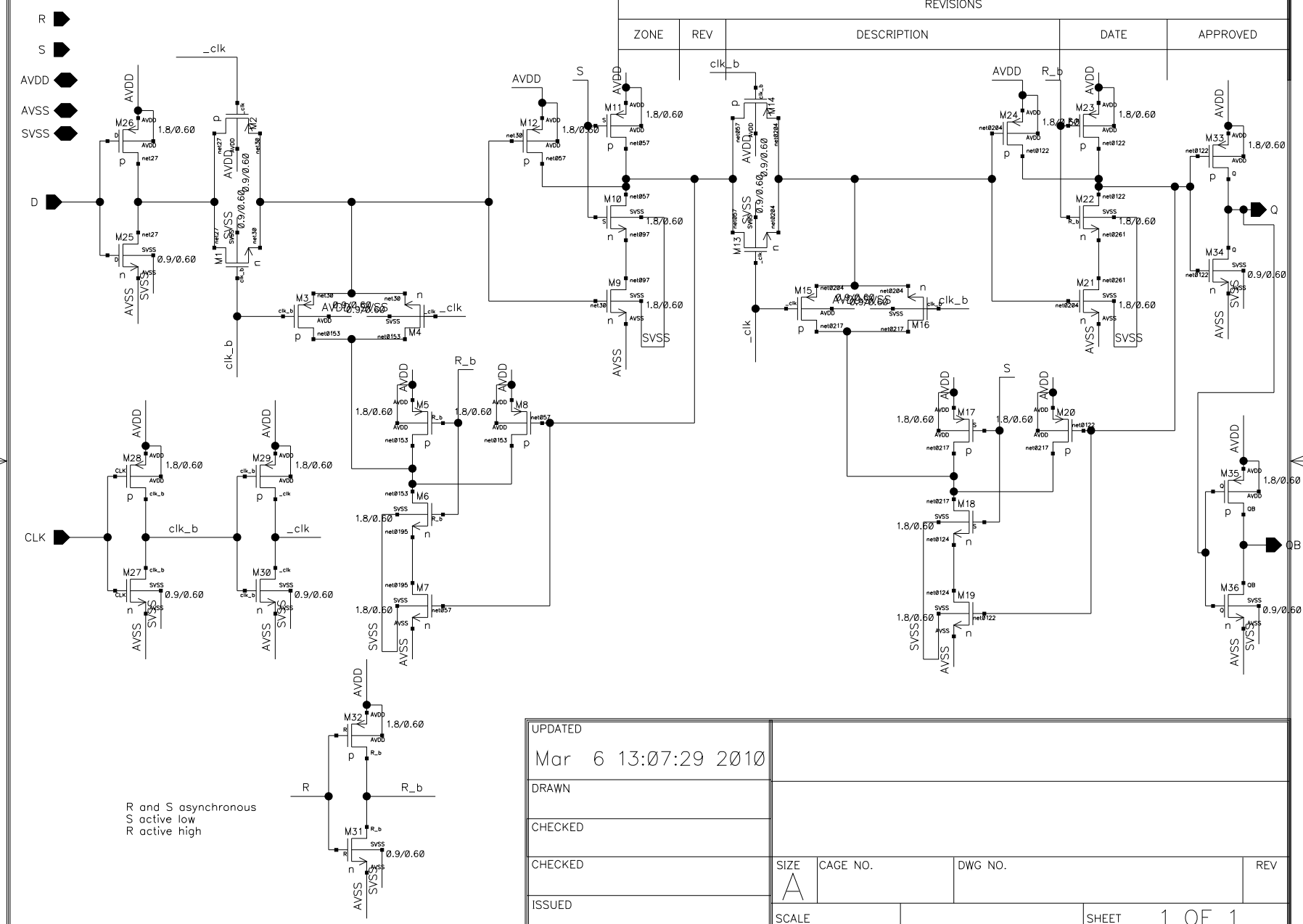
UPDATED	width_gen				
Jul 9 11:21:29 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	A				
	SCALE			SHEET	1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



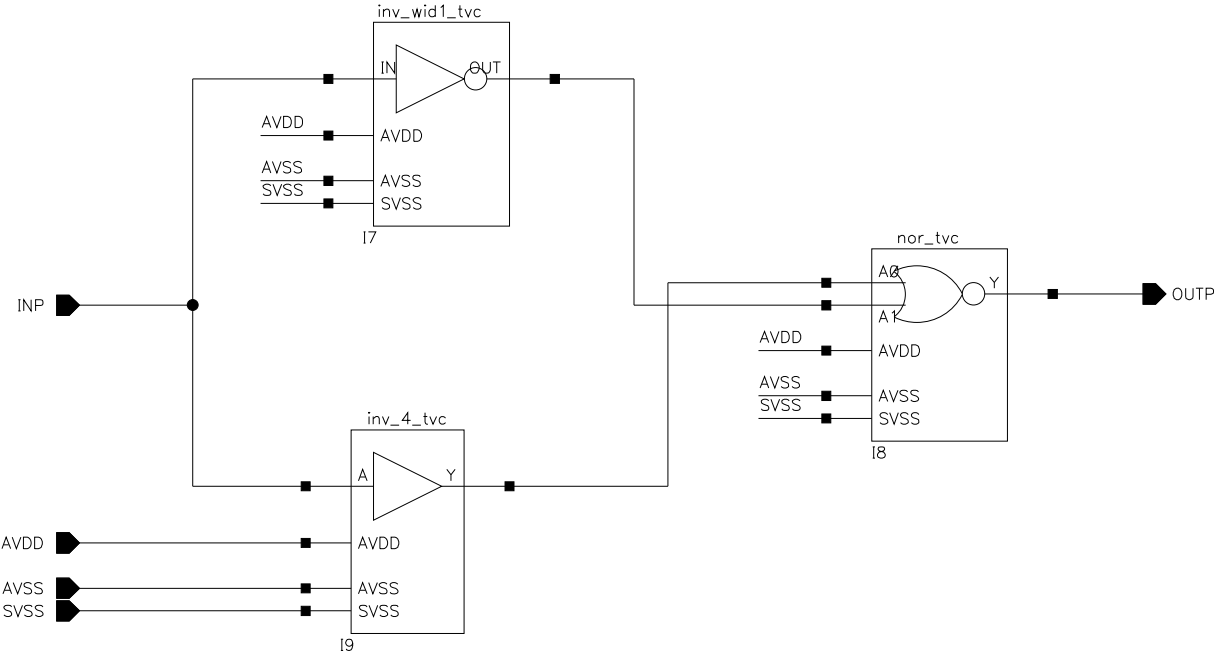
UPDATED	PadBidirHE		
Jul 9 16:28:29 2003			
DRAWN			
CHECKED			
CHECKED	SIZE	CAGE NO.	DWG NO.
ISSUED	A		REV
	SCALE	SHEET 1 OF 1	

REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED



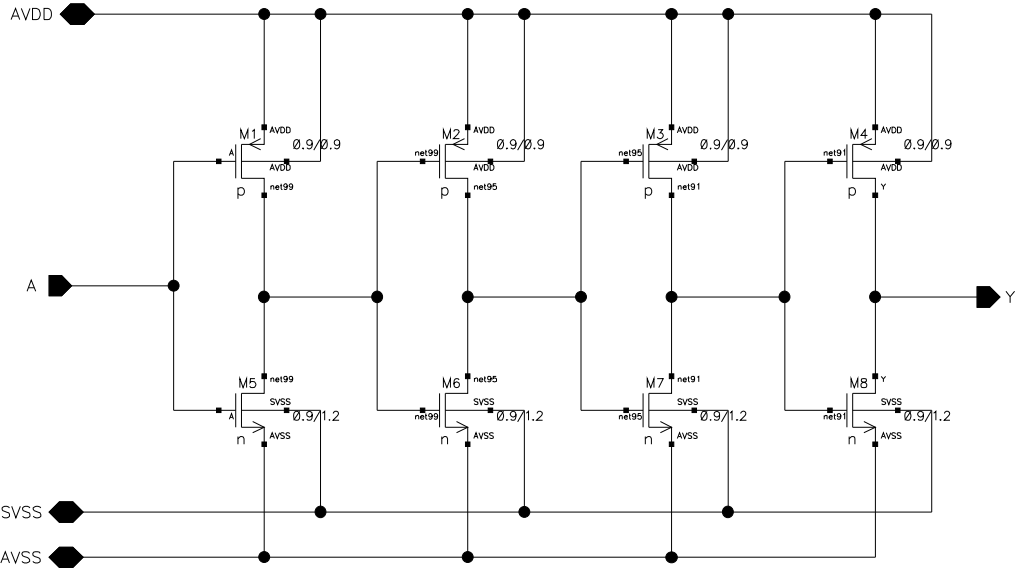
UPDATED Mar 6 13:07:29 2010			
DRAWN			
CHECKED			
CHECKED		SIZE A	CAGE NO.
ISSUED		DWG NO.	REV
SCALE		SHEET 1 OF 1	

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



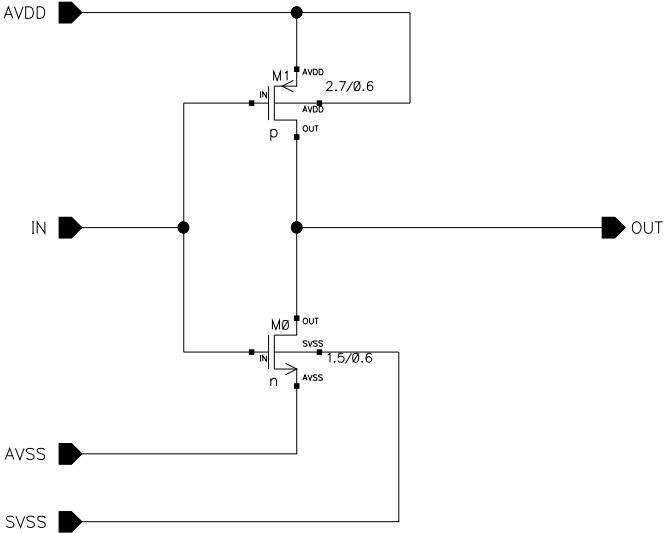
UPDATED	edge_det_pos				
Mar 24 09:53:35 2010					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET 1 OF 1			

	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



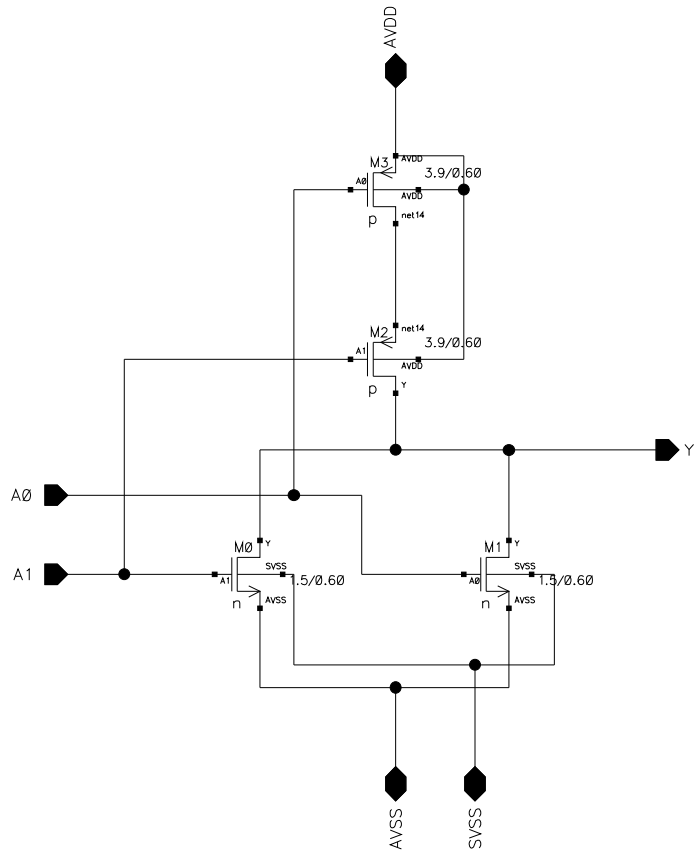
UPDATED	inv_12				
Mar 24 09:53:31 2010					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	inv_wid1				
Oct 4 12:03:01 2007					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET		1 OF 1	

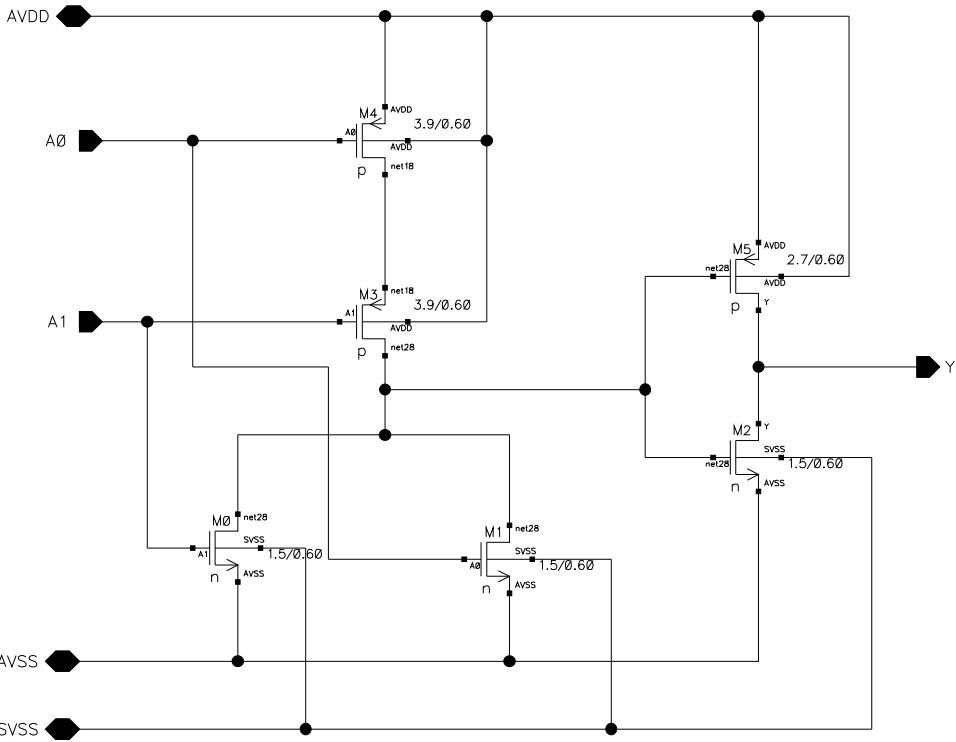
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED
Jun 22 12:47:58 2007
DRAWN
CHECKED
CHECKED
ISSUED

nor			
SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE	SHEET 1 OF 1		

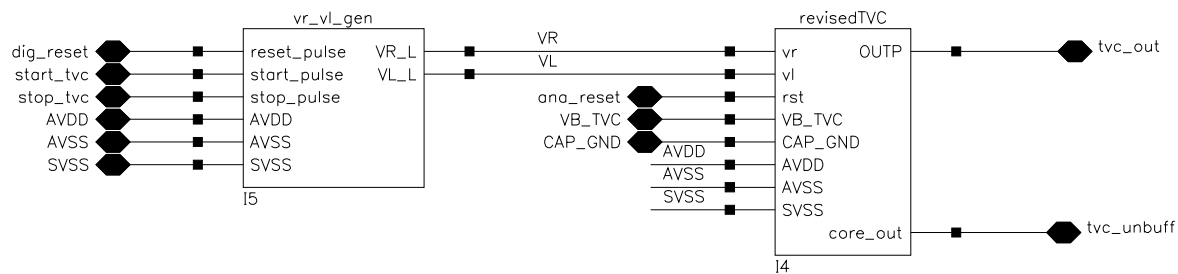
	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	



UPDATED	or				
Jul 6 11:07:39 2007					
DRAWN					
CHECKED	SIZE A				
CHECKED					
ISSUED					
CAGE NO.		DWG NO.		REV	
SCALE		SHEET		1 OF 1	

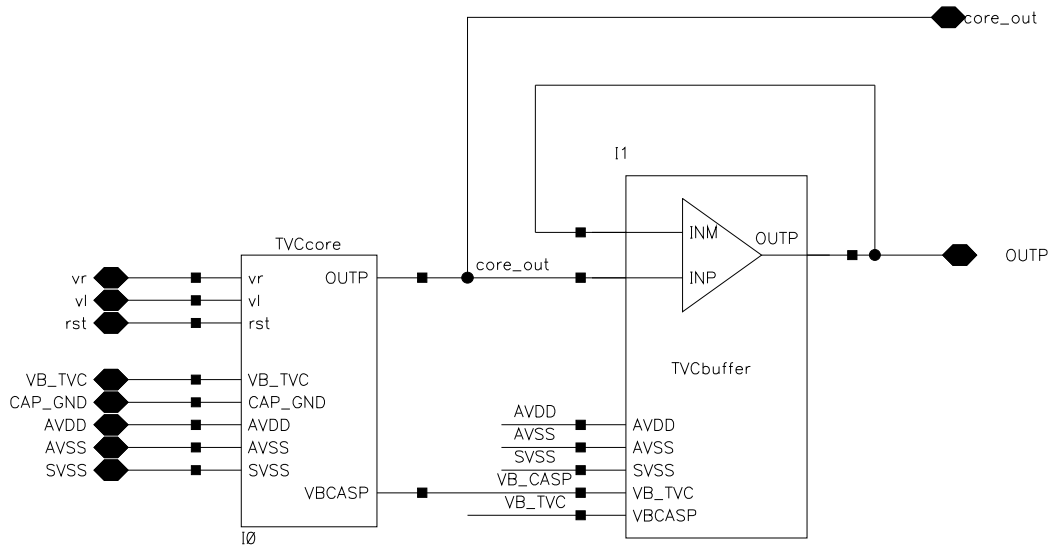
	CAGE NO.		DWG NO.		SH 1	REV
	REVISIONS					
ZONE	REV	DESCRIPTION		DATE	APPROVED	

VR and VL are active low signals.
They drive the gates of PFETs.



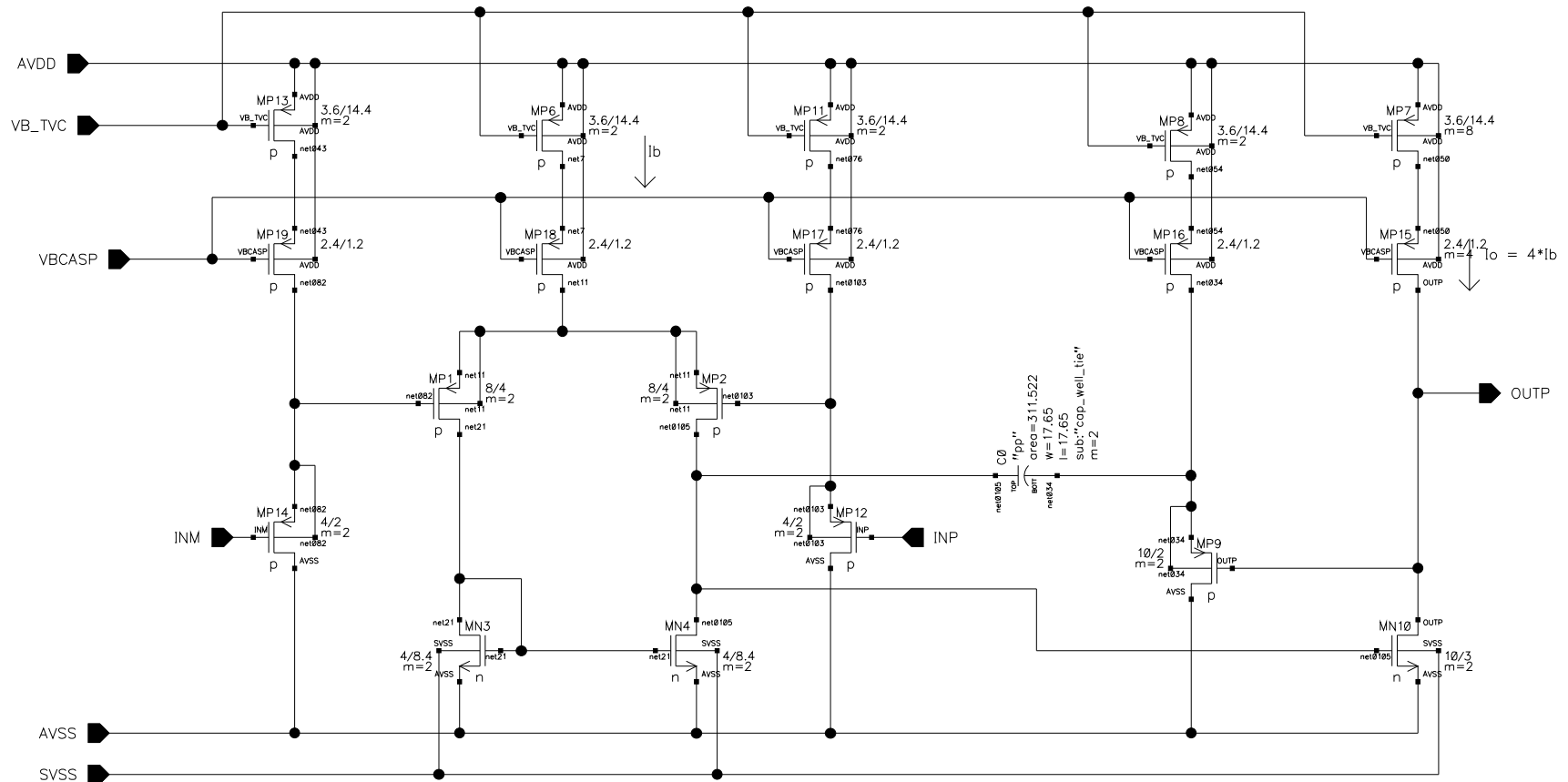
UPDATED	SIUE				
Mar 24 09:53:41 2010	Revised full TVC				
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET	1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	revisedTVC				
Feb 10 10:20:37 2010					
DRAWN					
CHECKED					
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE	SHEET 1 OF 1			

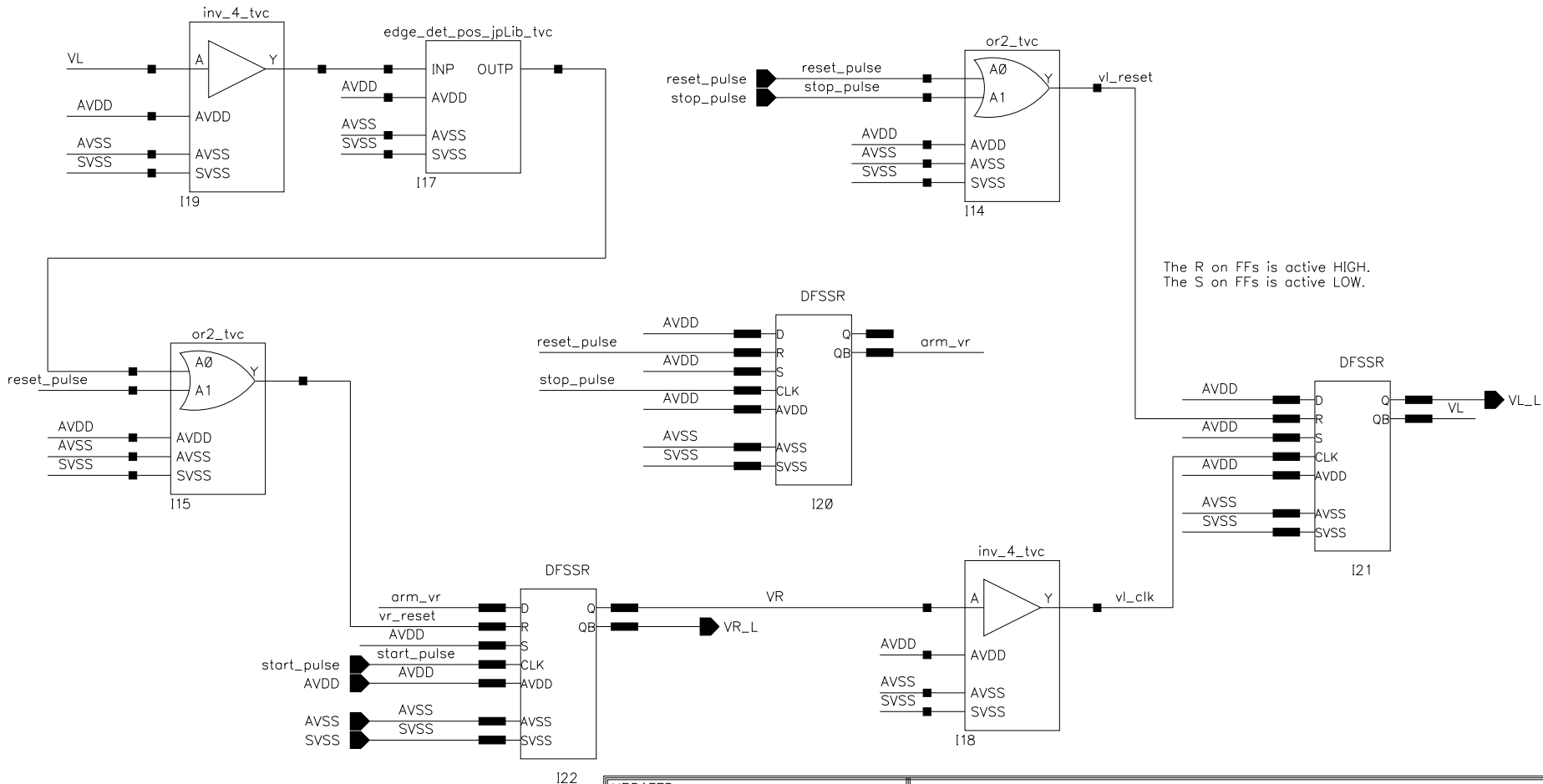
		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION	DATE	APPROVED	



Bias current:
500 ns range: 10 μ A
2 μ s range: 2.5 μ A

UPDATED	SIUE		
Mar 24 13:40:33 2010	TVC local buffer		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO.
ISSUED	SCALE		SHEET 1 OF 1

		CAGE NO.	DWG NO.	SH 1	REV
		REVISIONS			
ZONE	REV	DESCRIPTION	DATE	APPROVED	



UPDATED					
Mar 24 09:53:38 2010					
DRAWN					
CHECKED					
CHECKED	SIZE	CAGE NO.	DWG NO.	REV	
ISSUED	SCALE			SHEET 1 OF 1	