Performance of Revised TVC Circuit

PSD8C Version 2.0

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I) Introduction

This report attempts to document the performance of the revised TVC circuit. The redesign tried to correct several deficiencies identified in the original TVC circuit.

1.) TVC would "re-start" if CFD would fire after common stop signal was issued but before analog reset would come along. The work-around was to hold common stop high until the reset signal is issued. The digital control circuit was incorrectly designed.

2.) The TVC circuit displayed a severe temperature dependence (> 1ns/C). The temperature dependence was identified as being associated with the source follower which was used as a local (channel) buffer.

3.) There was charge sharing issue. This charge sharing problem was a result of the gate-to-drain capacity of the local source follower.

4.) Channels occupying a common quadrant of the IC displayed higher levels of crosstalk between their TVC circuits than displayed between channels which were located in different quadrants of the chip. More specifically, the crosstalk was a result of a transient associated with an intruder channel starting its TVC after the victim channel (which needed to reside in the same quadrant of the IC) had already started its TVC. The error was on the order of a couple nsec.

5.) It appeared that noise from the substrate could be coupling into the integrating amplifiers in each of the sub-channels. While not a significant issue, it was felt that some additional shielding could be helpful.

The following actions were taken:

1. Digital control logic was completely re-designed. The starting and stopping was made edge-sensitive and start signals occurring after a stop signal arrives but before a reset signal is applied are now ignored.

2. The source follower buffer was replaced with an amplifier (OTA) connected in a unity gain configuration. This removes both the temperature dependence and the charge sharing issues which plagued the initial design.

3. In order to slightly increase the available linear range, the capacitor in the TVC circuit was increased in size by about 10% (2.8 pF → 3.1 pF).

4. Each quadrant of the IC has a dedicated AVDD and AVSS pins. The TVC crosstalk issues were traced to the routing of the AVDD power line. In Rev 1.0 of PSD8C, a very wide AVDD line fed the center of the supply rails for the channels common to a quadrant. This shared impedance was the source of the problem. When a second channel in the quadrant

fired, it would alter the charging rate of the first channel because of a small induced change in the gate-source voltage of the FET providing current to the capacitor in the TVC circuit.

5. In order to potentially improve the noise performance of the integrator in each of the chip's 24 sub-channels, a NWELL was placed underneath both the resistors that determine integrator charging rate and under the integrating capacitor itself. This was done to reduce the amount of noise coupling from substrate to the inverting terminal of the op amp.

II) TVC Linearity (500 ns range mode)

We begin by looking at the results obtained for a nominal temperature of 27C and "typical" process parameters. Here are the results of electrical simulations (using the schematics and not the extracted netlists).

We begin by looking at the linearity. The simulation was set up to

1) Apply a "reset"
2.) Issue a "start"
3.) Wait a time D
4.) Issue a "stop"
5.) Go back and do (1) … each time (3) is performed the value of D is increased by 10 ns (if we are in 500 ns range) and increased by 40 ns (if we are in 2000ns range). A single simulation takes about 30 minutes to complete.

Shown on the next page is a plot (Fig. 1) of the raw (before our re-designed channel buffer) output from the TVC along with the output of the re-designed buffer. The difference in time between the "start" and "stop" signals is plotted on the x-axis. The slope is about 3.25mV per ns. The full-scale voltage (about 2V) corresponds to about 600 ns. There is no notable difference between the buffered and un-buffered outputs.

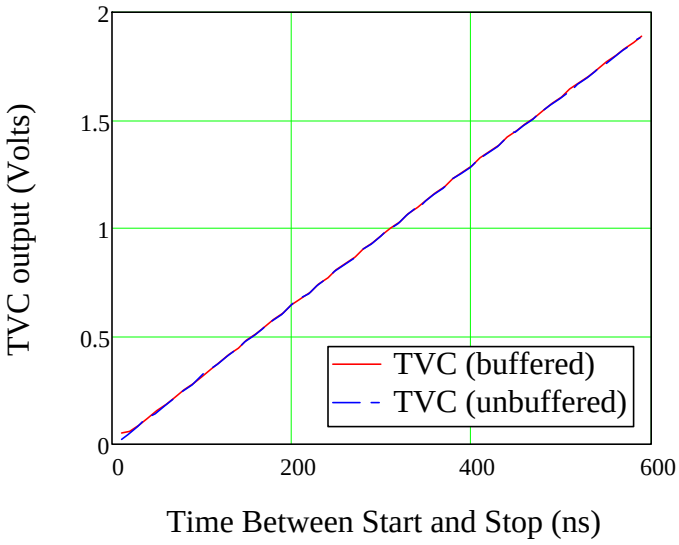


Fig. 1: The TVC buffered and unbuffered outputs as function of time between start and stop when operating in 500 ns range mode (27C and "typical" process parameters)

The differential output from the chip is plotted in Fig. 2. Note the full-scale differential range is near 5 Volts and will nicely match the range of the ADC (LTC1865) selected for use in the "super PSD" board.

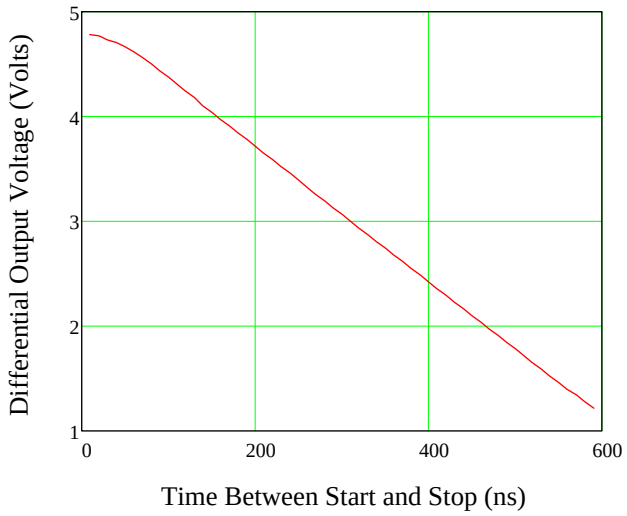


Fig. 2: The differential output at pins of chip (10K and 10 pF load) as function of relative time between start and stop pulses (27C and "typical" process parameters).

Before looking at the more important "differential linearity" plot, we present an "integral linearity" plot (Fig. 3). The units for the y-axis are nanoseconds. The TVC output, the output of the local buffer, and the differential output of the chip are all plotted in Fig. 3. The plot was obtained by performing a linear regression (over range from 160ns to 460 ns) and looking at the absolute difference between the data and the "best-fit" line. Note that the performance of our redesigned local buffer does not limit the performance for small times (the chip's output buffer does!). Also observe that the absolute error is less than +/- 1 ns for times between 100 and 500 nsec.

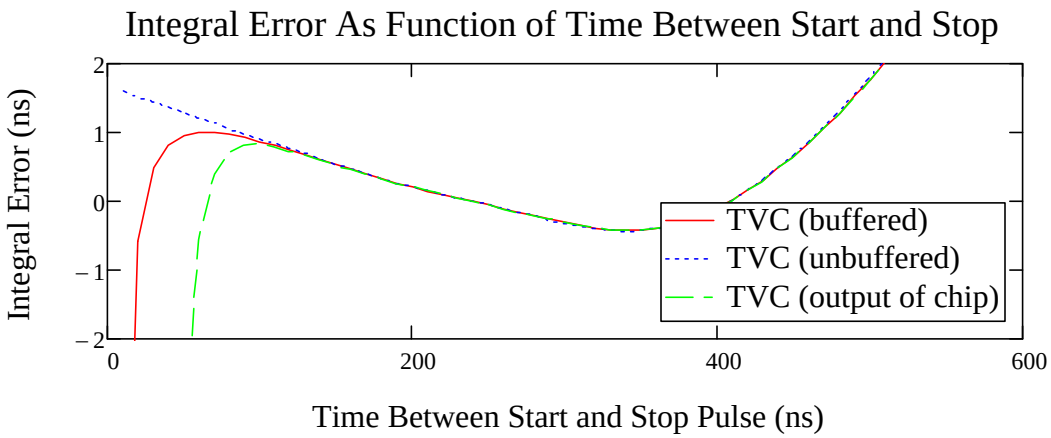


Fig. 3: Integral error as function of time between start and stop when TVC is operated in 500 ns range mode (27C and "typical" process parameters).

The more important differential linearity plot is presented in Fig. 4 below. Here is an explanation of how the graph was obtained. As already described the time between the start and stop pulses was increased in increments of 10 ns. Ideally the difference in TVC voltage between and two consecutive TVC outputs should always be the same and should always represent 10 ns. Rather than plot this difference in voltage, we converted the difference in *voltage* (representing 10 ns) into a *time* utilizing the slope obtained from the regression analysis used in determining the TVC's integral linearity characteristics. We then subtracted 10 ns since the difference if the TVC were ideal would be 10 ns. Finally we divided the resulting error by 10 ns (size of increment). Hence, we plot the differential error (ns / ns) on the y-axis versus the time (ns) between the start and stop pulses on the x-axis in Fig. 4.

If the TVC were perfect, one would expect a horizontal line (y = 0) indicating that the voltage encoding a 10 ns time difference is always the same (i.e. 10 ns with no variation). For times between about 100 ns and 300 ns this is nearly

what we observe. After 300 ns, however, we see the differential error increasing in magnitude (but negative). Since the differential error is negative, we conclude that the TVC response is slightly compressive. As the relative time between the start and stop pulses grows larger, the difference in time returned by the TVC is slightly understated.

Here is how the graph may be interpreted. If two events occur at around 500 nsec prior to the assertion of the "common stop" signal, but with a relative time difference of 1 nsec, then Fig. 4 suggests that the non-linear characteristics of the TVC will introduce an error of approximately 25 ps. If the two events occur at around 250 ns, then essentially no error (< 1 ps or so) would be introduced

It is worth noting that the three curves (unbuffered TVC, buffered TVC, differential output from chip) lie virtually on top of one another, and we conclude that the differential non-linearity characteristic is a result of the TVC circuit itself and not attributable to the characteristics of the local channel buffer nor to the differential buffer which drives the TVC output off-chip.

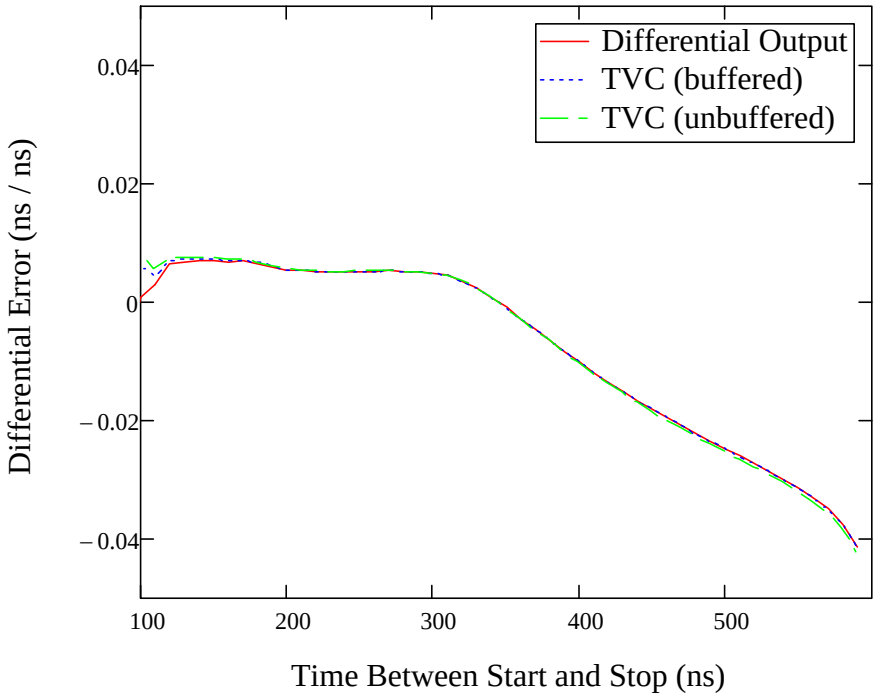


Fig. 4: Differential error (ns /ns) as function of time between start and stop when TVC is operated in 500 ns range mode (27C and "typical" process parameters)

We also looked at the differential error performance for “worst case power” (see Fig. 5) and “worst case speed” process parameters (see Fig. 6).

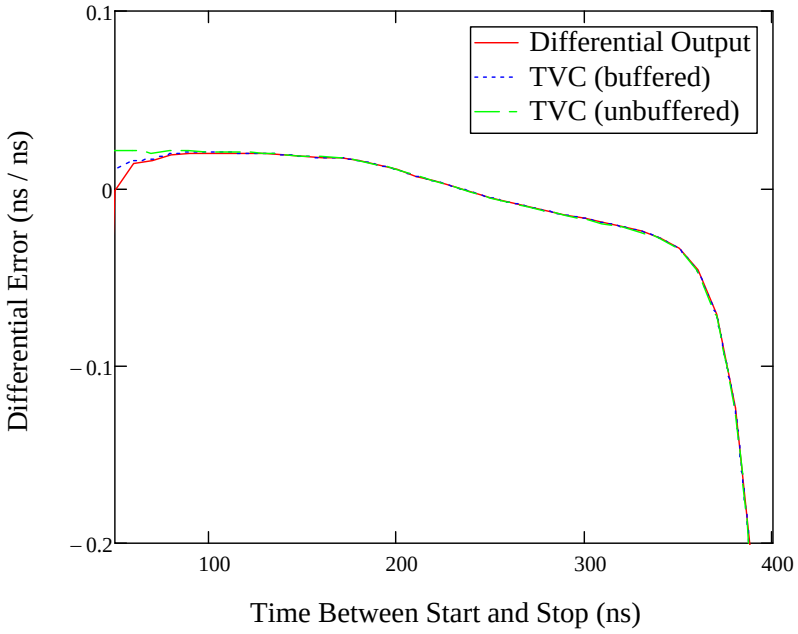


Fig. 5: Differential error (ns) as function of time between start and stop (27C and “worst case power” process parameters)

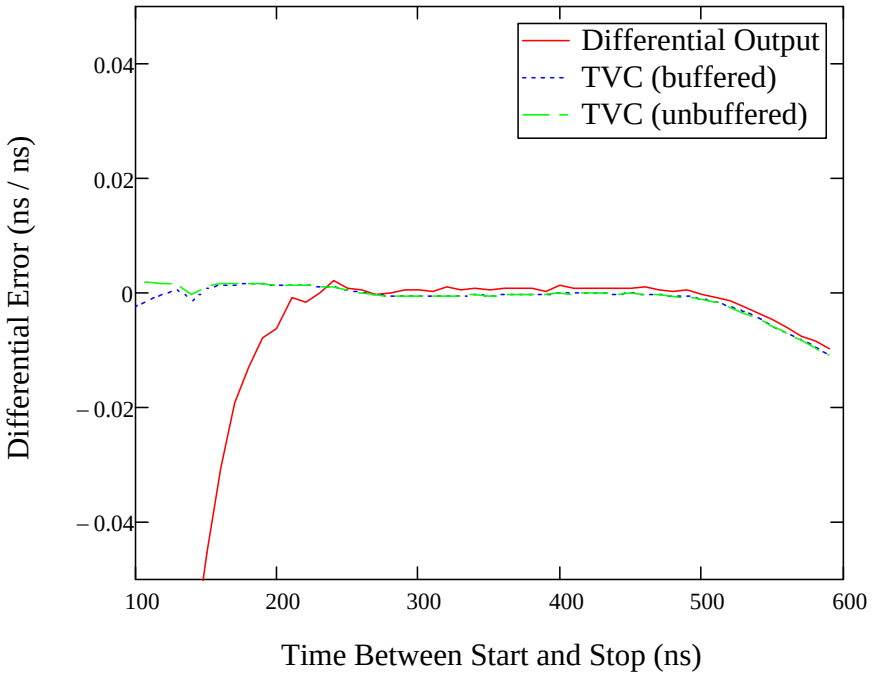


Fig. 6: Differential error (ns) as function of time between start and stop (27C and “worst case speed” process parameters).

II) TVC Linearity (2000 ns range mode)

In this section of the report we look at the performance of the TVC circuit when it is operating in the 2000 ns range mode (27C and "typical" process parameters).

Shown below is a plot (Fig. 7) of the raw (before our re-designed channel buffer) output from the TVC along with the output of the re-designed buffer. The difference in time between the "start" and "stop" signals is plotted on the x-axis. The slope is about 0.8 mV per ns. The full-scale voltage (little less than 2V) corresponds to about 2250 ns. As previously demonstrated, there is no notable difference between the buffered and un-buffered outputs.

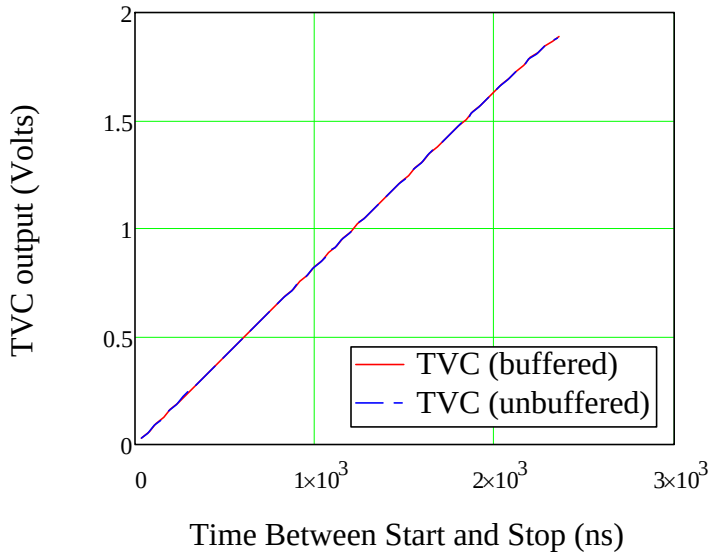


Fig. 7: The TVC buffered and unbuffered outputs as function of time between start and stop in 2000 ns range mode (27C and "typical" process parameters)

We now look at the integral linearity characteristics of the TVC when operated in the 2000 ns range mode. The TVC output, the output of the local buffer, and the differential output of the chip are all plotted in Fig. 8. The plot was obtained by performing a linear regression (over range from 440 ns to 1600 ns) and looking at the absolute difference between the data and the "best-fit" line.

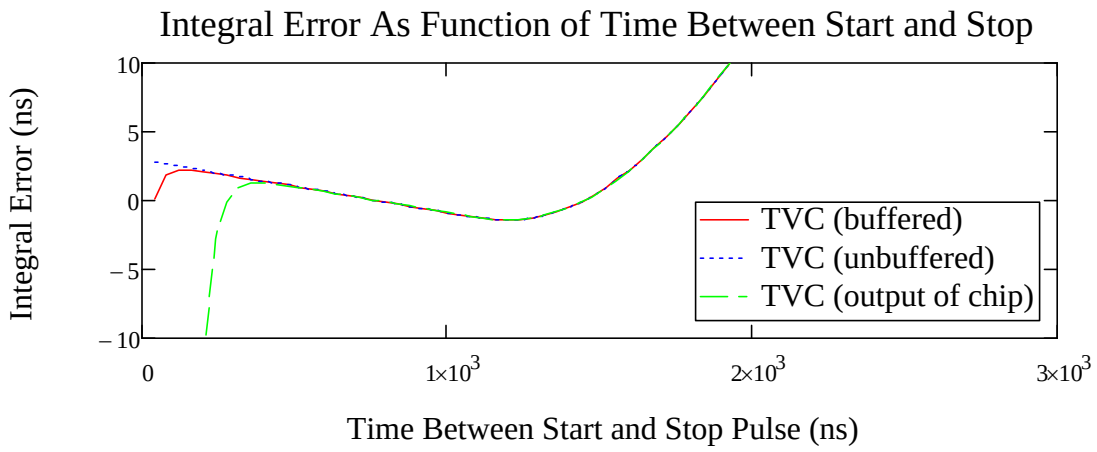


Fig. 8: Integral error as function of time between start and stop when TVC is operated in 2000 ns range mode (27C and "typical" process parameters).

The differential linearity plots are presented in Figs. 9, 10, and 11. The time increment was 40 ns (as opposed to 10 ns for the 500 ns range mode).

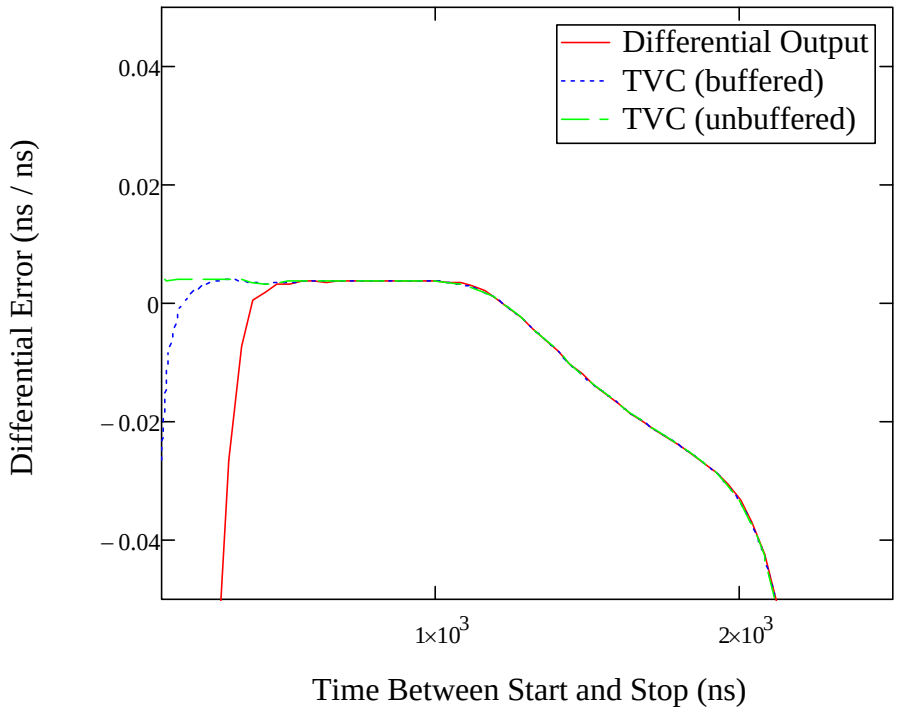


Fig. 9: Differential error (ns /ns) as function of time between start and stop when TVC is operated in 2000 ns range mode (27C and "typical" process parameters)

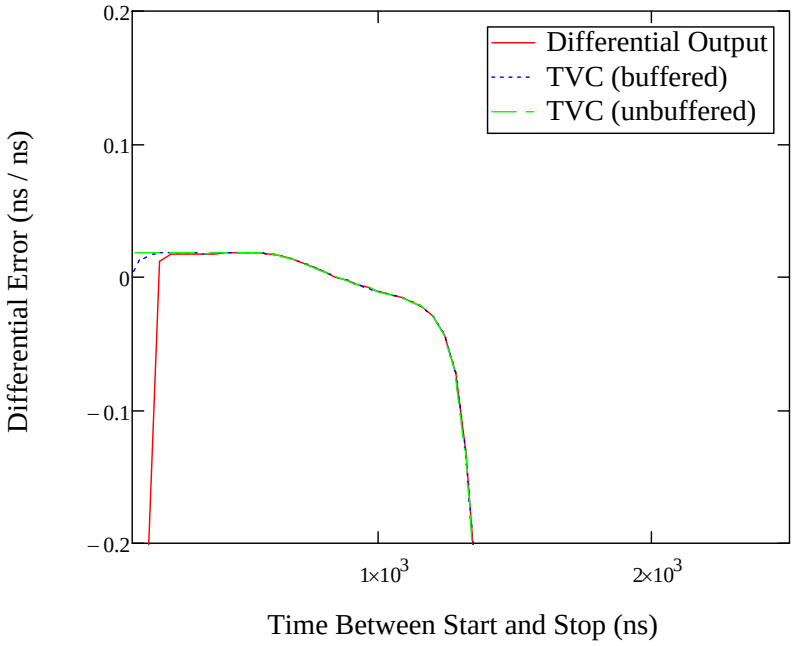


Fig. 10: Differential error (ns) as function of time between start and stop (27C and “worst case power” process parameters)

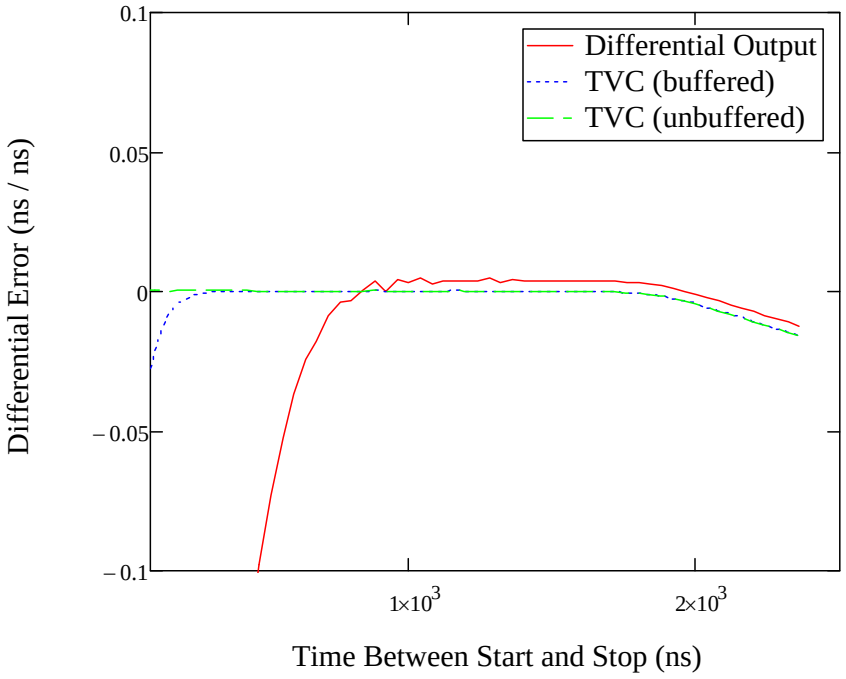


Fig. 11: Differential error (ns) as function of time between start and stop (27C and “worst case speed” process parameters)

III) TVC Temperature Dependence

In this section of the report we examine the TVC's temperature sensitivity. Recall, in the current version of the PSD8C chip, the temperature sensitivity is quite severe (about 1 ns / C). The temperature characteristics of the TVC circuit are vastly better now!!!!

We will start by looking the TVC when operated in the 500 ns range mode. As one can clearly see from Fig. 12, the results for the 0C, 27C, and 50C simulation runs lie virtually on top of one another. In Fig. 13 we present a "difference" plot.

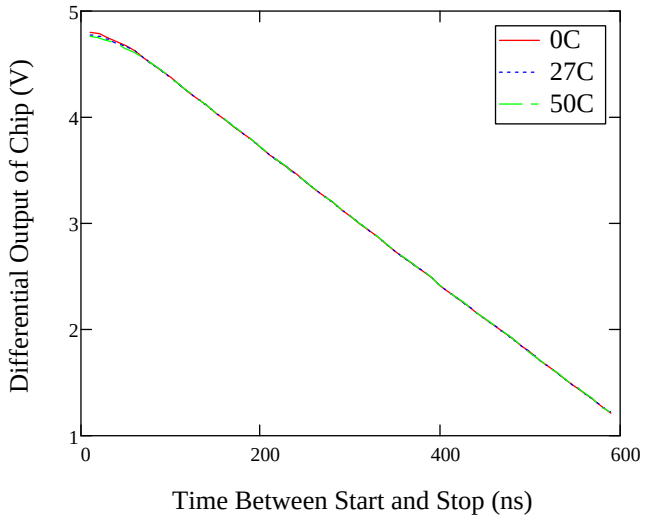


Fig. 12: Differential output voltage from chip as function of time between start and stop pulses (500 ns range, "typical" process parameters).

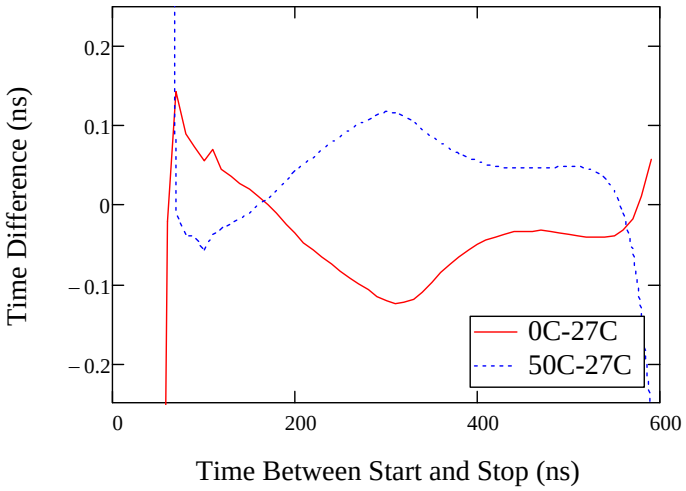


Fig. 13: Using the 27C run as our reference, we look at the time shift (ns) that would occur if temperature was changed to 0C or to 50C

From Fig. 13 we conclude that the temperature dependence is much less (under 5 ps / C).

We repeated the experiment for the TVC being operated in the 2000 ns range mode and “typical” process parameters. See Fig. 14 and Fig. 15.

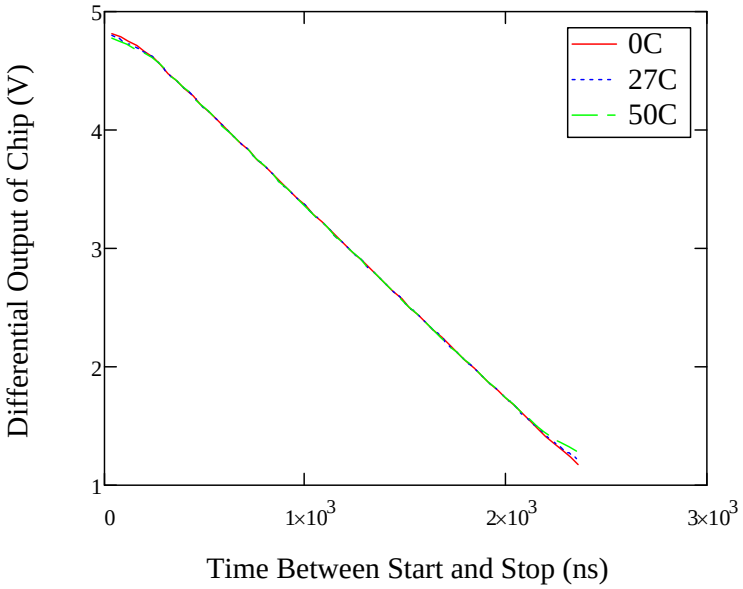


Fig. 14: Differential output voltage from chip as function of time between start and stop pulses (2000 ns range, “typical” process parameters).

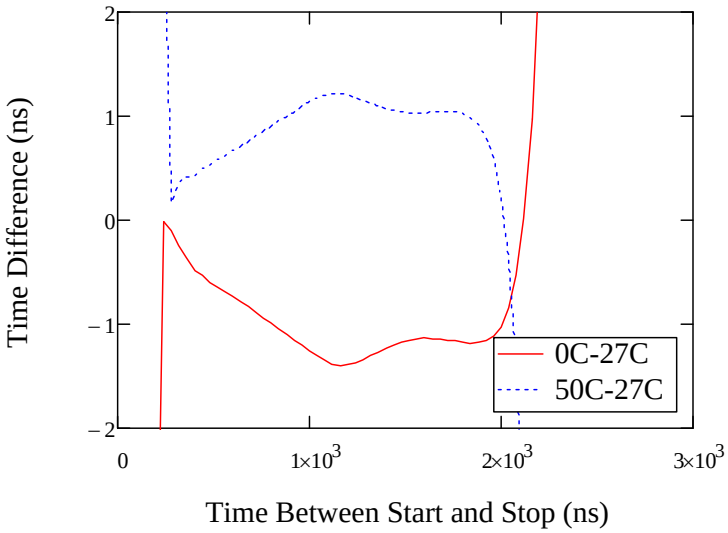


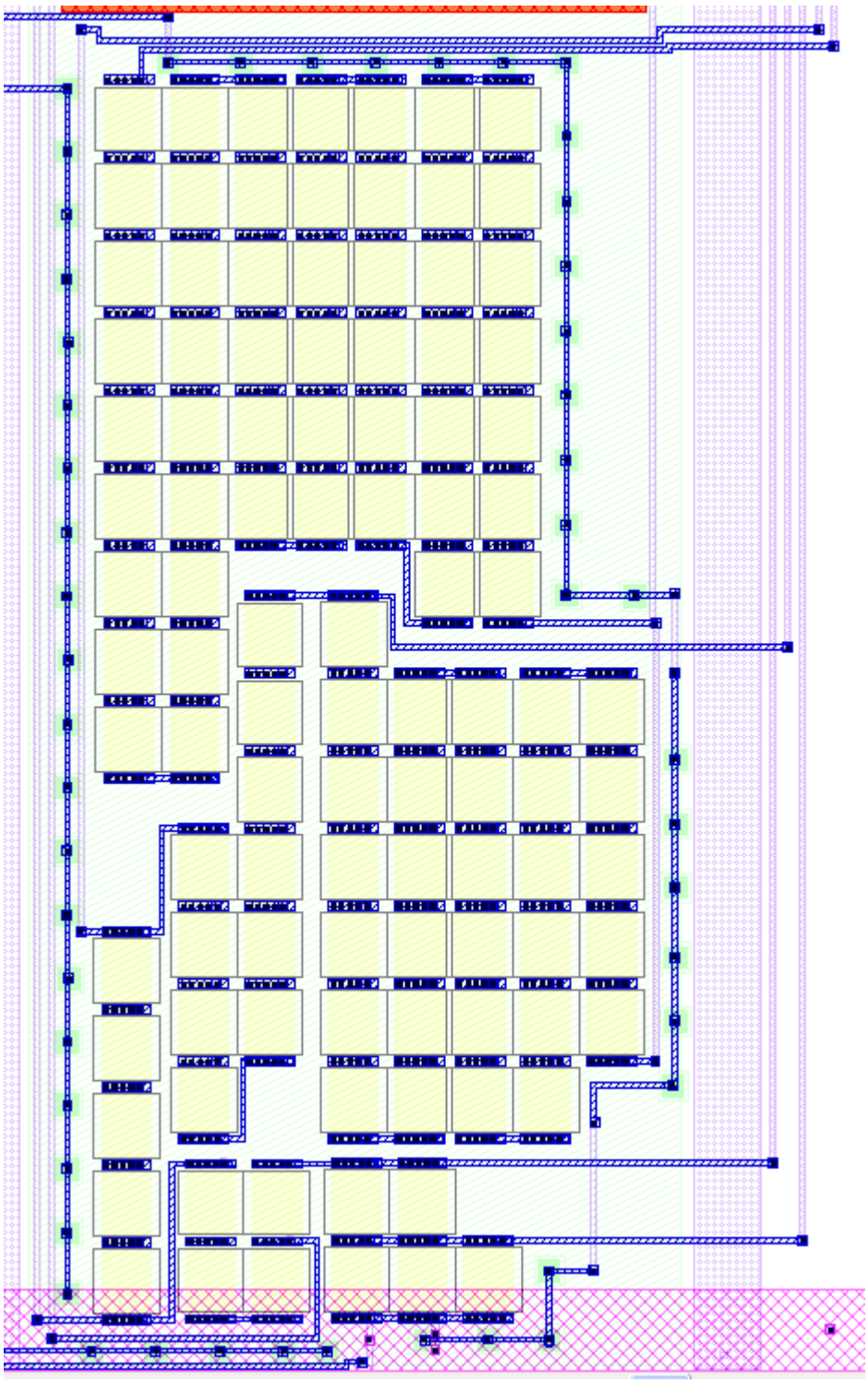
Fig. 15: Using the 27C run as our reference, we look at the time shift (ns) that would occur if temperature was changed to 0C or to 50C

From Fig. 15 we conclude that the temperature dependence is approximately 40 ps/C when the TVC is operated in the 2000 ns range mode. While not as good as when operated in the 500 ns range mode, this is still quite good.

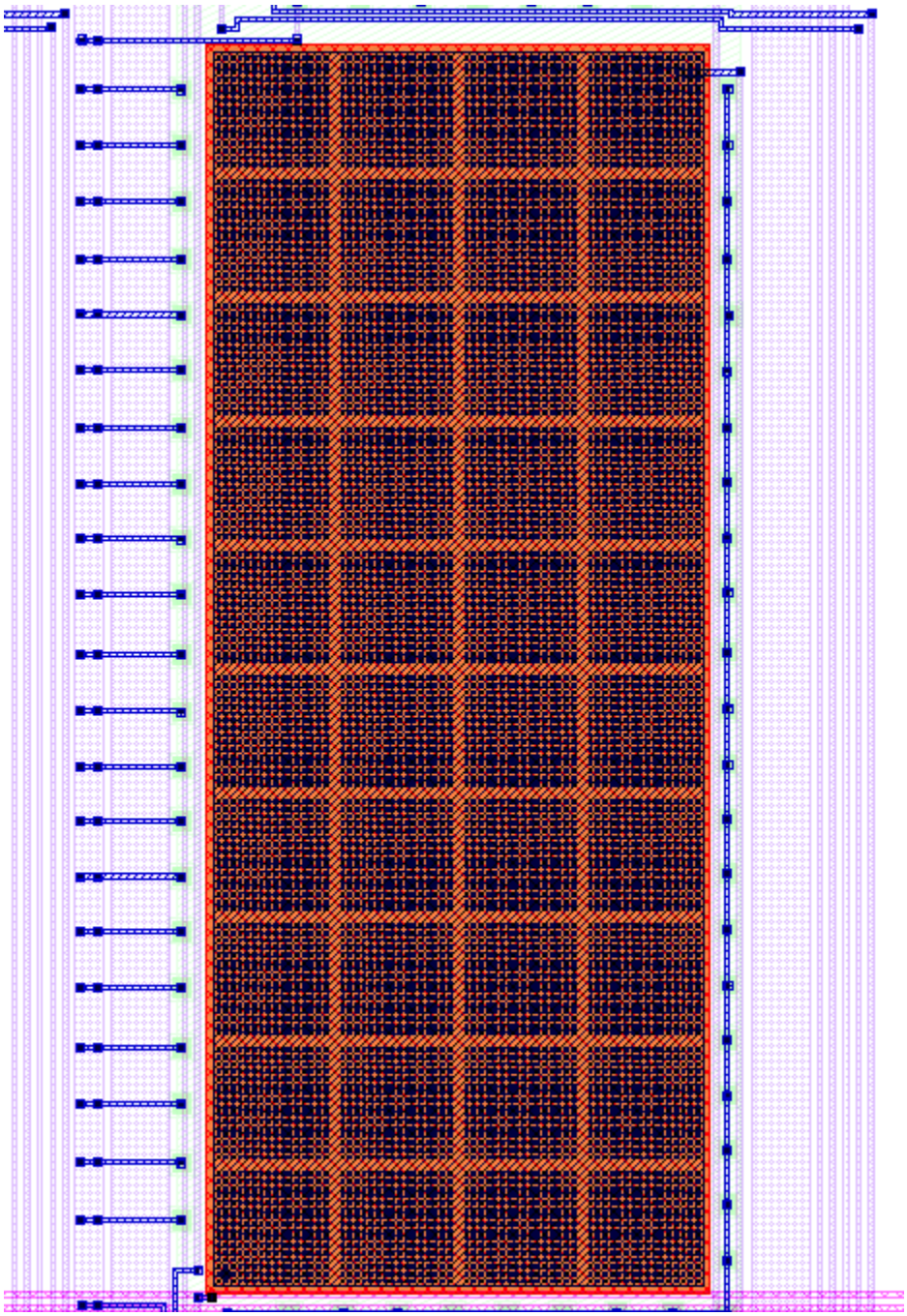
APPENDIX A

LAYOUT

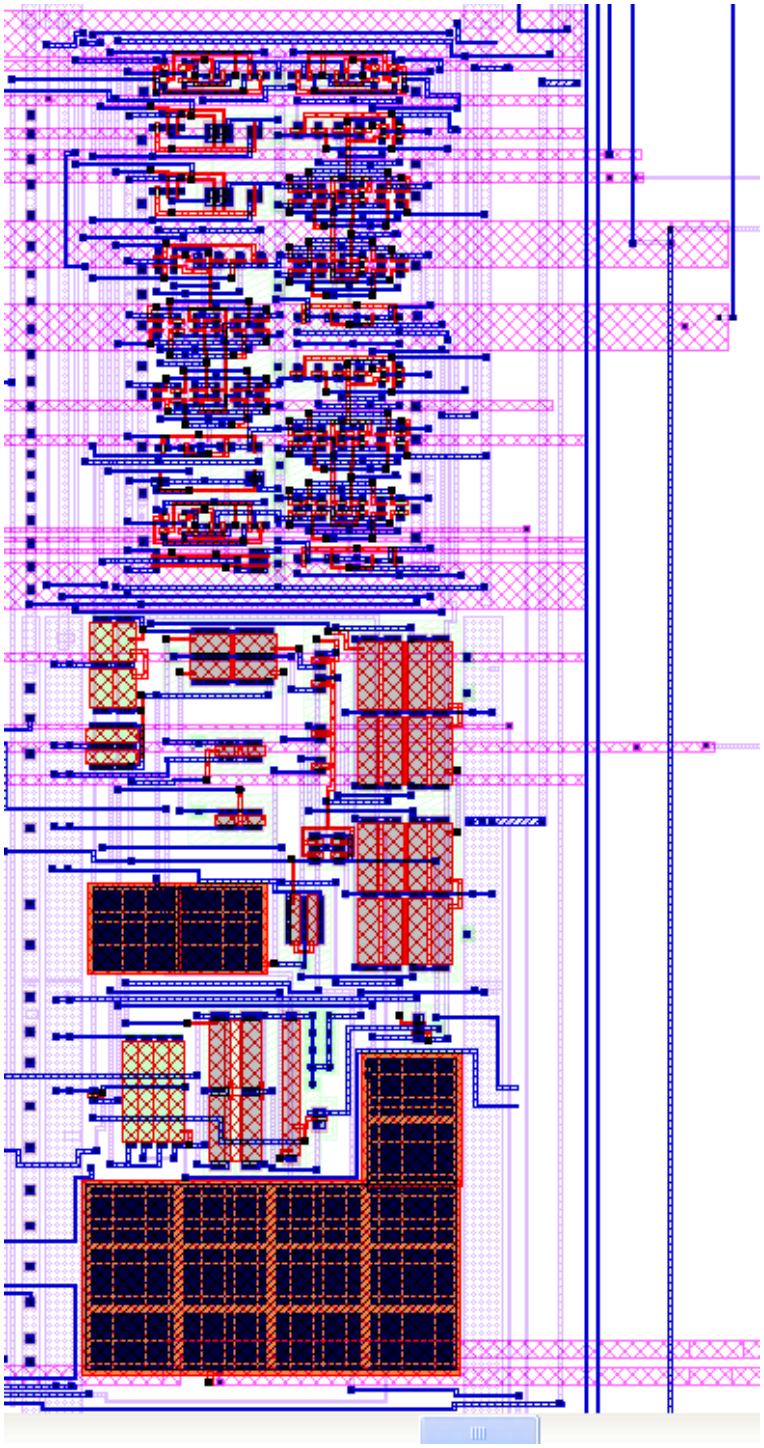
This is integrator resistor array layout, clearly showing NWELL shield. The NWELL shields bottom surface of POLY II resistors from noisy P-substrate.



A NWELL shield was added underneath the integrating capacitor, also.



The layout of the revised TVC circuit appears on the next page. The redesigned digital logic is clearly visible near top. The TVC core is located at the bottom. Note the addition of a couple of additional unit capacitors to extend range by about 10 %. Sandwiched between these two structures is the local buffer (with 0.5 pF compensation capacitor clearly visible. The local buffer is a two stage design with a PFET input stage.



The AVDD pin for the lower right quadrant of the chip is shown below. Note that the connection to the pin is made through 3 separate lines. The wide line feeds the majority of the circuits in this quadrant of the IC. One of the thinner lines feeds the revised TVC circuit shown for one of the quadrant's channels while the other line feeds the neighboring channel. The only shared impedance is now that associated with the pad itself along with the AVDD bonding wire.