Final Report for Period: 09/2008 - 02/2009 **Submitted on:** 05/21/2009

Principal Investigator: Engel, George L. **Award ID:** 0618996

Organization: Southern Ill U Edwardsvill

Submitted By:

Engel, George - Principal Investigator

Title:

Development of a Pulse Shape Discrimination CMOS ASIC

Project Participants

Senior Personnel

Name: Engel, George

Worked for more than 160 Hours: Yes

Contribution to Project:

Dr. Engel supervises the development of the ASIC under development for this NSF project.

Name: Sobotka, Lee

Worked for more than 160 Hours: Yes

Contribution to Project:

Dr. Sobotka leads the Washington University nuclear physics group that is helping specify how the ASIC under development should operate.

Name: Famiano, Michael

Worked for more than 160 Hours: Yes

Contribution to Project:

Dr. Famiano will use the ASIC, currently under development, in an upcoming experiment.

Post-doc

Graduate Student

Name: Hall, Michael

Worked for more than 160 Hours: Yes

Contribution to Project:

Michael Hall worked as a graduate research assistant since the start of the project (Sept. 2006). Mike was one the principal designers of the integrated circuit which we developed. Mike defended his thesis on the topic (December 2007). Mike's support for year came directly from the NSF grant. The support consisted of tuition remission and a monthly stipend of $920. Mike completed his thesis and graduated in December. Mike is now a doctoral student in the Computer Science and Engineering Department at Washington University in Saint Louis.

Name: Proctor, Justin

Worked for more than 160 Hours: Yes

Contribution to Project:

Justin Proctor worked as a graduate research assistant since the start of the project (Sept. 2006). Justin was one of the principal designers of the integrated circuit. Justin defended his thesis on the topic (December 2007). Justin's support came directly from the NSF grant. The support consisted of tuition remission and a monthly stipend of $920.

Justin graduated in December 2007 and is now working for a company

here in the St. Louis area.

Name: Valluri, Nagendra

Worked for more than 160 Hours: Yes

Contribution to Project:

Nagendra (Hari)Valluri worked on the project as a graduate research assistant from June 1, 2007 until August 2008. Hari was responsible for the physical layout of the digital circuits used in the integrated circuit developed under this NSF grant. The support consisted of tuition remission and a monthly stipend of $920.

Name: Dasari, Dinesh

Worked for more than 160 Hours: Yes

Contribution to Project:

Dinesh Dasari worked on the project as a graduate research assistant from May 15, 2007 - August 15, 2008. Dinesh was responsible for the physical layout of the analog circuits used in the integrated circuit under development for the this NSF project. Dinesh's support during summer 2007 came from state of IL matching funds ($10,000) that the university awarded me to be used on the project. After that he was supported by the NSF grant. The support consisted of tuition remission and a monthly stipend of $920.

Name: Ngyuen, Nam

Worked for more than 160 Hours: Yes

Contribution to Project:

Nam Ngyuen worked as a graduate research assistant on this project from Jan. 2008 - Dec. 2008. Nam was a quarter-time graduate assistant (10 hours/week) from January 2008 until May 2008. Beginning in the summer he was made a half-time assistant (20 hours/week). Nam designed a I2C interface for the custom integrated circuit under development. Nam wrote a thesis on his work and graduated in December 2008. Nam's support comes directly from the NSF grant. The support consisted of tuition remission and a monthly stipend of $460 while he was quarter-time and $920 when he was promoted to half-time.

Name: Yelchuri, Naga

Worked for more than 160 Hours: Yes

Contribution to Project:

Naga Yelchuri worked as a graduate research assistant on this project from Jun 9, 2008 - Feb. 28, 2009. He was a half-time assistant (20 hours/week). Naga plans to write a thesis on his work (design of a 12-bit ADC) and graduate in 2009. Naga's support came directly from the NSF grant. The support consisted of tuition remission and a monthly stipend of $920 (later $1000 per month).

Name: Reddy, Sruthi

Worked for more than 160 Hours: Yes

Contribution to Project:

Sruthi Laxma Reddy worked as a graduate research assistant on this project from May 15, 2008 - August 15, 2008. She was a half-time assistant (20 hours/week). She only worked on the project during summer 200). She assisted the PI in maintaining the CAD tools and the UNIX boxes that we use in the project. She also helped train students use the IC design tools. Sruthi's support came directly from the NSF grant. The support consisted of tuition remission and a monthly stipend of $920.

Name: Paul Antony, Arokia

Worked for more than 160 Hours: Yes

Contribution to Project:

Arokia has worked as a graduate research assistant on this project since May 15, 2008. He was a half-time assistant (20 hours/week). He only worked on the project during summer 2008. He assisted the PI in accomplishing many miscellaneous tasks; for example, drawing figures for papers/reports, setting up a second IC design lab (we outgrew our original research room), and preparing/maintaining documents associated with the project. Arokia's support came directly from the NSF grant. The support consists of tuition remission and a monthly stipend of $750.

Name: Yerra, Taraka

Worked for more than 160 Hours: No

Contribution to Project:

Taraka Neelakan Yerra worked as a graduate research assistant on this project from Jan. 15 to Feb 28, 2009 . He was a half-time assistant (20 hours/week). Neel's support comes directly from the NSF grant. The support consisted of a tuition remission and a monthly stipend of $1000. He wrote a synthesizable Verilog description of the PSD readout electronics. The code will be used to create a PSD chip emulator.

Undergraduate Student

Technician, Programmer

Other Participant

Research Experience for Undergraduates

Name: Brown, James

Worked for more than 160 Hours: Yes

Contribution to Project:

James Brown is an undergraduate who worked on the project last summer (2007). James learned how to use AutoCAD and then prepared a bonding diagram for the integrated circuit under development. James also helped developed the project's web site during summer 2007. James continued to work on the project as an undergraduate in the Fall 2007 and Spring 2008 semesters. James continued work on materials displayed on the project's website and made a presentation about the project at the Argonne Undergraduate Symposium in November 2007. James' support came directly from the NSF grant. James worked 10-20 hours per week at a rate of approximately $13.00/hour.

Years of schooling completed: Junior

Home Institution: Same as Research Site

Home Institution if Other:

Home Institution Highest Degree Granted(in fields supported by NSF): Master's Degree

Fiscal year(s) REU Participant supported: 2007

REU Funding: REU supplement

Organizational Partners

Washington University

Western Michigan University

Other Collaborators or Contacts

Activities and Findings

Research and Education Activities:

Findings:

Training and Development:

The project has provided several graduate students (Mike Hall, Justin Proctor, Nagendra Hari Valluru, Dinesh Kumar Dasari, Sruthi Laxma Reddy, Nam T. Ngyuen, Naga C. Yelchuri, and Antony Paulan) with an opportunity to work on the development of a mixed-signal integrated circuit. Skills provided to students working on this project include: report preparation, maintaining IC design CAD tools, physical layout of both analog and digital integrated circuits, design of digital and analog circuits (operational amplifiers, voltage and current references, digital-to-analog converters), and modeling of systems using both VerilogA and Matlab. Many (Dasari, Valluru, Ngyuen, and Yelchuri)of these students are working on (or have completed - Proctor and Hall) Master Theses. Justin Proctor and Michael Hall made presentations at a graduate symposium held on the SIUE campus in April 2007. Mike Hall also made a presentation at the CSUI symposium held at Argonne National Laboratory in November 2007.

The project also has allowed an undergraduate and a minority student (James Brown) to become involved in a research project and interact with graduate students. James learned how to use AutoCAD to produce bonding diagrams for integrated circuits and on how to create web pages. James made a presentation at a conference this November at Argonne National Laboratory and also presented a poster at the ILSAMP conference near Chicago in October 2007.

Outreach Activities:

In February 2007 and February 2008, the SIUE School of Engineering held an Open House. Many (several hundred) prospective students and parents toured the engineering building. As part of the open house we (myself and graduate students) showcased the IC Design Research Laboratory. We explained to the visitors the goals and objectives of the NSF project and demonstrated how the integrated circuit under development as part of this NSF grant is designed. We also explained that in addition to the IC being used in nuclear physics experiments how it might someday be used in systems for detecting radiation released as part of a terrorist threat.

Journal Publications

Books or Other One-time Publications

Michael Hall, "Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation
", (2007). Thesis, Published
Bibliography: Masters Thesis, December 2007, can be found in Southern Illinois University Edwardsville Lovejoy Library

Justin M. Proctor, "Design of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Required
", (2007). Thesis, Published
Bibliography: Master Thesis, December 2007, available in Southern Illinois University Edwardsville Lovejoy Library

Dinesh Dasari, "Design of On-chip ADC for Custom ASICs Used in the Detection of Ionizing Radiation", (2008). Thesis, Accepted
Bibliography: Masters Thesis. Available at SIUE Lovejoy Library.

Nagendra Sai Hara Krishna Valluru, "Design of a RAM Buffer for Multi-channel Integrated Circuits
Used in the Detection of Ionizing Radiation
", (2008). Thesis, Accepted
Bibliography: Masters Thesis. Available at SIUE Lovejoy Library.

Nam Nguyen, "Design of I2C Interface for
Custom ASICS
Used in the Detection of
Ionizing Radiation

", (2008). Thesis, Published
Bibliography: Available at SIUE Lovejoy
library

Web/Internet Site

URL(s):

www.ee.siue.edu:~gengel/PSD.htm

Description:

This site serves as a repository for reports related to the progress of the project. It also provides items of interest to other researchers in the field. For example, the site contains a large collection of Cadence OCEAN scripts which were developed to evaluate the performance of circuits used in the project. The site also contains MathCAD worksheets that were developed to design key components on the IC. The site also contains schematics and other design related data that is available to those interested in the details of the project and/or as examples that may be of use to engineers working on related activities.

Other Specific Products

Contributions

Contributions within Discipline:

A group at Los Alamos (LANL) has become very interested in our PSD chip. They would like to use the chip in the work they do at LANL. We have been talking with Mark Wallace and Edward McKigney among others. They recently (March 2009) have decided to fund further development of our PSD system centered around the PSD8C chip which was developed as part of this NSF grant.

Contributions to Other Disciplines:

Contributions to Human Resource Development:

Contributions to Resources for Research and Education:

Contributions Beyond Science and Engineering:

Conference Proceedings

Categories for which nothing is reported:

Activities and Findings: Any Research and Education Activities
Activities and Findings: Any Findings
Any Journal
Any Product
Contributions: To Any Other Disciplines
Contributions: To Any Human Resource Development
Contributions: To Any Resources for Research and Education
Contributions: To Any Beyond Science and Engineering
Any Conference

2008 NSF Final Report (May 2009) for Grant #06118996

This final report for Grant #06118996 is divided into three sections. In Section I of this report we provide a brief overview of the project along with a list of objectives that we had hoped to accomplish during the grant period. In Section II, we describe how successful we were in meeting these grant objectives. Since the details of the design and simulation of the micro-chip, which is the subject of this grant, have been discussed in the interim reports, in this final report we concentrate on a prototype system which makes use of this custom circuit. Finally, in Section III we briefly describe how the work performed as part of the NSF grant will continue over the next two years.

I. Project Overview

The objective of the NSF grant was to produce a micro-chip that would complement an existing (shaped and peak-sensing) analog chip (called **HINP16C**) developed a few years earlier by our laboratory, with one capable of particle identification using pulse-shape discrimination (PSD). The PSD integrated circuit (IC) which we proposed to develop was to be suitable for use with both CsI(Tl) ("slow", used for charge-particle discrimination) and liquid scintillator ("fast", used for neutron-gamma discrimination) detectors.

Over the two-year grant period (Sept. 1, 2006 – Aug. 31, 2008) we had proposed the following activities:

1) design, simulate, layout, and fabricate an IC capable of PSD,
2) train several graduate and undergraduate students,
3) build and test a prototype system,
4) use the IC in an experiment,
5) make a "production chip",
6) and distribute test stations to other interested groups.

In short, we argued in the proposal that successful completion of this project would add a powerful new capability to the CMOS ASIC "tool box" for radiation detection instrumentation, make large detectors arrays with important information in the pulse shape more cost effective, and would train several graduate and undergraduate students in mixed-signal (CMOS) design.

Because testing of the PSD8C IC could not be completed by August 31, 2008 we asked for, and were granted, a 6 month extension. Hence, the grant period officially ended on February 28, 2009.

II. Project Accomplishments

In this section we will demonstrate how all of our project objectives were successfully met. We will address each of the aforementioned objectives.

Design, simulate, layout, and fabricate an IC capable of PSD.

Work on the integrated circuit began in September, 2006. The IC was designed and carefully simulated before eventually being laid out and fabricated. The IC was christened PSD8C (Pulse Shape Discrimination – Eight Channel). The process of designing, simulating, and laying out PSD8C took significantly longer than initially thought, in large part because we were not able to re-use as many of the circuits from our earlier HINP16C design as we had initially anticipated. Moreover, in order to obtain a more compact layout very little of the HINP16C layout was used in crafting PSD8C. Only the layout for the HINP16C primitive digital cells was directly used in PSD8C. A plot of the final layout for the PSD8C IC in presented in Figure 1 below.

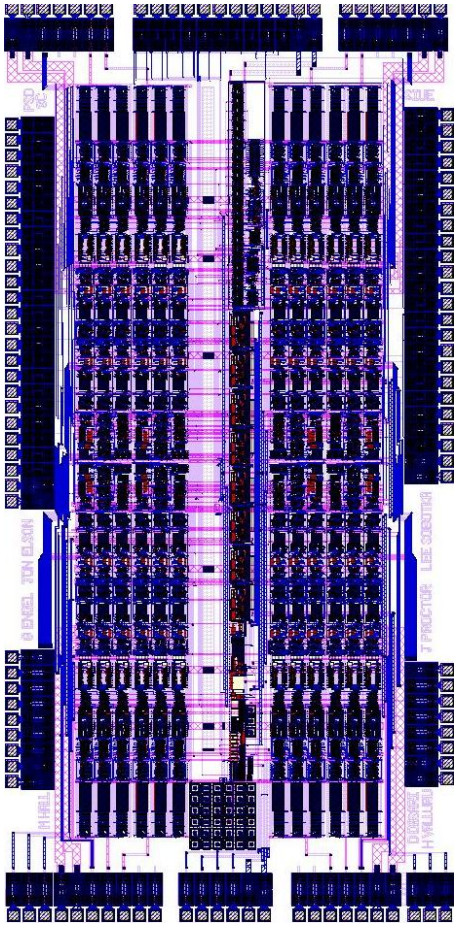


Figure 1: Final layout for PSD8C chip

The PSD8C design employs a technique known as pulse shape discrimination (PSD) to classify the incident radiation. Each of the eight channels is composed of a time-to-voltage converter (TVC) with two time ranges (0.5 μsec, 2 μsec) and three sub-channels. Each of the sub-channels consists of a gated integrator with 8 programmable charging rates and an externally programmable gate generator that defines the start (with 4 time ranges) and width (with 4 time ranges) of the gate relative to an external discriminator signal. The chip supports 3 triggering modes. The IC produces four sparsified analog pulse trains (3 integrator outputs and 1 TVC output) with synchronized addresses for off-chip digitization with a pipelined ADC. The IC possesses two bias modes and occupies an area of approximately 2.8 mm x 5.7 mm. It has a power dissipation of 135 mW in the high-bias mode (for use with "fast" detectors) and 60 mW in the low-bias mode (for use with "slow" detectors).

PSD8C was submitted to MOSIS (MOS Implementation Services) for fabrication in February 2008. The chip was fabricated in the AMIS 0.5-micron NWELL (C5N) process. The die area was 15.5 mm^2. The 40 dies that we received were packaged in a 128-lead plastic thin quad flat pack (LQFP128A) with a cavity size of 14 mm x 14 mm. Fabrication cost was $7776. The packaging cost for the 40 dies was $2600. Thus, the final cost to obtain 40 packaged parts was $10,376. This was a few thousand dollars less than what we had budgeted because the IC turned out to be slightly smaller than what we had originally estimated. Packaged parts arrived from MOSIS in May 2008 and testing of the ICs was begun shortly thereafter.

Train several graduate and undergraduate students.

During the grant period, 9 graduate students and 1 undergraduate student (a minority student) worked on this NSF project. Five of the nine graduate students wrote Masters Theses. Some of the students (Michael Hall and Justin Proctor) presented there work at the 2007 SIUE Graduate Symposium held each April on the campus of Southern Illinois University Edwardsville (SIUE). The theses were:

Title:	Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation
Author:	Michael J. Hall
Date:	December 2007

Title:	Design of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Required
Author:	Justin M. Proctor
Date:	December 2007

Title:	Design of On-Chip ADC for Custom ASICs Used in the Detection of Ionizing Radiaiton
Author:	Dinesh K. Dasari
Date:	August 2008

Title:	Design of a RAM Buffer for Multi-Channel Integrated Circuits Used in the Detection of Ionizing Radiation
Author:	Nagendra K. Valluru
Date:	August 2008

Title:	Design of I^2C Interface for Custom ASICs Used in the Detection of Ionizing Radiation
Author:	Nam Nguyen
Date:	December 2008

James Brown, an undergraduate made a presentation at the Argonne Undergraduate Research Symposium November 2-3, 2007. The title of his talk was "Multi-Channel Integrated Circuits for Use in Nuclear Physics Experiments".

Build and test a prototype system.

The PSD8C chips have been successfully integrated into a prototype system. Our present implementation strategy is depicted in Figure 2. The detector outputs are initially routed to the ASD (Amplifier-Splitter-Delay) board. Each ASD board accommodates 16 detectors. The detector signals are split. The amplified but "non-delayed" signals drive a custom CFD (Constant Fraction Discriminator) board (CFD-32).

The outputs from the CFD-32 are in turn connected to the PSD chip board. The CDF logic signals are used to start the internal delay generators located on the PSD8C ICs. Each of the chip boards (CB)

services two PSD8C chips (i.e. 16ch/CB). "Delayed" versions of the detector signals drive the linear inputs on the pair of PSD8C chips residing on each of the chip boards. Each PSD chip produces 4 analog output pulse trains: 1 for timing (T) and 3 (A, B, C) associated with the three integrators comprising each channel.

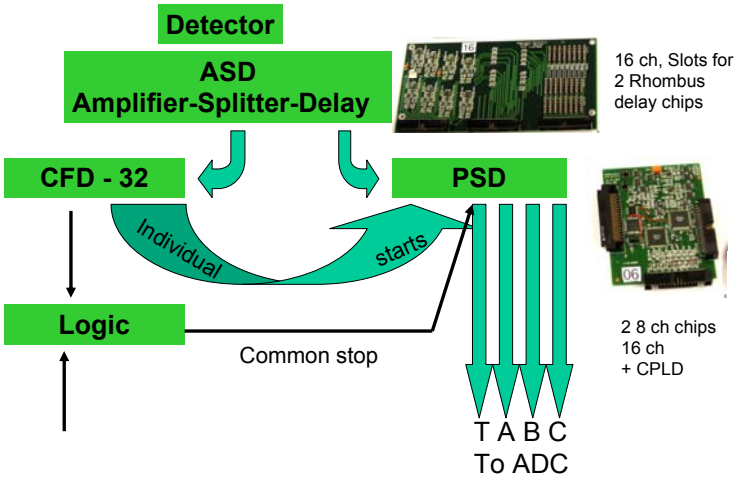


Figure 2: Present implementation strategy.

Our prototype system consists of a mother board (MB) which can house 16 chip-boards (i.e. 256 ch/MB) and is housed in a metal enclosure roughly the size of a shoebox. The 8 ASD boards are housed in an enclosure of similar size (i.e. 128 ch/ASD box). A PSD mother board, along with one PSD8C chip board and one ASD board are shown in Figure 3.

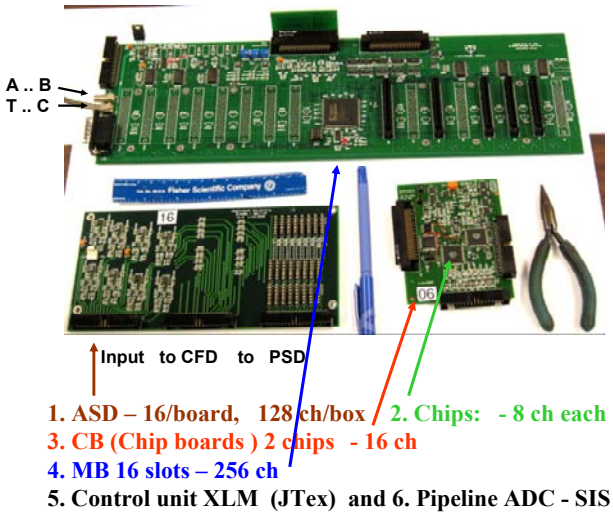
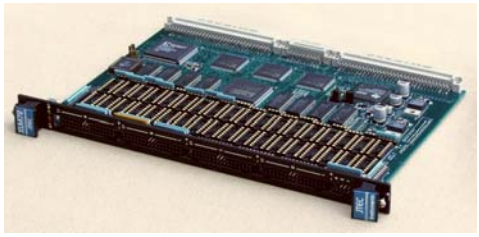


Figure 3: Components of the prototype system.

The analog pulse trains from the PSD8C chips are routed to the acquisition modules shown below in Figure 4.

VME ADC, 8 channels (4 pairs), **14-bit** differential, pipeline, from SIS/Struck, http://www.struck.de

Present ACQ modules



VME address and control module, XLM-80 designed by Jan Toke, Univ. of Rochester, www.JTEC-Instruments.com

Figure 4: Acquisition modules currently in use.

Scope traces of some of the analog outputs from a representative PSD8C chip are presented in Figure 5. A lot of effort and time went into testing and characterizing the performance of the PSD8C chip before integrating the IC into the system shown in Figure 4.

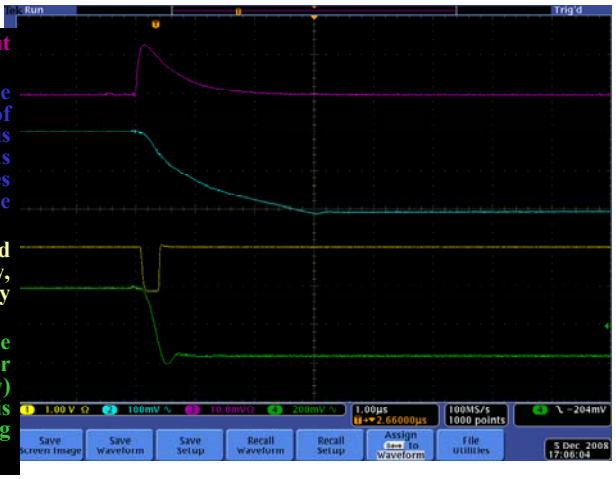
Some traces

The purple trace is the input tail pulse.

The blue trace is the accumulating integral of the total charge. This integration window is 3 us (not shown) and completes with an output charge voltage of about 200 mV.

The yellow trace is the second integration window, prompt and approximately 400 ns wide.

The green trace is the accumulated integral over this second (yellow) integration window. This integral, ends up being about 400 mV.



Each of the three integrations (of which the outputs of two are shown here) has its own output driver and thus can be linearly scaled as desired. These three outputs (e.g. blue and green), as well as a voltage proportional to the time difference between the channel trigger and an external reference, are sequenced into an off-chip pipeline ADC.

Figure 5: Scope traces for some of PSD8C outputs.

The prototype system has been used to take spectra. Some recent ^{22}Na spectra are presented in Figure 6. The quality of these energy spectra is equal to those of discrete component shaper systems. We believe that the PSD system is competitive with shaper systems as long as the pile-up rate in individual detectors is less than a few percent.

While all three integrators function as designed, we have not been able to test the quality of the PSD information from either CsI(Tl) or liquid scintillator as yet. We expect to do these tests in the summer of 09. This testing has been delayed due to present software limitations.

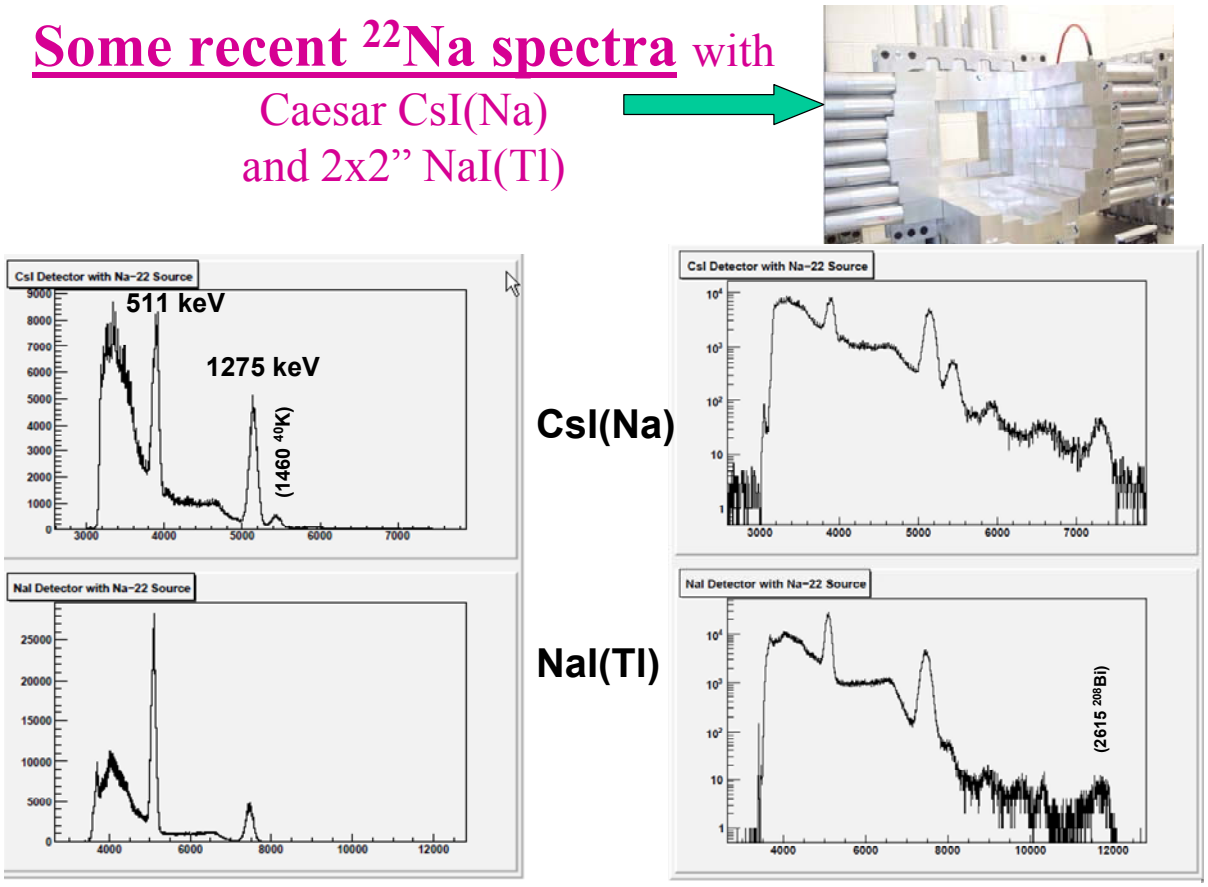


Figure 6: ^{22}Na spectra taken using the prototype PSD system. The top spectrum (displayed both in linear – left, and semilog – right) is from a CsI(Na) detector, from the Caesar array, while the bottom spectrum is from a NaI(Tl) detector (again shown in both linear and semilog.) The trigger rate for these data was 1kHz.

To date no significant deficiencies in PSD8C performance have been identified. In large part it performs as theory predicted and simulation confirmed (see the Proctor and Hall Theses available at http://www.ee.siue.edu/~gengel/PSD.htm). While some on-chip time cross-talk has been identified, it should not pose any problems in the first experiments planned where the PSD8C chip is to be used. In these early experiments, the inherent detector time resolution is around 10 nsec. The on-chip time cross-talk is just a couple of nsec when the TVC is in the 500 nsec range mode and perhaps 3-4 times more severe when the TVC operates in the 2 μs range mode.

Plans for use in experiments

The PSD system is presently being evaluated for use with the new Caesar array at the NSCL. Testing time is very limited, but it may be used in experiments this summer. (Most likely one on n/p knockout proposed by the WU group.) However, if not used in the first round of experiments with Caesar, it will be used in the second round. This new array can be run with conventional electronics, however this route does not provide dedicated electronics, suffers from a huge timing walk problem and is cumbersome.

In future years the WU group intends to use the PSD chip for the following arrays.

1. The WU neutron array (used with GAMMASPHERE).
2. A more granular version of the residue detector presently being planned by Prof. Sarantites [WU].
3. The Plastic-CsI(Tl) arrays built as multiplicity filters (by the WU and MSU reaction groups) for intermediate-energy reaction studies.

Make a "production chip"

In the NSF proposal we stated that

"*An 8-channel 'prototype' chip will be submitted for fabrication within 8 months of funding being approved and a revised, 16-channel 'production' version will be submitted after use of the 'prototype' IC in the experiment planned for the summer of 2007. The 'production' chip will address any deficiencies uncovered in the initial 'prototype' and will be made available to other groups.* "

As already mentioned, the 'prototype' chip took longer to develop than anticipated. Fortunately, since there were no significant deficiencies identified with the original prototype design, there really is no reason to fabricate a revised design at this time. Additional unpackaged PSD8C dies can be purchased from MOSIS for a modest cost and packaged.

The PSD8C was designed in such a way that it would be straight-forward to expand the existing eight channel design to sixteen channels. In fact all of the necessary input and output pads to support a sixteen channel design were included in the pad frame. Moreover, the existing readout electronics in PSD8C supports 16 channels. Only additional copies of existing changes would need to be placed and connected. A compelling need to expand to 16 ch has be made by a group at LANL (see below) but it makes little sense to do so until system size exceeds 256 ch.

Distribute test stations to other interested groups.

As mentioned above, a prototype system has been delivered to Michigan State University (MSU).

By June 8, we anticipate shipping a small (64ch) system to LANL. Mark Wallace and the Ed. McKigney (both or LANL) appreciated that a system based on the PSD chip would be ideal for a novel scintillator project, using hundreds of $LaBr_3$ detectors. This DTRA project, mentioned below, is funding future work on this PSD project.

III. Future of the Project

Los Alamos National Laboratories (LANL) has recently agreed to support continuation of the work originally funded by this NSF Grant. The support for work conducted at SIUE will come is the form of a sub-award from the Nuclear Reactions Research Group (headed by Dr. Lee Sobotka) located at Washington University (WU) in Saint Louis. The objectives of our work with LANL are as follows.

1. To bring up the present PSD chip and support hardware at LANL.
2. To test the present PSD chip and support hardware with $LaBr_3$.
3. Transfer the DAQ to the new XLM-XXV (rather the separate SIS and XLM-80 units.) The XLM units are products of JTex.
4. To implement on chip or on CB ADC's
5. If the full DTRA project moves forward, to implement a 16-ch channel chip.

Items 1, 2 and 3 will be completed in the summer of 09. Item 4 is discussed below and item 5 is a long-term objective, and not included in our present agreement with LANL.

The existing PSD8C while fully functional only supports analog output data streams. Researchers as LANL desire a system with a digital interface. It is much easier to transmit digital data over long distances in the presence of significant environmental noise.

The team will design a digital interface for the existing PSD8C chip which will be implemented on an FPGA. Eventually the FPGA will be placed on the PSD8C chip board and will service a pair of PSD8C chips. An external ADC will also need to be integrated onto the chip board.

The digital logic will be described using Verilog® HDL and will include:

- control logic which will interact with the configuration registers on the pair of PSD8C chips as well as with the readout electronics on the pair of chips;

- control logic that will sample the analog output data streams from the two chips and store the results in a memory located on the FPGA; and

We will develop prototype designs using a third-party Xilinx development system. The design will then be handed off to WU where the designs will be integrated into the actual PSD8C chipboards. We will design a small board consisting of two PSD8C chips and a small amount of support circuitry which can be plugged into the Xilinx development system.

Initially, we had proposed that the ADC, RAM buffer, and I^2C serial interface should all be integrated onto the PSD8C chip. In fact, this possibility was discussed in some depth in our previous interim report. After further reflection and study, this effort seems to be unnecessary. The advantages hoped for can be achieved with the FPGA–based design described above and without the need to integrate the ADC and associated circuits on the chip itself.

However, since the design of the RAM buffer is complete and the design of the ADC is nearly complete, it seems reasonable to complete the design. Integrating these components onto the chip would definitely save area and power but is much more risky and cannot be done as quickly as the FPGA-based design. While at this time, it is unlikely, that we would integrate these components onto the next revision of the PSD8C chip, we would like to keep this option available, perhaps for a later

revision of the chip. This work will be performed by a graduate student. The student is expected to complete the work and graduate by December 2009.