Design of On-chip ADC for Custom ASICS Used in the Detection of Ionizing Radiation

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ABSTRACT

DESIGN OF ON-CHIP ADC FOR CUSTOM ASICS
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by

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This thesis presents the design and simulation of a 12-bit, 2 MSample/sec Analog-to-Digital Converter (ADC). The ADC is intended for use in a family of integrated circuits (ICs) used in the detection of ionizing radiation. The ICs are being developed by the Integrated Circuit Design Research Laboratory at Southern Illinois University Edwardsville (SIUE). The current chip designs provide analog outputs. Storing data in a digital format on-chip before transmittal to a host computer over an "I2C-like" interface will result in improved system performance.

The ADC will be implemented in the future in a 5-Volt AMIS 0.5 μm, double-poly, tri-metal CMOS process (C5N). The converter described in this thesis employs a two-step flash technique with digital error correction. It is configured as a fully-differential circuit. The converter performs a 7-bit "coarse" flash conversion followed by 6-bit "fine" flash conversion, the results of which are then combined through a digital correction algorithm to produce the desired 12-bit output.

Electrical simulations demonstrate that the noise characteristics of the converter are consistent with those of a 12-bit quantizer. Simulations indicate that, in the presence of typical offset and mismatch errors, the effective number of bits (ENOB) will be 11.8. This work was initiated by the heavy-ion nuclear chemistry and physics group at Washington University in Saint Louis and is funded by NSF Grant #06118996.

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CHAPTER 1

INTRODUCTION

Background

The IC Design Research Laboratory at Southern Illinois University Edwardsville (SIUE) is part of an interuniversity collaboration which has as its long-term goal the development of a family of multi-channel custom integrated circuits (ICs) suitable for use in a wide variety of low- and intermediate-energy nuclear physics experiments where the detection of ionizing radiation is needed. The greater collaboration includes researchers at Washington University in Saint Louis, Michigan State University, Western Michigan University, and Indiana University.

Often in nuclear physics experiments the type of radiation must be classified, the energy of the incident must be determined, and the position of interaction within the detector itself must be estimated [Sob:07]. The ICs which have already been designed and fabricated, as well as those currently under development contain the analog electronics that make the accomplishment of these scientific objectives possible. Moreover, someday these micro-chips may be used by the Department of Homeland Security (DHS) in nuclear threat detection systems deployed throughout the country.

The reasons why the collaboration became interested in developing a family of micro-chips for use in nuclear physics experiments include: (1) the need for high density signal processing in low- and intermediate-energy nuclear physics community is widespread,(2) no commercial chip was identified that was capable of doing what the researchers wanted, and (3) the scientists deemed it necessary for the “experimenter” to be in the “designer’s seat”.

Preliminary work on the ICs began in the year 2000 [Gan:00] [Mal:01]. Initially the development was funded through support from the nuclear reactions group in the Department of Chemistry at Washington University in Saint Louis; however, because of the success of the project over the years, the current work is funded by the National Science Foundation (NSF Grant #06118996).

While the initial intent was to use the ICs in nuclear physics experiments, we are now proposing to create a mini-center that will work on different aspects of nuclear threat detection systems for DHS. One aspect of our most recent proposal to NSF concerns the development of a suite of analog ASICs (Application Specific Integrated Circuits) for use with scintillation (Sc) and semiconductor solid-state (SS) detectors. Standard signal processing components would be developed in addition to novel elements including single, few, and "round-robin" charge integrators, chip-level filtering, and on-chip digitization (the topic of this thesis).

The goal of our group is to achieve a great simplification in digital-signal processing (DSP) by doing as much as possible in the front-end CMOS (Complementary Metal-Oxide Semiconductor) ASIC. Compact low-power CMOS digitizers are relatively slow. A full-blown DSP-based approach would require a digitizer with 14-bit resolution and a sample rate in excess of 100 MSamples/sec. Our group plans to overcome this limitation by using one of two analog schemes (one each for Sc and SS detectors) to reduce the time dependence of the signal to a few analog voltages that can be stored and subsequently digitized on-chip. We refer to the economical (low power, size, and money) strategy as Analog-Assisted Digital Signal Processing (AA-DSP).

It is the on-chip digitization of these analog output signals (from the various ICs under development) which is the topic of this Master's Thesis. In the following section, we briefly discuss in more detail the integrated circuits that we *have*

developed, *are* developing, and *will* develop over the next few years. In the subsequent section, we will enumerate the advantages of digitizing the analog signals on-chip as opposed to bringing the analog signals off-chip for digitization.

Integrated Circuits for Use in Nuclear Physics

A significant focus of the proposed mini-center will be on the design of low-noise, high-performance analog integrated circuits for use with detectors for ionizing radiation. This work will build on our past and ongoing efforts. The principal example of the former is our HINP16C chip [Eng:07a, Sad:02]. An example of the latter is our current project to develop a Pulse-Shape Discrimination (PSD) chip [Eng:07b, Hal:07, Pro:07]. The PSD project will be extended in the future to a full Analog-Assisted DSP scheme (AA-DSP) with information compaction, as well as the digitization, done on the front-end chip. The former is necessary as the digitizers will be relatively slow (a few Msamples/sec). As we shall see in this thesis even the design of a 12-bit, 2 MSample/sec ADC in a 0.5 micron CMOS technology is quite challenging.

Our collaboration has successfully developed and implemented the HINP16C chip, now in wide use in basic nuclear science. In addition to our own group, groups at the National Superconducting Cyclotron laboratory (NSCL), Oak ridge National Laboratory (ORNL), Indiana University, and Western Michigan University use this chip. Nuclear Physics (NP) groups at Florida State and Louisiana State are building entire programs around this chip as well.

This CMOS ASIC, based on prior work by Spieler and Britton [Spi:05, Sim:95], is described in detail in [Eng:07a, Sad:02] and its integration into a large-scale system is presented in [Wal:07]. A sampling of the science (from our group) using this chip, can be found in [Cha:07b,Cha:07c]. A motherboard which is

capable of housing 16 chipboards (CBs) is shown in Figure 1.1. A representative CB supporting two HINP16C chips is present in the foreground. A single motherboard is capable of supporting 512 independent channels.

Figure 1.1: HINP16C based system

Each of the sixteen channels of HINP16C contains a charge sensitive amplifier (CSA) with two gain ranges, shaper, constant-fraction discriminator (CFD), peak detector, time-to-voltage converter (TVC), and analog output sequencing logic. On the other hand, this chip has **no** pulse-shape analysis capability and ***relies on an external ADC*** (Analog-to-Digital Converter) for digitization. A block diagram for a single channel of the HINP16C chip is illustrated in Figure 1.2.

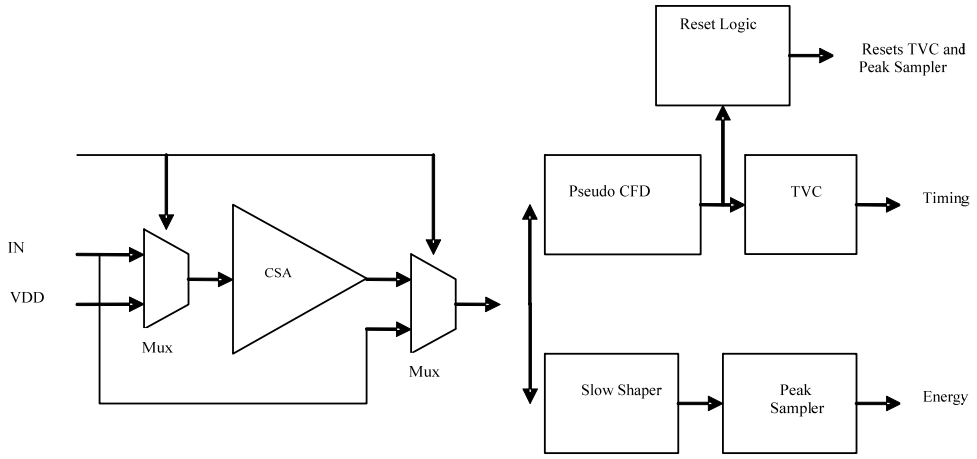

Figure 1.2: Block diagram of HINP16C chip

The "Timing" and "Energy" outputs in Figure 1.2 are analog pulse trains which are currently digitized by an off-chip ADC. The ADC described in this thesis *could* be integrated into a future generation HINP16C chip. An ADC integrated with HINP16C is desirable for many reasons as we will discuss in the following section of this thesis.

Signal-shape analysis capability (not possible with the HINP16C chip) is desirable in order to distinguish γ-rays, n's, α-particles from cosmic or other background events from scintillator-based systems. The shape analysis is also needed for tracking applications in large volume Ge or any size CZT detector arrays. A now nearly completed NSF-funded project (chip has been fabricated but as yet to be tested and fully characterized) moved us into the PSD (Pulse Shape Discrimination) realm for scintillators. An eight-channel chip we call PSD8C, fully described in [Hal:07] and [Pro:07], utilizes CMOS technology to provide: a) integration of several regions of the analog signal, b) time-to-amplitude conversion, and c) generates pulse streams from each of the above for an *off-chip* ADC.

To focus our attention, we consider a PSD capable scintillator (e.g., CsI(Tl), $LaCl_3$:Ce [Hoe:05], stilbene, or BC501) and the analog electronics [Pro:07] illustrated in Figure 1.3.

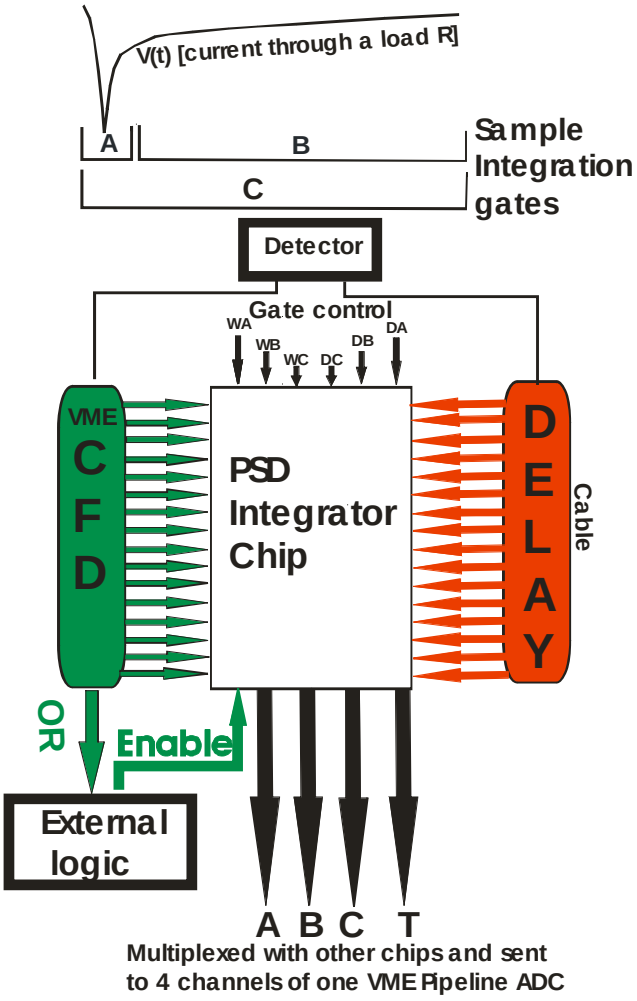

Figure 1.3: Overview of analog pulse-shape discrimination integration scheme

The photomultiplier tube generated current pulses are split to be used in logic and linear branches. Representative pulses [Hal:07] are depicted in Figure 1.4.

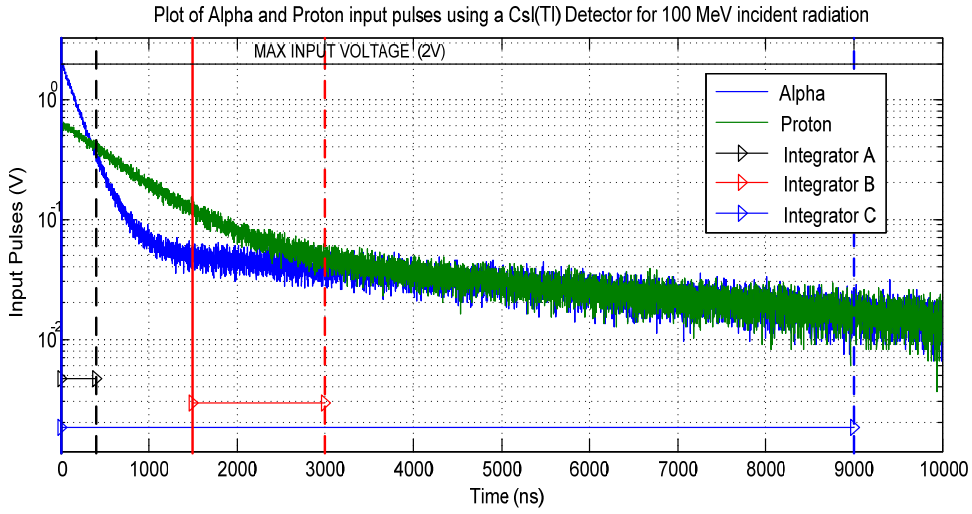

Figure 1.4: Sample current pulses from CsI(Tl) (alpha-blue and proton-green).

Timing signals are generated by compact, low-power constant-fraction discriminators recently developed by our collaboration. The individual logical timing signals and delayed linear signals are sent to the CMOS chip for multiple time region integration. The individual CFD logic signals ANDed with a global enable signal provide channel enables for three different integrations (**A, B** & **C**). These integrations are performed with start times referenced to the individual discriminators. In addition, the amplitude, **T,** produced is proportional to the difference in time between the individual discriminator firing and an external common stop reference. The delays in the integrators' starting times (D_A, D_B, D_C) and the widths (W_A, W_B, W_C) of the integration windows are externally controlled by the user [Pro:07].

Figure 1.5 shows the simulated response to different pulse shapes for two different detector types. The plots on the left show standard "PSD" plots with average signals, while the plot on the right show the angle distributions from

simulations, with additive noise. Cleary, one is able to easily identify particle type using the PSD technique.

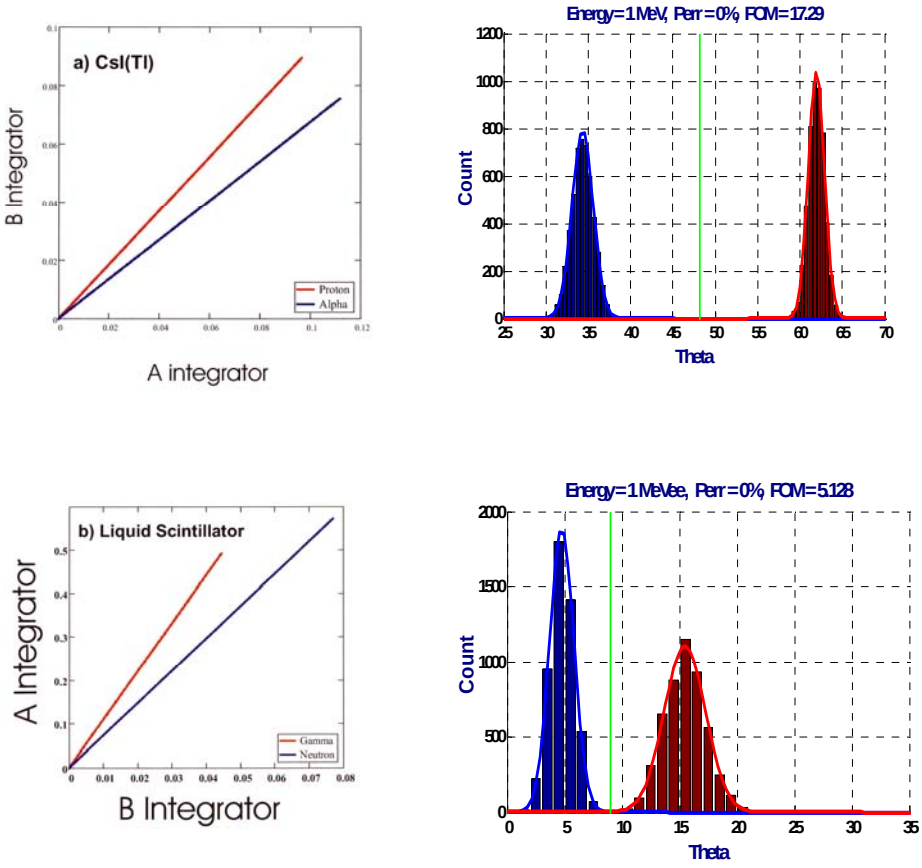

Figure 1.5: PSD plots demonstrating particle identification

The PSD8C chip's planned use, in basic NP experiments, is for: CsI(Tl) (charged particle ID), CsI(Na) (γ-ray spectroscopy with pile-up rejection and possible n/γ discrimination), and for BC-501A (n/γ discrimination). In all cases, the detector arrays have over 100 elements and the cost of conventional electronics is prohibitive.

While in basic science experiments, there is no problem with coupling the PSD8C chip with conventional power-hungry (VME) ADCs, the same cannot be said of DHS applications. Our group imagines an array of scintillators (e.g. CsI(Na), but perhaps ultimately a LaHalide detector) attached to the new generation of compact photomultiplier tubes (PMTs). The PSD8C chip just described, with a single ADC of the type described in this thesis integrated into the chip, along with a new generation of compact low-power CFD's would provide a compact, low-power and easily portable system suitable for homeland security applications

The PSD8C project is the first of two. The second project is to extend the CMOS–ASIC capability into the realm of extracting ***full*** pulse-shapes [Eng:07b]. While it is true that traditional DSP accomplishes this, traditional DSP is not transportable to a high-density, front-end CMOS ASIC. This is due to its need for fast (> 100 MSample/sec) many-bit digitizers (> 12 bits) in conventional DSP.

In principle, a signal waveform encodes (via a small set of signal parameters) what is truly important to the NP community. These are the answers to the: "what" (particle type), "where" (x,y,z) and "when" (t) questions. Using traditional DSP, the waveform is collected, digitized and stored over a long period of time. This is a *digitization intensive* operation that puts *extreme* demands on the downstream computation. Our group's proposed approach [Eng:07b] is to provide analog compaction on the front-end ASICs, analog storage of this information on the front-end ASIC, **and then "slow" digitization with an on-chip ADC**. In short, the ultimate "front-end" objective of this proposal is to push the analog CMOS possibilities as far as they can go in order to aid and simplify DSP operations.

We call our design to accomplish this goal "Analog-Assisted DSP" (AA-DSP) and its logic is shown in Figure 1.6. The proposed AA-DSP chip could be used to extract position information from a large segmented Ge or from pixilated CZT

detector array. This logic is an extension and improvement on that reported by Pullia et al. [Pul:00]. In order to characterize the waveforms, two sampling "round-robin" loops (per channel) are envisioned: a) A fast sampling loop used to extract parameters associated with the rise time of the primary CSA signal and total waveform of the induced signals; and b) a much slower sampling loop used to obtain multiple samples in the tail region of the primary CSA signal [Hal:07].

The timing logic (CFD + TVC) and the two banks of round-robin "integrate and hold" circuits (*fast* and *slow*) are fed by one of several CSA options. The adjectives *fast* and *slow* refer to the duration of time that each integrator is gated on. For our initial simulations, the (individual) period of integration is 62.5 ns in the *fast* bank and 500 ns in the *slow* bank. Simulations performed to date suggest that the proposed technique will be effective in capturing the desired waveforms.

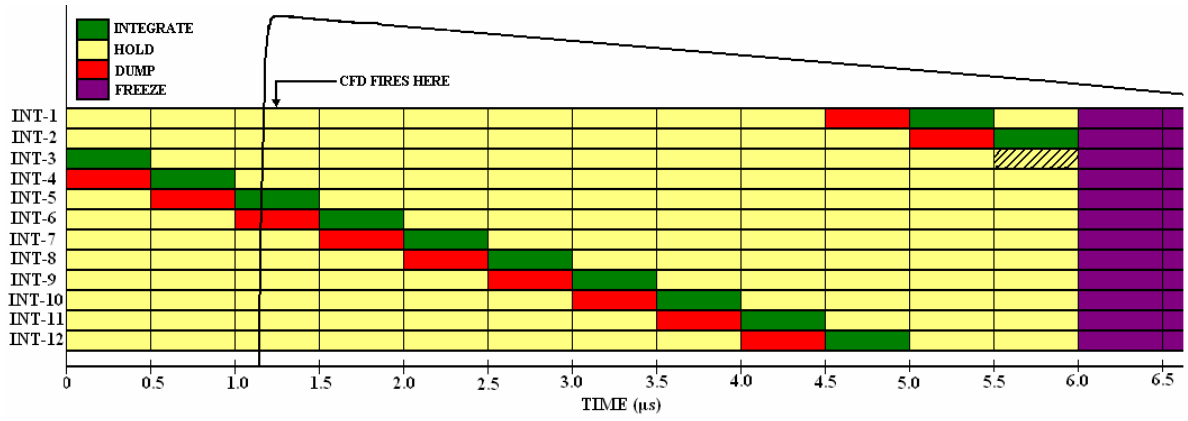

Figure 1.6: AA-DSP logic

Need for On-Chip ADC

Cleary, all three multi-channel ICs (HINP16C, PSD8C, and AA-DSP) discussed in the previous section could be enhanced by the addition of an on-chip ADC. The transmission of sensitive high-speed analog pulse trains to an off-chip VME ADC is a very difficult task. Low-level analog signals are easily corrupted. Moreover, even if the system is correctly designed, it is the nuclear physicists who set up and conduct the experiments. It is easy to degrade the performance of an analog system through improper grounding or shielding. The transmission of high-speed digital signals even over long distances is, on the other hand, relatively easy. Digital signals have high noise immunity.

Furthermore, VME ADCs are relatively expensive, large, and power-hungry. As described in an earlier section, it is important that systems proposed for use in nuclear threat detection systems to be used by DHS be compact and low-power. These attributes can only be achieved if an on-chip ADC is employed. Since the ICs described in the previous section are all fairy large (15 mm^2 – 50 mm^2), the proposed ADC and companion RAM, used to store the digitized results, will increase the overall chip area (and chip costs) by only 10 – 30%.

In the case of HINP16C since there are 16 channels and two analog pulse streams (“Energy” and “Time”), a 2 MSample/sec converter could complete the digitization in a maximum of 16 μs. In addition to the ADC, a small 32 location, 18-bit wide memory (16 amplitude and 16 time values) is needed to store the results [Val:08]. Generally, only a small subset of the channels actually are impacted by radiation at any given time and need to be read out so the digitization would take even less time, typically just a few microseconds. Just like the currently used VME ADCs, the resolution of the on-chip converter need not exceed 12 bits.

For the PSD8C chip where there are 8 channels. Each channel consists of 3 sub-channels and a time-to-voltage converter (TVC). The digitization could once again be completed in a maximum of 16 μs. As with HINP16C, only a small 32 location memory is needed to store the digitized values. Even for the AA-DSP chip with 8 channels the digitization could be completed in a maximum of 125 μs (could be done in less time if multiple ADCs are used). Even in this case only a 256 location memory is required to store the data.

To minimize the system-level interconnect, we propose to transmit the contents of the RAM storing the ADC results back to a host computer via a serial "I2C-like" interface. This greatly simplifies the system level design and in particular the design of mother board and associated chip boards.

The on-chip ADC described in this thesis will be integrated for the first time in a second generation PSD8C chip. The IC is expected to be fabricated and ready for field testing by December 2009. The on-chip ADC presented in this thesis will then be used in the AA-DSP chip described in the previous section. While there are no immediate plans to integrate an on-chip ADC with HINP16C, this may well happen at some point in the future if funds for the integration were made available.

Object and Scope of Thesis

The object of this thesis is to describe the design of an on-chip Analog-to-Digital Converter (ADC) suitable for integration with a series of custom ASICs developed or currently under development by our IC design research laboratory. The ASICs are intended for use in the detection of ionizing radiation in instruments intended for experiments in low- and intermediate-energy nuclear physics and (perhaps someday) in real-time homeland security nuclear threat detection

systems. The central features of the converter design include 12-bit resolution with a sampling rate of 2 MSamples/sec.

There are five chapters in this thesis. Brief descriptions of the ASICs which might benefit from the integration of an on-chip ADC were presented in this chapter along with a rationale for integrating the ADC into these custom chips in the future. In Chapter 2 we will compare several ADC architectures and provide justification for why a two-step flash technique was selected for integration. Moreover, a detailed description of the architecture and algorithm employed by the proposed two-step flash converter is provided. Chapter 3 discusses the design and performance of the many sub-components utilized in the ADC design. In Chapter 4 we present simulation results. The ADC was simulated at the behavioral level using MathCAD® and also at the electrical level using Cadence's Spectre® program. The MathCAD simulations were used to compare the results from the electrical simulations as part of the debugging process. Moreover, the effect of non-ideal behavior associated with the various sub-components was investigated using the simulator implemented in MathCAD®. Finally, Chapter 5 will give conclusions and discuss the future direction of this research work.

CHAPTER 2

ADC ARCHITECTURE

Comparison of ADC Architectures

Analog-to-Digital Converter (ADC) architectures can be classified into two main categories based on the sampling rate of the input analog signal: 1) Nyquist-rate analog-to-digital converters b) Over-sampling analog-to-digital converters. If f_B is the highest frequency of interest of the analog input signal and f_S the frequency at which the analog input signal is sampled, then according to the Nyquist sampling theorem the sampling frequency f_S must be at least twice the maximum input frequency, $f_{B,}$ in order to recover the signal from its samples. ADCs that operate with an input signal frequency close to the half the sampling frequency are called Nyquist-rate ADCs. This type of converter frequently require a very sharp cutoff for the preamplifier or anti-aliasing filter making it difficult and complex to implement [All:03].

ADCs that have input signal frequency much less than half the sampling frequency are called over-sampling ADCs. The anti-aliasing filter requirements of over-sampling ADCs are more relaxed than those of Nyquist-rate converters. The reason for this is that the sampling frequency is much higher than the Nyquist rate. The transition band that extends from the edge of the signal band to the edge of the smallest frequency band at which signals alias into the signal band is quite wide and the transition is smooth. A comparison of the frequency spectrum of a Nyquist-rate ADC and an over-sampling ADC is as shown in Figure 2.1 [All:03].

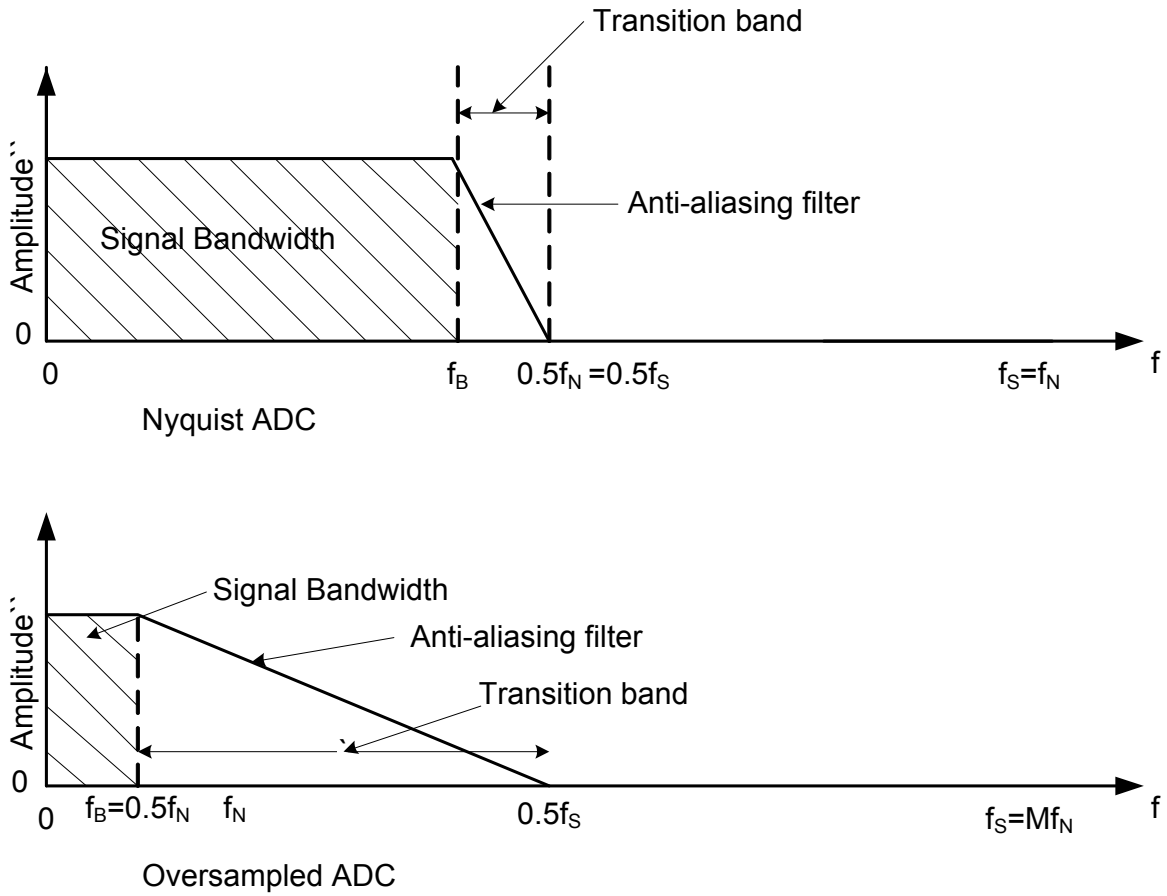

Figure 2.1: Frequency spectrum of Nyquist-rate ADC and over-sampling ADC

Conversion rate	Nyquist-rate ADCs	Over-sampled ADCs
Slow (10-100 Samples/sec)	Serial (ramp, dual-ramp). High resolution possible. (< 14 bits possible)	Very high resolution possible (< 24 bits possible)
Medium (1-100 KSamples/sec)	Successive approximation Algorithmic (< 16 bits possible)	Moderate resolution (< 18 bits possible)
Fast (1 – 100 MS/sec)	Flash Multiple-bit pipeline Folding and interpolating (< 14 bits possible)	Low resolution (< 6 bits possible)

Table 2.1: Classification of ADC architectures

Within the two major classes of converters, there are many sub-classifications. Table 2.1[All:03] presents the classification of various types of ADCs along with their resolution and conversion rates. Based on the earlier description it is easy to understand that the fastest converters are those of the Nyquist class. When high sample rates and resolution are needed, Nyquist-rate converters still rule! In "slow" and "medium" speed applications, the over-sampling converters dominate. In over-sampling converters, "resolution in time" is traded in for "resolution in amplitude". Over-sampling converters are very popular because they require relatively low-performance analog sub-systems where both matching and offsets requirements are easily met.

Among the fastest of the converters are those generally referred to as "flash" or "parallel" ADCs. In "flash" converters, the input voltage is compared against 2^N (where N is the number of bits of resolution desired) voltages linearly spaced across the full-scale range of the converter. The comparator output generate a "thermometer" encoded output which is in turn converted to a binary encoded output. Note for a N-bit conversion, 2^N analog comparators are required.

While flash converters are capable of very high sampling rates, the associated hardware is very large when high resolution (> 8 bits) is required. In this research we selected a "folding" ADC [All:03]. In a folding ADC the full-scale range is subdivided into P sub-ranges. Each of the P subranges is mapped into a single subrange. A "coarse" converter determines in which of the P subranges the input signal lies. The input signal is then mapped into the aforementioned single subrange. A "fine" quantizer then acts on this range to determine the appropriate fine bits. When this process occurs over two clock cycles, the resulting ADC is called a "two-step" ADC. In the next section, we discuss two-step flash converters.

Two-Step Flash Converter

Two-step (sometime referred to as "two-stage" or "half-flash") flash architectures are an effective means of realizing high-speed, high-resolution analog-to-digital converters because they can be implemented without the need for operational amplifiers having either high gain, large gain-bandwidth product, or a large output swing. Moreover, with conversion rates approaching half those achievable by fully parallel designs, half-flash architectures provide both a relatively small input capacitance and lower power dissipation than their full-flash relatives [Raz:92].

As discussed in Chapter 1, an ADC suitable for integration on the various ICs under development should be capable of 12-bit resolution and a sampling rate of a few MSamples per second. The design described in this thesis is based on an earlier design by Wooley and Razavi [Raz:92]. In the sections that follow we will describe our design and the manner in which in differs from the Wooley converter. The designs are very similar at the architectural. Significant differences exist in how the circuits are clocked an in the implementation details at the circuit level.

The main advantage of using a two-step flash converter over a fully parallel converter in the proposed application is the reduction in the number of comparators used. For example, a fully parallel 12-bit ADC would require 2^{12} (4096) comparators where a two-step flash ADC (7-bit first stage and 6 bit second stage) requires on 128 comparators in the first stage and 64 comparators in the second stage (a total of just 192 analog comparators). Thus, use of a two-step flash ADC results in substantial reduction in the number of comparators. The proposed two-step flash ADC has a 7-bit first stage that produces a "coarse" estimate of the input analog voltage. The 6-bit second stage then uses this "coarse" estimate to

produce a “fine” estimate of the input analog voltage. Digital correction logic is then used to combine the two estimated in order to produce the desired 12-bit result.

One bit of redundancy or overlap is used in the proposed architecture to enable the second stage to correct for out-of-range errors in the first-stage (resulting from mismatch errors), thereby relaxing the precision required of the first-stage comparators. The use of a fully-differential (differential input AND differential output) architecture increases the input dynamic range, eliminates even-order harmonic distortion, and suppresses common-mode noise due to supply transients and noise coupling via the substrate [Raz:92]

The ADC is designed with an input range of -1.2 Volts to 1.2 Volts relative to the analog signal ground, which we call AGND. The AGND voltage in our design is 2.4 Volts. Therefore, the effective input range of the ADC is from 1.2 Volts to 3.6 Volts. This range is exactly what is needed for both the amplitude and time pulse trains currently produced by the ICs discussed in Chapter 1 of this thesis. The ADC is designed such that it produces a 12-bit zero output for an effective input analog voltage of 1.2 Volts (approximate bandgap voltage) and a 12-bit all ones output for an effective input analog voltage of 3.6 Volts (3 X bandgap voltage). The digital output word could easily be converted to a twos-complement representation if it proves more convenient.

Two-Step Algorithm

The two-step algorithm that is used in the ADC architecture is as shown in Figure 2.2. We will describe the algorithm [Raz:92] in detail in this section of the thesis.

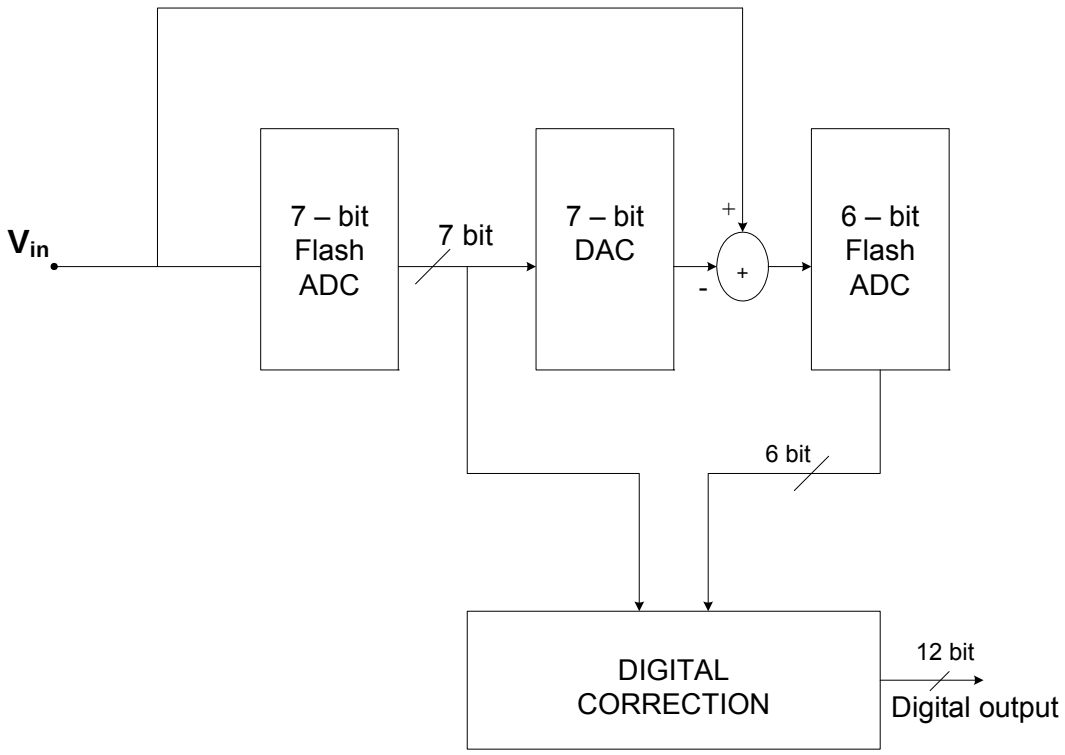

Figure 2.2: ADC converter architecture

As illustrated in Figure 2.2, the input analog voltage, V_{in}, is applied to the first stage of the ADC. The first stage produces a "coarse" digital output for the applied input analog voltage. The 7-bit coarse digital output is then passed to a 7-bit switched-capacitor (SC) Digital-to-analog converter (DAC) which produces an analog estimate of the "coarse" value. This analog estimate of the "coarse" code is then subtracted from the input analog voltage by the subtractor (which we refer to as the "residue generator" in the remainder of this thesis) in order to produce the "residue". The "residue" voltage is then passed, as an analog input, to the second stage of the converter. The second stage is a 6-bit flash ADC that produces a "fine" digital output for the applied "residue" voltage.

The 7-bit coarse digital output is passed through a delay register (not shown in the figure) and then to the digital correction logic circuit where it is combined with the 6-bit fine digital output of the second stage to produce the 12-bit final digital output. Details on how the two digital values are combined to form a single 12-bit digital word will be presented in a later section of this thesis.

First Stage

A block diagram of the first-stage electronics is shown in Figure 2.3.

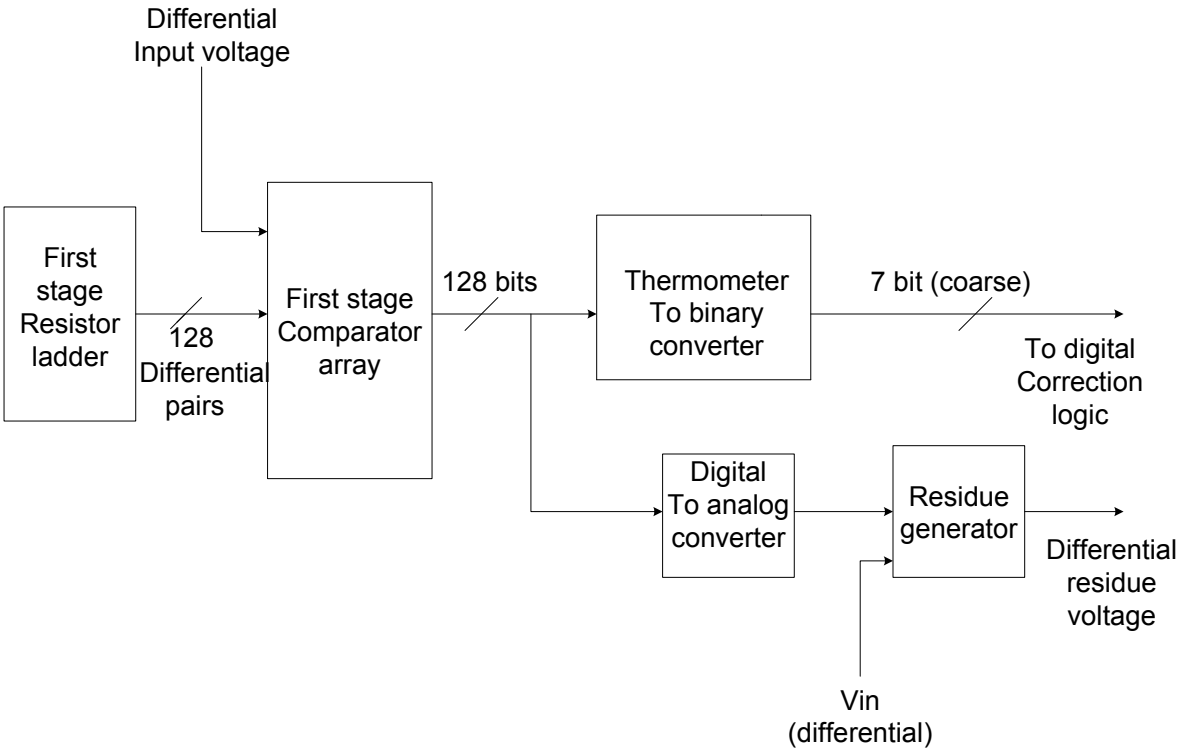

Figure 2.3: Block diagram of first-stage electronics

The first stage of the ADC is composed of a resistive ladder, an array of 128 comparators, a SC DAC, a residue generator and a thermometer- to-binary converter. In order to differentiate the first-stage components from the components of the second stage a prefix 'first stage' is added to the comparators

and the resistor ladder. The first-stage resistor ladder consists of 2^7 (128) identical resistors. One end of the first-stage ladder is connected to V_{Ref_plus} (3.6 Volts) terminal and the other to V_{ref_minus} (1.2 Volts). The first-stage ladder divides the full-scale range (2.4 Volts) into 128 equal steps (stepsize is 18.75 mV). The tap voltages from the first-stage resistor ladder are used as one of the inputs to the first-stage comparators with the other input to each of the first-stage comparator coming from the analog input voltage, $V_{in.}$

A first-stage comparator produces a 'one' if the applied tap voltage is greater than the analog input voltage, $V_{in,}$ else it produces a 'zero'. Thus the array of 128 first-stage comparators produces a 128-bit "thermometer" code. This 128-bit code is then sent to a thermometer-to-binary converter where it is encoded into the 7-bit (coarse) estimate. The 128-bit thermometer code also drives a switched-capacitor DAC, which produces an analog approximation of the thermometer code. The analog approximation produced by the DAC is subtracted from the analog input voltage, V_{in} to obtain the "residue". The first stage comparators, DAC, and residue generator are all implemented as fully differential circuits.

Second Stage

The block diagram of the second-stage electronics is shown in Figure 2.4. The second (or "fine") stage digitizes the differential output of the residue generator to encode the six least significant bits (fine) of the ADC. The second-stage consists of a resistive ladder with a ladder loading correction circuit, an array of 64 comparators, and a thermometer-to-binary converter.

The second-stage ladder consists of 128 identical resistors that are connected across four resistors of the first stage ladder near its mid-point. Recall that the first-stage ladder divides the full-scale range (2.4 V) into 128 equal

segments with each segment 32 LSBs (Least Significant Bits) wide or 18.75 mV. A LSB equals $\frac{2.4}{2^{12}}$ Volts or 586 μV. The second- stage has a full-scale (FS) range of 128 LSBs *i.e.* 75 mV. Therefore, the second-stage ladder is connected across four first-stage ladder resistor segments.

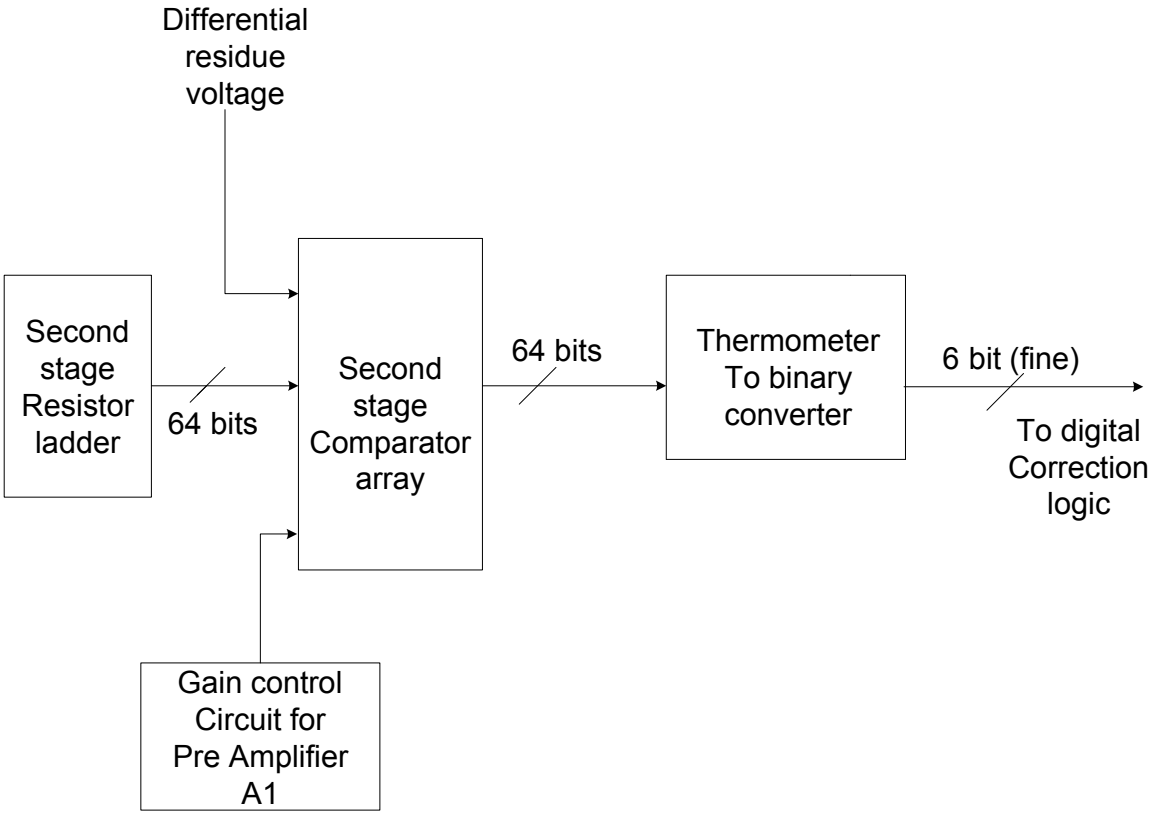

Figure 2.4: Block diagram of second-stage electronics

The loading introduced by the second-stage ladder upon the first-stage ladder introduces a systematic error. This error can be eliminated by cancelling the currents drawn from the first-stage ladder by the second-stage ladder. This is done by injecting currents equal to those drawn by the second stage ladder at the junction of the two ladders [Raz:92].

The tap voltages from the second-stage resistor ladder are applied as one of the inputs to the second stage comparators, the other input, applied to all of the second-stage comparators, is the residue voltage from the first stage. A preamplifier, A_1, with a gain of approximately 14 (considerably larger than the value of 3 used in the original Wooley [Raz:92] design) is used to amplify the differential 'residue' input which varies from 1 to 64 LSB (*i.e.* from 585 mV to 37.5 mV). This is necessary to prevent the signal integrity of the differential 'residue' input from being lost due to the offset voltage of second stage comparator or charge injection from the switches.

The gain control circuit produces a control voltage for the preamplifier, A_1, to ensure a gain which is insensitive to process corner. As will be explained in more detail later, the control voltage automatically adjusts the gain as process parameters vary. This novel pre-amplifier design developed as part of this research will be described in more detail in a later section of this thesis.

The second-stage comparators produces a 'one' if the applied tap voltage is greater than the residue voltage else it produces a 'zero'. Thus, the array of 64 second-stage comparators produces a 64-bit thermometer code. This code is then applied to a thermometer-to-binary converter where it is encoded into the 6-bit (fine) value which is then passed on to the digital correction logic.

System Timing

The system timing of the ADC is as shown in Figure 2.5 and is somewhat different from that employed by Wooly *et. al.* The operation of the individual components in the ADC is controlled by three non-overlapping mutually exclusive clocks $Ø_1$, $Ø_2$, $Ø_3$. Mutually exclusive implies that at any given time only one of the three clocks is high. The entire operation of the ADC is pipelined (unlike the orginal

design) and is completed in two clock periods. A clock period is defined as a single occurrence of all the three clock phases: $Ø_1$, $Ø_2$, $Ø_3$. The design of the three-phase clock generator is beyond the scope of this thesis. A VerilogA model of the generator was used in all electrical simulations of the ADC presented in Chapter 4.

Since the analog pulse trains associated with the various radiation detection ICs discussed in Chapter 1 will always be digitized as a block, the pipelined behavior has a negligible impact on overall system performance adding only one additional clock cycle to the time required to digitize the block of analog voltages. The use of pipelining; however, allows for longer settling times associated with the aforementioned analog sub-systems and also simplifies the timing constraints. Wooley's design depended upon small, reasonably well-controlled delays in order to ensure proper operation of many of the analog sub-systems. Here we only require that the clocks be non-overlapping. We will assume a master clock frequency of 5 MHz (200 nsec clock period) for convenience. This implies that the duration of each of the three phases is 67 nsec. This applies an output sample rate of 1.7 MSamples/sec. The operation of the ADC is explained below with the help of Figure 2.5. Note, a new input voltage to the ADC should be applied at the start of $Ø_2$.

During $Ø_1$, the first-stage resistor ladder tap voltages are sampled by the first-stage comparator circuits. Offset-cancellation in the first-stage comparators also takes place during $Ø_1$. The analog input voltage, V_{in}, is then sampled by the first-stage comparators during $Ø_2$. The first-stage comparators compare the first-stage ladder tap voltages with the sampled input voltage and produce either a 'one' or a 'zero' based on their inputs. The first-stage comparators make their "decision" during $Ø_3$. The outputs from the first-stage comparator are latched on the falling edge of $Ø_3$.

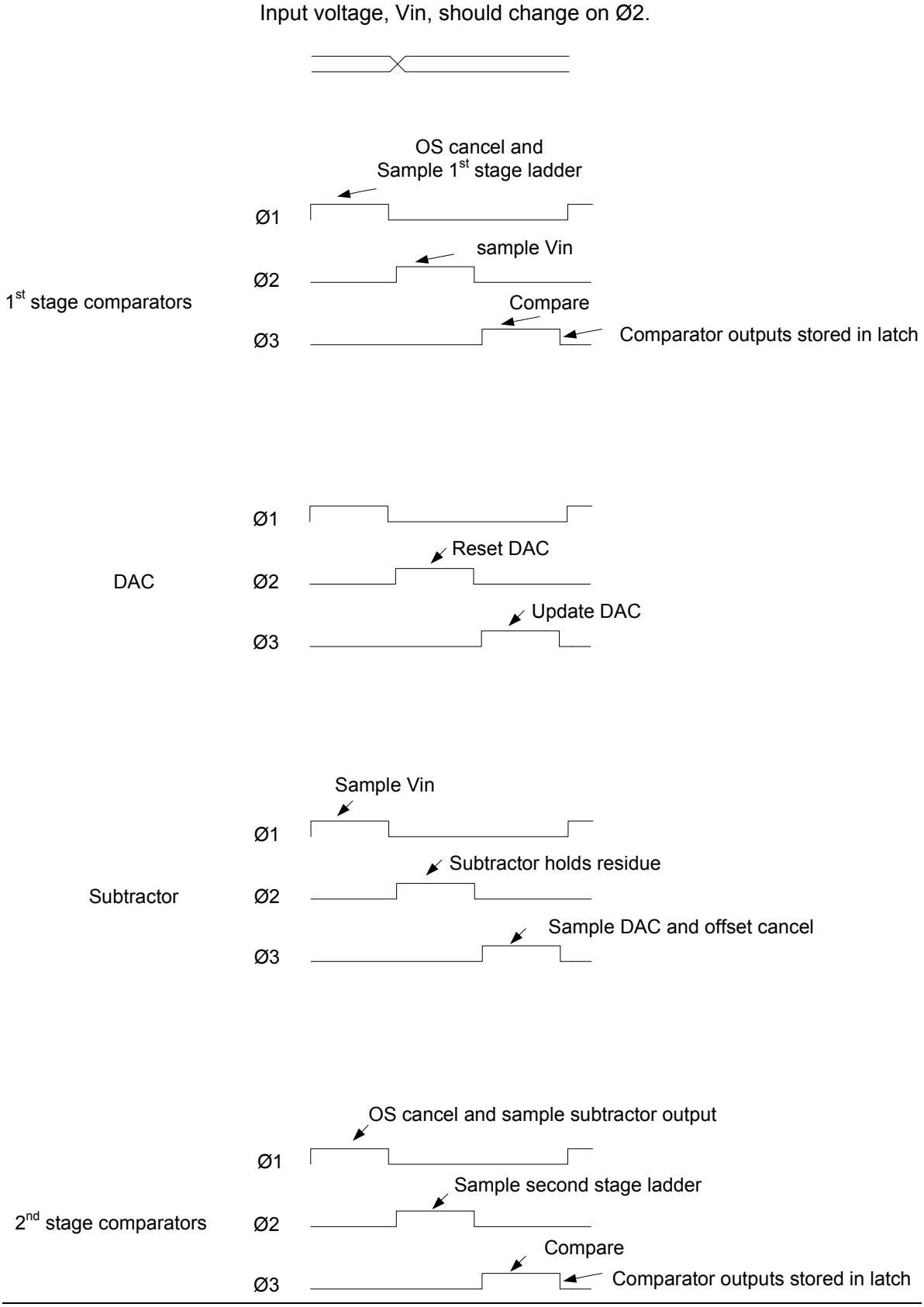

Figure 2.5: System timing diagram

The digital-to-analog converter (DAC) is reset during $Ø_2$ and its value is updated based on the first stage comparator's output during $Ø_3$. This implies that the time it takes for the first-stage comparators to resolve (not long because of the positive feedback that is employed) plus the time it takes for the DAC outputs to resolve must not exceed 67 nsec. The residue generator (subtractor circuit) samples the DAC output during $Ø_3$. Offset cancellation of the residue generator output also takes place during $Ø_3$. The residue generator samples the input voltage, $V_{in,}$ and subtracts the DAC output voltage from it producing the 'residue' during $Ø_1$ of the next clock period. The subtractor circuit has 67 nsec to settle. The subtractor holds this residue during $Ø_2$.

Offset-cancellation of the second-stage comparators takes place during $Ø_1$. The comparators also sample the residue generator output during $Ø_1$. The second-stage ladder tap voltages are sampled by the second-stage comparators during $Ø_2$. The second stage comparators produce either a 'one' or a 'zero' based on their inputs during $Ø_3$. Note: the second-stage comparator outputs are delayed from the first-stage comparator outputs (because of the pipelining) by one full clock period. The "fine" and "coarse" codes are aligned in the digital correction logic by delaying the "fine" code by one register delay.

Digital Encoding

Digital encoding performs the function of converting the thermometer code outputs of the comparators into a binary code. The design of the digital encoding and correction logic (at the circuit-level) is beyond the scope of this thesis. The logic-level design will now be described. VerilogA code was used to implement the digital encoding and correction logic in the electrical simulations presented in Chapter 4.

The digital encoding is used to obtain a 7-bit "coarse" output from the first stage and a 6-bit "fine" output from the second stage. These binary outputs are then corrected digitally to obtain the 12-bit ADC output. The encoding logic used in this ADC consists of a series of AND gates followed by an encoder. The digital encoding can be modified to correct out of order 'ones' and 'zeros' caused by large offsets in the comparators by sensing three adjacent levels in the thermometer code [Raz:92].

Redundancy and Digital Correction Algorithm

The first-stage comparators are designed for high-speed and modest resolution, while potential moderate errors are accommodated by using one bit of overlap between the two stages [Raz:92]. The overlap makes sure that the residue (difference between V_{in} and the DAC output voltage) of the first stage falls within the input range of the second stage. With ideal comparators and reference voltages, the first-stage output changes for input transitions that are integer multiples of 32 LSBs. The residue would then vary from 0 to a maximum of 32 LSBs, and the second stage would need a quantization range of 32 LSBs, that is a resolution of 5 bits.

Let us suppose that the j^{th} comparator in the first stage has an offset of '$deltaV_j$', then the code transition threshold corresponding to a V_{in} of (32LSB)*j is shifted by '$deltaV_j$'.

As shown in Figure 2.6 where the j^{th} and $(j+1)^{th}$ comparators have offsets $deltaV_j(<0)$ and $deltaV_{j+1}(>0)$, the residue varies from $deltaV_j$ to $(32LSB)+deltaV_{j+1}$.

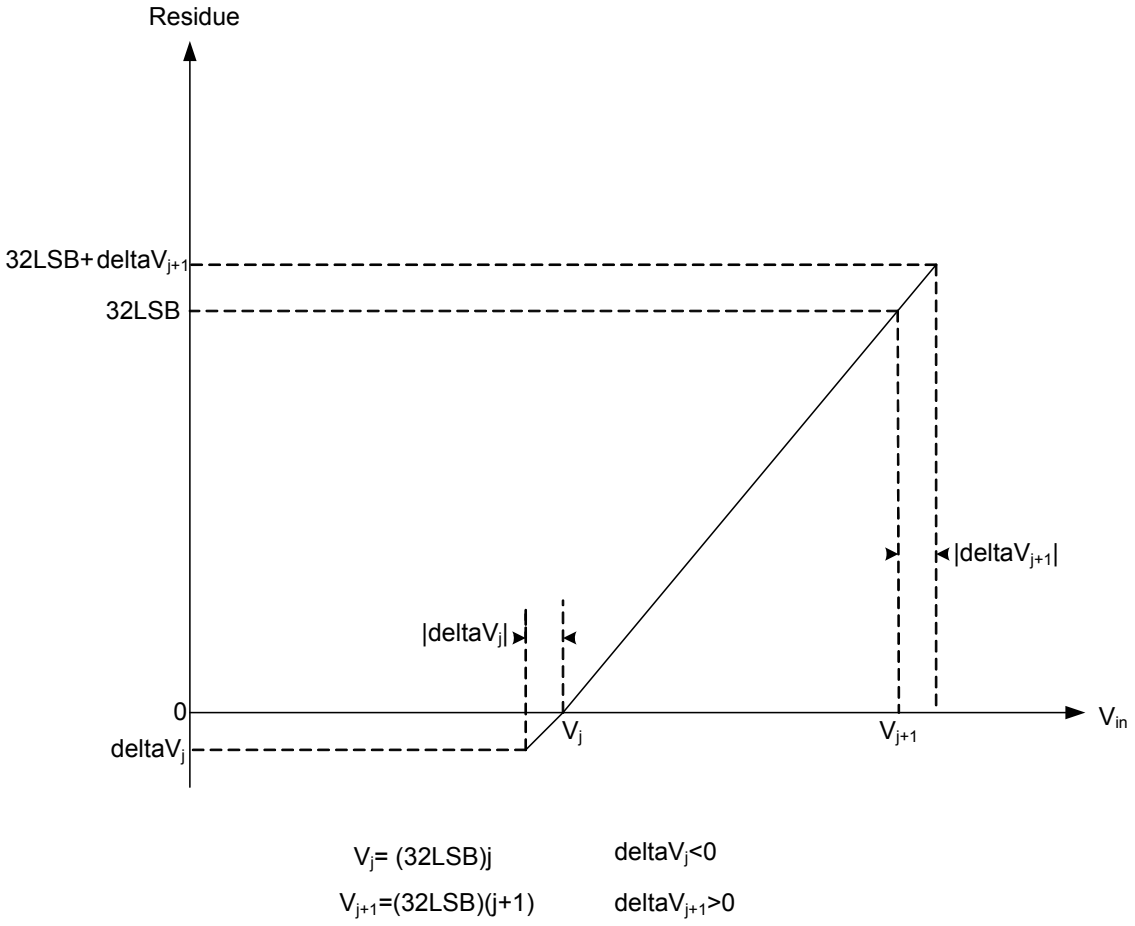

Figure 2.6: Residue versus input voltage

Therefore, an input range of 32 LSBs in the second stage is not sufficient to digitize the residue. The 12-bit ADC is assumed to have a first-stage comparator offset that never exceeds 16 LSBs (9.3 mV). As we shall demonstrate later, out first-stage comparators were designed to have input-referred offsets considerably smaller than this value (3σ offset of 1 - 2 mV). The second stage is designed for a resolution of 6 bits in order to digitize a residue as large as 64 LSBs. This value provides a buffer of +/- 16 LSBs as we shall now demonstrate.

As shown in Figure 2.7, the residue from the first stage is shifted up by 16 LSBs, so that as long as offsets from the j and (j+1) comparators in the first stage are less than 16 LSBs, the residue falls within the input range of the second stage *i.e.* 64 LSBs. In order to shift the residue up by 16 LSBs, the analog output of the DAC is shifted down by 16 LSBs.

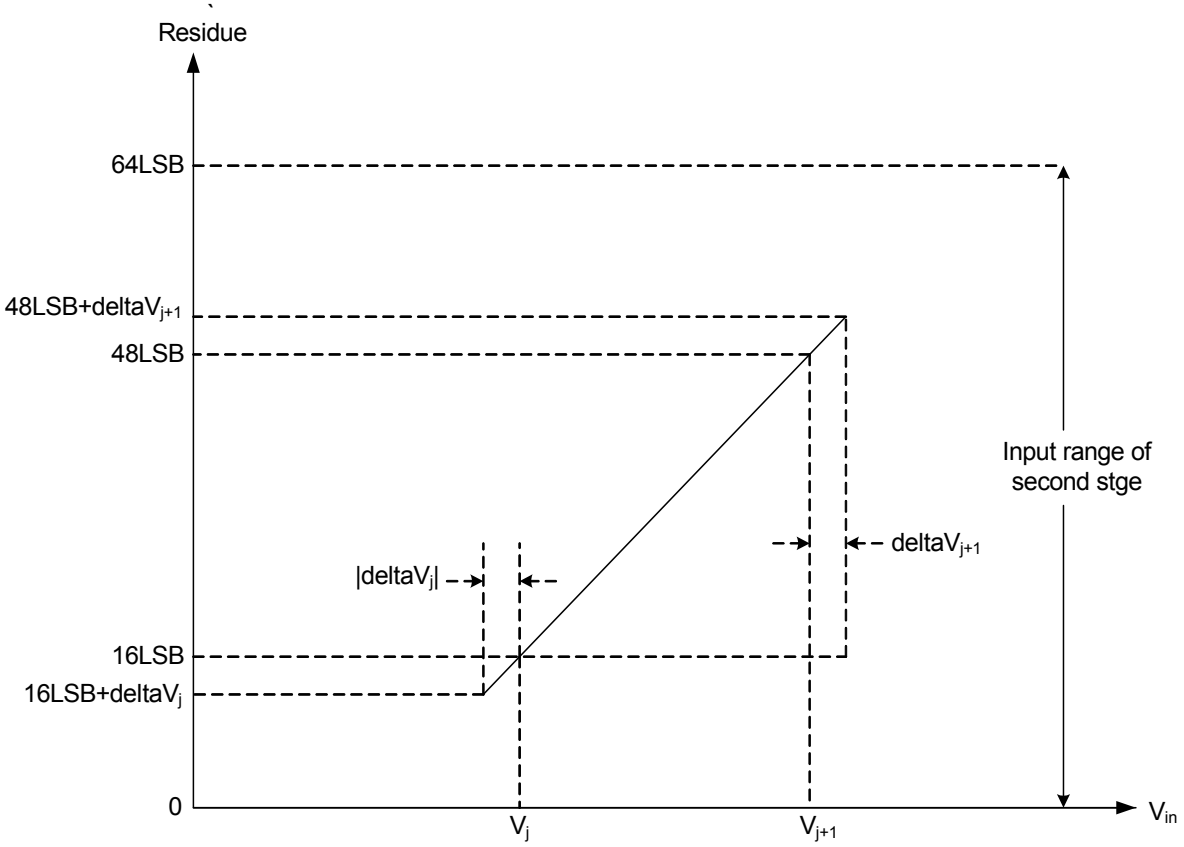

Figure 2.7: Range expansion in A/D converter

The digital outputs of the two stages of the ADC are added using the digital correction logic to obtain the final 12-bit output of the ADC. The digital correction algorithm is depicted in Figure 2.8

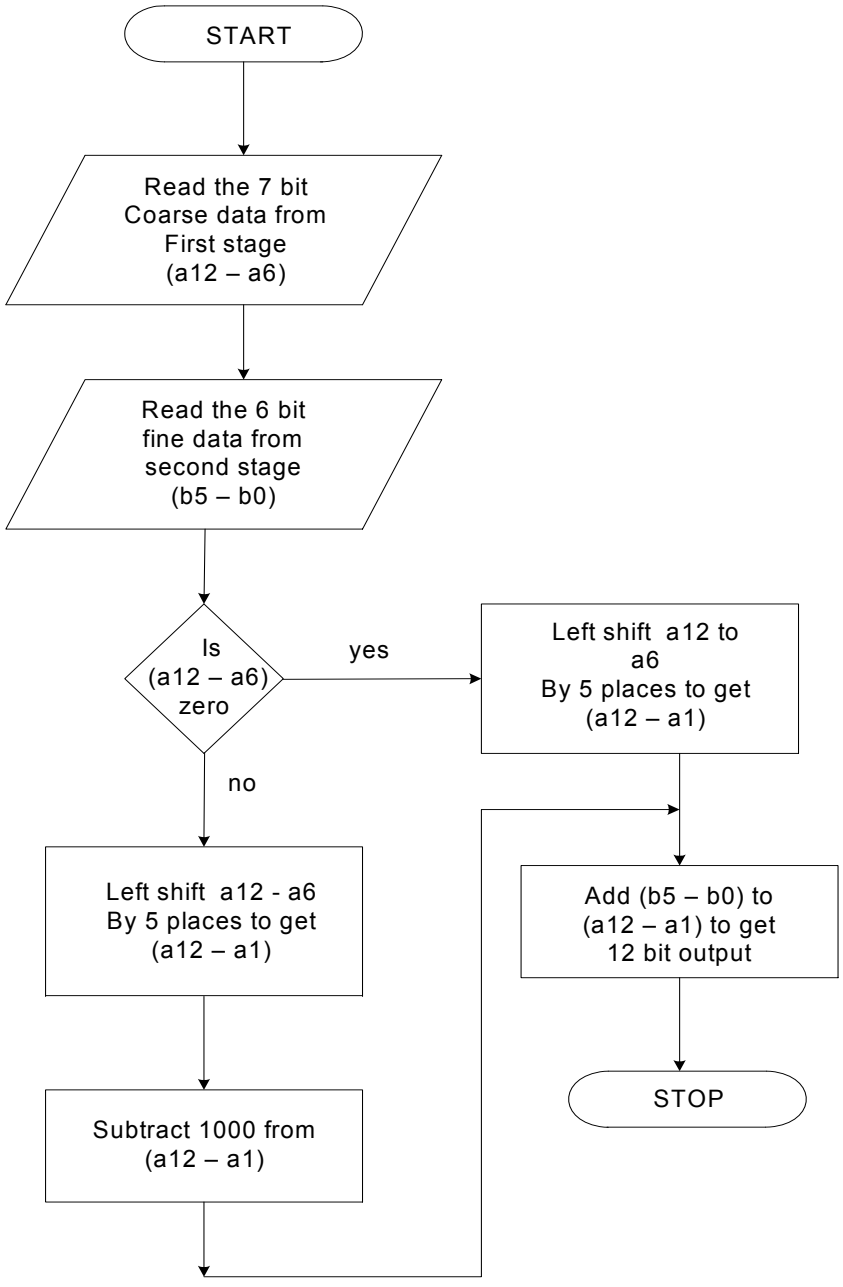

Figure 2.8: Digital correction algorithm flowchart

The algorithm first checks the 7-bit digital output from the first stage, if it is zero, the entire output of the first stage is shifted to the left by five places and the

6-bit second stage output of the ADC is added to the first-stage output to get the 12-bit final output. If the output of the first stage is not zero, we shift it to the left by five places and shift it down by 16 LSBs. This is done to emulate shifting the DAC output down by 16 LSBs. The 6-bit second stage output of the ADC is then added to the first stage output to get the 12-bit final output.

CHAPTER 3

DESIGN OF SUB-SYSTEMS

The ADC described thus far is comprised of two stages with each stage consisting of various analog sub-systems: analog comparators, resistor ladders, a digital-to-analog converter (DAC), and a switched-capacitor (SC) subtractor. The target technology is the AMIS 0.5 micron, NWELL process (C5N). The process supports three metal layers, double-poly capacitors, and a high resistance poly layer. The C5N process is a 5 Volt process.

The circuits described in this chapter were designed assuming the (nominal) process parameters shown below:

V_{TN} is threshold voltage of NFET = 0.75 Volts

V_{TP} is threshold voltage of PFET = -1 Volts

K_{PN} is transconductance parameter of NFET = 100 $\mu A/V^2$

K_{PP} is transconductance parameter of PFET = 32 $\mu A/V^2$

K_{aN} is 1/f noise parameter for NFET = 6.3×10^{-26} A F [Lee:02], [OCo:99]

K_{aN} is 1/f noise parameter for PFET = 3.8×10^{-30} A F

Single-Ended to Differential Converter

Single-ended signaling is a method of transmitting signals where one wire carries a voltage that represents the signal. Differential signaling is a method of transmitting signals by means of two complementary signals sent on two separate wires. The main disadvantage of single-ended signaling is that it lacks the ability to reject noise caused by differences in ground voltage level and any noise that may be picked up on the signal wire. This is because single ended method relies on the absolute value of the voltage carried by the wire to represent the signal whereas a

fully-differential method relies only on the absolute difference between the two complimentary voltages to represent the signal. Thus, any noise affecting both the wires is cancelled out when taking the difference.

Since the analog output pulse trains from the ICs discussed in Chapter 1 are single-ended but the ADC is fully-differential, a single-ended-to-differential conversion must be performed. The single-ended-to-differential converter as the name suggest converts a single-ended input voltage into a fully differential voltage with respect to an analog ground (in our case AGND, 2.4 Volts). The singled-ended-to-differential conversion circuit is comprised of two operational amplifiers. One operational amplifier is connected as a unity-gain follower while the second as an inverting gain amplifier with a gain of -1 as shown in Figure 3.1. The value for R is 30 kΩ and is implemented with the HY resistor layer (*doped* poly2 layer with a sheet resistance of 1 kΩ per square).

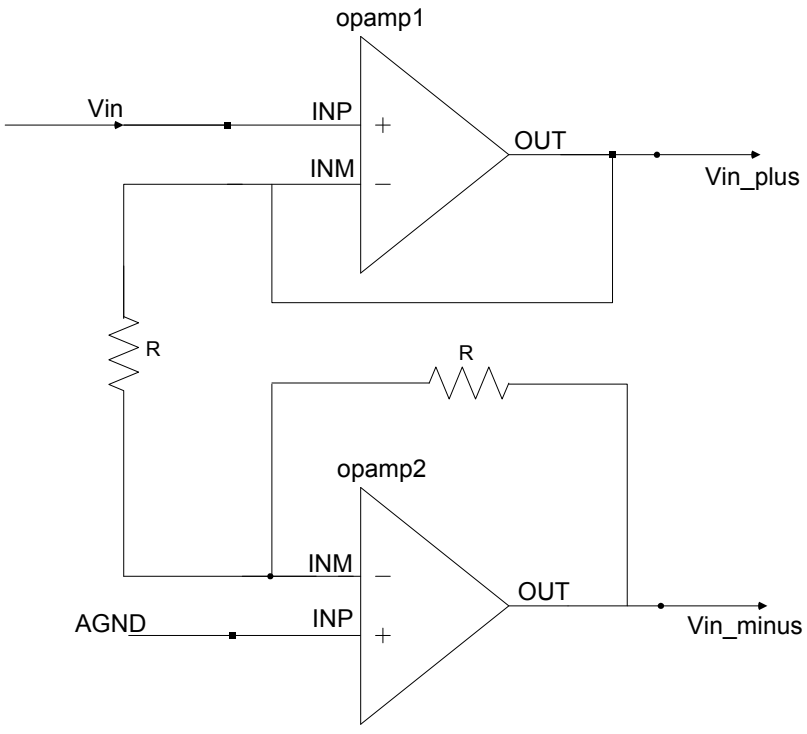

Figure 3.1: Single-ended-to-differential conversion circuit

The input V_{in} is applied to the top operational amplifier which is in a unity gain configuration to obtain V_{in_plus} and to the bottom operational amplifier which is in an inverting configuration in order to obtain V_{in_minus}. The output is fully-differential and centered about AGND. While the circuit was simulated and its performance was consistent with expectations, no effort was made to actually integrate the circuit into the ADC design at this time. Single-ended-to-differential conversion was performed using VerilogA for the electrical simulations described in Chapter 4. Several of the ADC sub-systems are yet to be designed and were modeled using VerilogA. The VerilogA code can be found in Appendix A.

Core operational amplifier

The core operational amplifier used in this circuit is a two-stage design [Hog:94]. The first stage is a folded cascade and the second stage is a class AB output stage. The class AB output stage is a complementary common-source amplifier where the NFET serves as the load for the PFET and vice versa.

The core operational amplifier meets the following specifications. The GBW is approximately 50 MHZ. It is capable of output currents of several milli-amps and possesses a near rail-to-rail output voltage swing. The slew rate of the amplifier is approximately 10 Volts/μsec. The core amplifier was not designed by the author; but rather, was designed for the PSD8C IC described in Chapter 1. A more detailed description can be found in [Pro:07].

Reference Generator

The reference generator provides the ADC with three reference voltages: (V_{ref_plus}, V_{ref_minus}, and AGND). As shown in Figure 3.2, the circuit employs three

operational amplifiers. The core amplifier is the same as the one used in the single-ended-to-differential converter circuit. All the resistors used in the circuit are of the HY type. All the resistors have a value of 30KΩ.

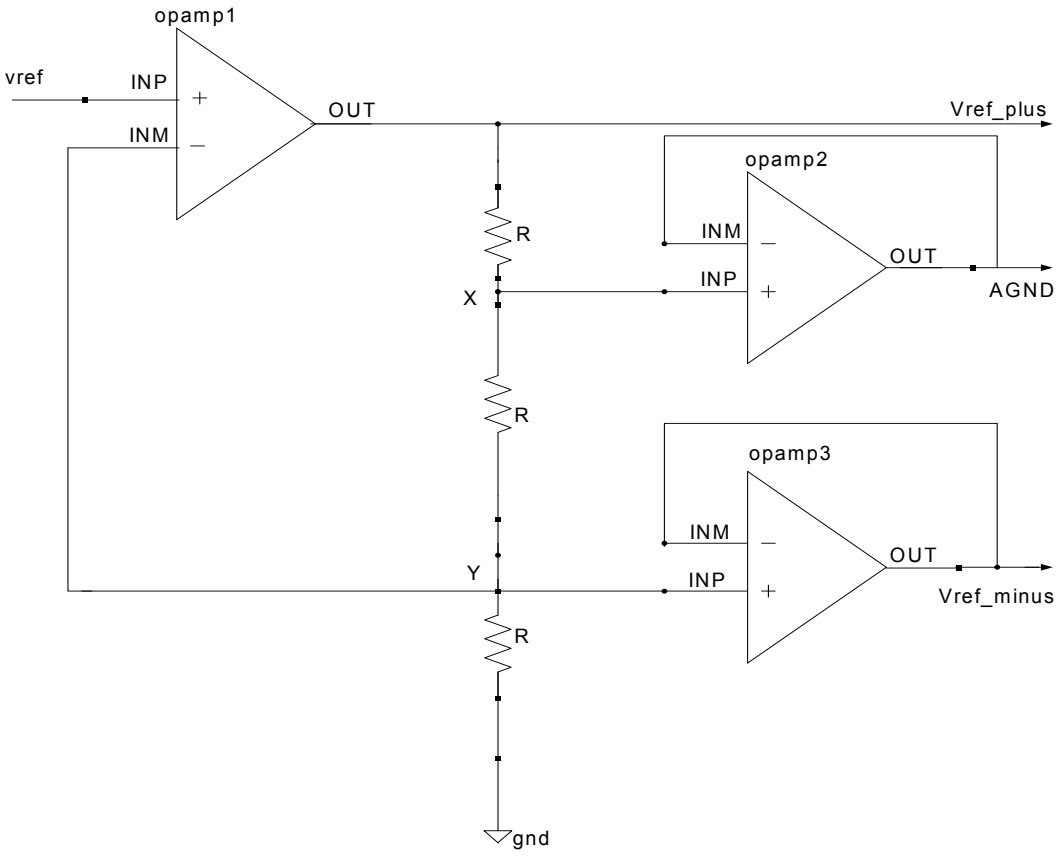

Figure 3.2: Reference generator circuit

The non inverting terminal of operational amplifier1 is fed with a bandgap voltage V_{REF} (approximately 1.2 Volts) that is obtained from the 'FULL_BIAS' circuit of the PSD-8C chip. For more details on the biasing circuits, the reader is referred to [Pro:07] and [Sad:02].

The operational amplifier (OpAmp 1) is in a non inverting configuration and its output voltage is given as $V_{ref\_plus} = V_{REF}(1+\frac{R_2}{R_1})$. Where $R_2 = 2R$. and $R_1 = R$, resulting in V_{ref_plus} of 3.6V. OpAmp 2 and OpAmp 3 are voltage followers, and they

buffer the voltages at points X and Y. Since all three resistors are equal, the drop across each resistor is the same resulting in the voltages at points X and Y being 2.4 Volts and 1.2 Volts respectively. Thus, AGND is 2.4 Volts, and V_{ref_minus} is 1.2 Volts.

While the circuit was simulated and its performance was consistent with expectations, no effort was made to actually integrate the reference generator circuit into the overall ADC design at this time. Single-ended-to-differential conversion was performed using a VerilogA model in the electrical simulations described in Chapter 4. A more detailed characterization of its performance is needed before the circuit will be integrated into the overall ADC design.

First Stage Ladder

The first-stage ladder circuit is used to divide the full-scale range (2.4 Volts) of the ADC into 128 differential voltages that vary in steps of 32 LSBs. As shown in Figure 3.3 each resistor in the ladder is constructed from "NY" poly. A "NY" resistor is made of a *undoped* poly II layer. The NY sheet resistance is nominally 50Ω/square. Based on [Raz:92], a value of 40 Ω was chosen. A length of 10 μm and a width of 12.5 μm is used for each NY resistor in the ladder. Based on information from the fabricator, we feel these values will yield acceptable matching characteristics (on the order of 0.5 %). The total resistance of the ladder is 5.12 kΩ. This means that the ladder dissipate 1.1 mW of power. Due to process variations, the ladder resistance is likely to vary by +/- 20 percent.

If the input capacitance for a first-stage comparator is on the order of 100 fF then for a tap near the center of the ladder the associated time constant, τ, is equal to 512 ps. Since ten time constants provide more than sufficient time for voltages

settle to the 12-bit level, the tap voltages applied to the comparators should become stable in less than 5 nsec (which is a small fraction of the 67 nsec associated with a single phase of the clock). Figure 3.3 illustrates the way in which the tap voltages are applied as differential pairs to the first stage comparators.

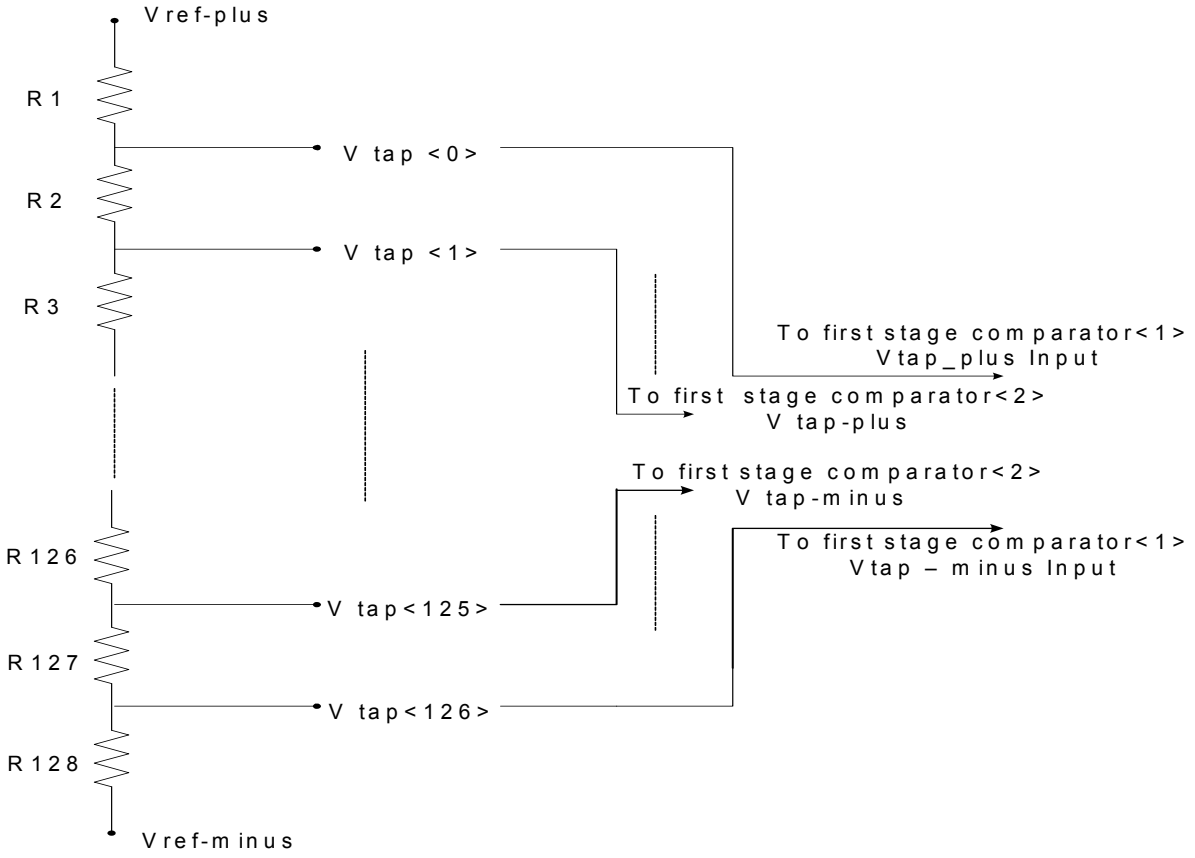

Figure 3.3: First-stage ladder circuit

First Stage Comparator

The performance of the first-stage comparator plays a crucial role in overall system performance. The input-offset of the first-stage comparator must be well within the error range covered by the redundancy and digital correction as was discussed in the previous chapter. With a one bit redundancy this range is approximately 9.4 mV for a differential input range of 2.4 Volts.

Figure 3.4 presents a block diagram of the first-stage comparator design. The block diagram of Figure 3.4 is provided to make it easier for the reader to understand how the overall comparator operates. The design consists of an offset-compensating preamplifier (gain of approximately 5) followed by a latch. In Wooley's [Raz:92] design, upon which ours is based, the pre-amplifier and latch operations were merged. While this reduces transistor count, it complicates the design to some extent.

The switches S_1-S_4 are used to sample the differential input voltage and the differential first-stage resistor ladder tap voltages. During $Ø_1$, the resistor ladder tap voltages are sampled. The preamplifier is forced into the offset cancellation mode when switches S_5 and S_6 are closed during $Ø_1$. The preamplifier is designed such that it idles at 1/3 rd of the supply voltage during offset cancellation mode. The offset cancellation is not perfect but reduces the offset by a factor of (gain+ 1) which is 6 in this design. During $Ø_2$ the differential input voltage is applied to capacitors C_0 and C_1.

The preamplifier amplifies the difference between the tap voltages applied in $Ø_1$ and differential input voltages applied during $Ø_2$ i.e. (V_{ref_plus}-V_{in_plus}) and (V_{ref_minus}-V_{in_minus}) and produces two outputs 'outp' and 'outm'. The outputs 'outp' and 'outm' are then applied to the latch in $Ø_3$ to get the final output of the first stage comparator. The latch is also designed to hold the comparator output during $Ø_1$.

Figure 3.5 shows the first stage comparator schematic. The first-stage schematic is designed to discriminate voltage differences as small as 2 mV and to settle within 25 nanoseconds. The sizes of all the transistors used in the above schematic are as shown in Table 3.1. Devices M_1-M_4 and M_{10} constitute the pre-amplifier. The bias current through device M_{10} is 50 μA. FETs M_5, M_6, M_8, and M_9

form the latch. Further work is needed to make sure the input-referred offset is sufficiently small but the offset is estimated at about 2 mV.

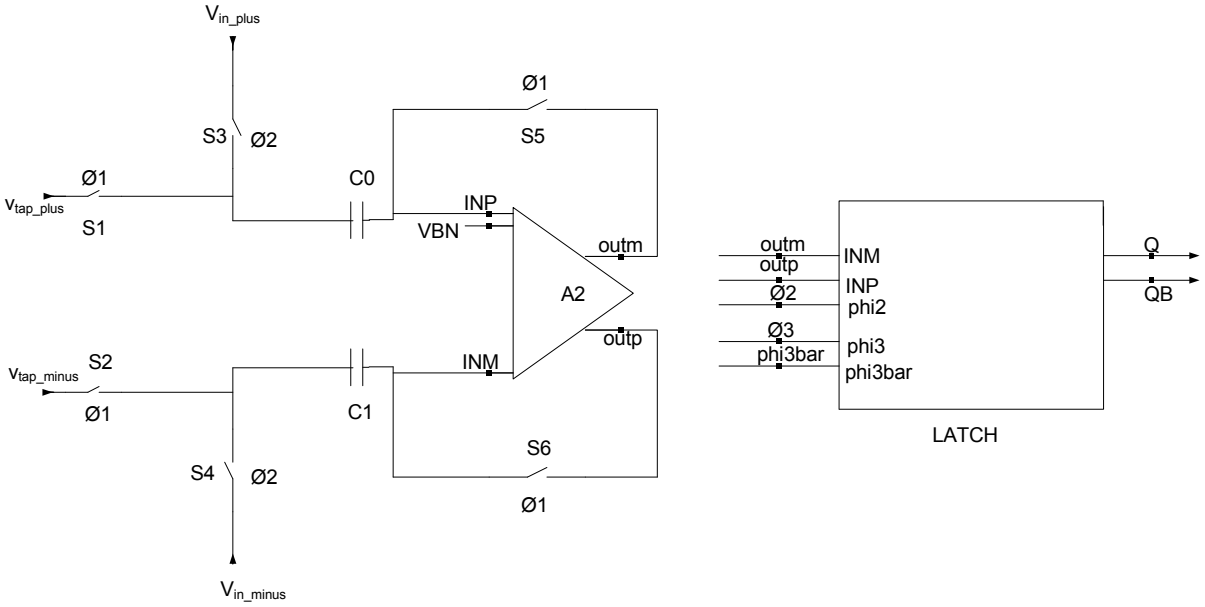

Figure 3.4: First-stage comparator block diagram

Transistor	Type	Width(μm)	Length(μm)	Multiplier
M1	n	1.6	0.6	1
M2	n	1.6	0.6	1
M3	p	1.7	2.9	1
M4	p	1.7	2.9	1
M5	p	1.9	2.8	1
M6	p	1.9	2.8	1
M8	n	1.9	9.6	1
M9	n	1.9	9.6	1
M10	n	6.4	2	1
M11	p	3.1	0.6	1
M12	p	3.1	0.6	1
M13	n	0.9	0.6	1
M14	n	0.9	0.6	1
M15	n	0.9	0.6	1
M16	n	0.9	0.6	1
M17	n	0.9	0.6	1
M18	n	0.9	0.6	1
M19	n	0.9	0.6	1

Table 3.1: Transistor sizes for first-stage comparator schematic

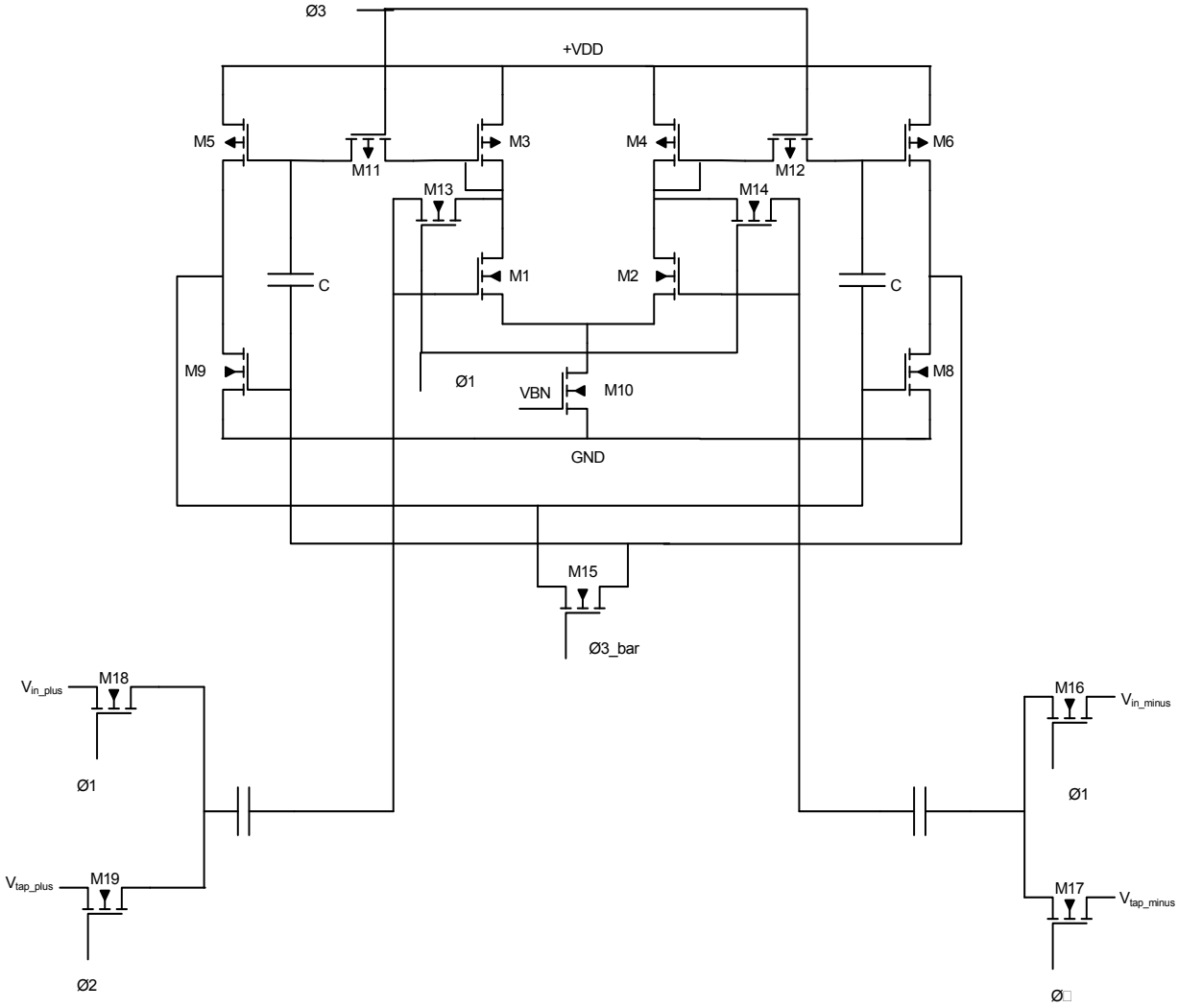

Figure 3.5: First-stage comparator schematic.

Digital-to-Analog Converter

The ADC's first-stage comparators produce a thermometer code output which leads us to use a "linear" or "segmented" capacitor array for the Digital to Analog Converter (DAC) that can be driven directly by the outputs of the first-stage comparators. The linear capacitor array DAC has many advantages; for example, it avoids the need to convert the thermometer code output of the first stage comparators into a binary code, thereby increasing the speed of the ADC. Using a

linear array capacitor DAC ensures a monotonic transfer characteristics of the DAC [Raz:92]. A linear array DAC is also easy to layout.

The DAC used in the ADC is fully-differential and is made of two arrays of DAC unit capacitors. The DAC_PLUS array consists of 128 DAC_PLUS unit capacitors (1 pF) and produces the DAC_PLUS output. Similarly, the DAC_MINUS array consists of 128 DAC_MINUS unit capacitors (C_U) and produces the DAC_MINUS output. In the array the top plate of the capacitors in all the unit cells are tied together. Both DAC_PLUS and DAC_MINUS arrays are driven by the first-stage comparator outputs. In order to shift the DAC output down by 1/2 LSB, as described in Chapter 2, the capacitor driven by the very first comparator in the array was made 0.5 pF or one-half the size of the unit capacitor used in the remainder of the array.

Figure 3.6 shows the DAC unit cell. The DAC is reset during $Ø_2$ and updated during $Ø_3$. The operation of both of the unit cells is identical except that they are switched to different reference voltages based on the first-stage comparator's complimentary outputs.

Let us consider the first DAC_PLUS unit cell in the DAC_PLUS array. If the Comp_plus output of the first comparator in the first stage is a 'one' then the bottom plate of the capacitor in the first unit cell is switched to V_{ref_plus} else it is switched to V_{ref_minus}. Similarly, if the output of the second comparator in the first stage is a 'one' then the bottom plate of the capacitor in the second unit cell is switched to V_{ref_plus} else it is switched to V_{ref_minus}. By switching some of the capacitors to the positive reference and others to the negative reference, a capacitor voltage divider is formed.

Thus if '$sumk_k$' capacitors out of the total 'C_{TOTAL}' are connected to V_{ref_plus} in the DAC_PLUS then its output voltage is given as :

$$\text{DAC\_plus}= \frac{[\text{Vref\_plus} - \text{Vref\_minus}] * \text{sumk}_k + [\text{Vref\_minus}] * C_{TOTAL} + V_{AGND} * (\frac{C_U}{2})}{C_{TOTAL} + (\frac{C_U}{2})}$$

The DAC_MINUS array also functions in a similar manner except that when Comp_plus output of the first comparator is a 'one' then the bottom plate of the capacitor in the first unit cell is switched to V_{ref_minus} else it is switched to V_{ref_plus} .

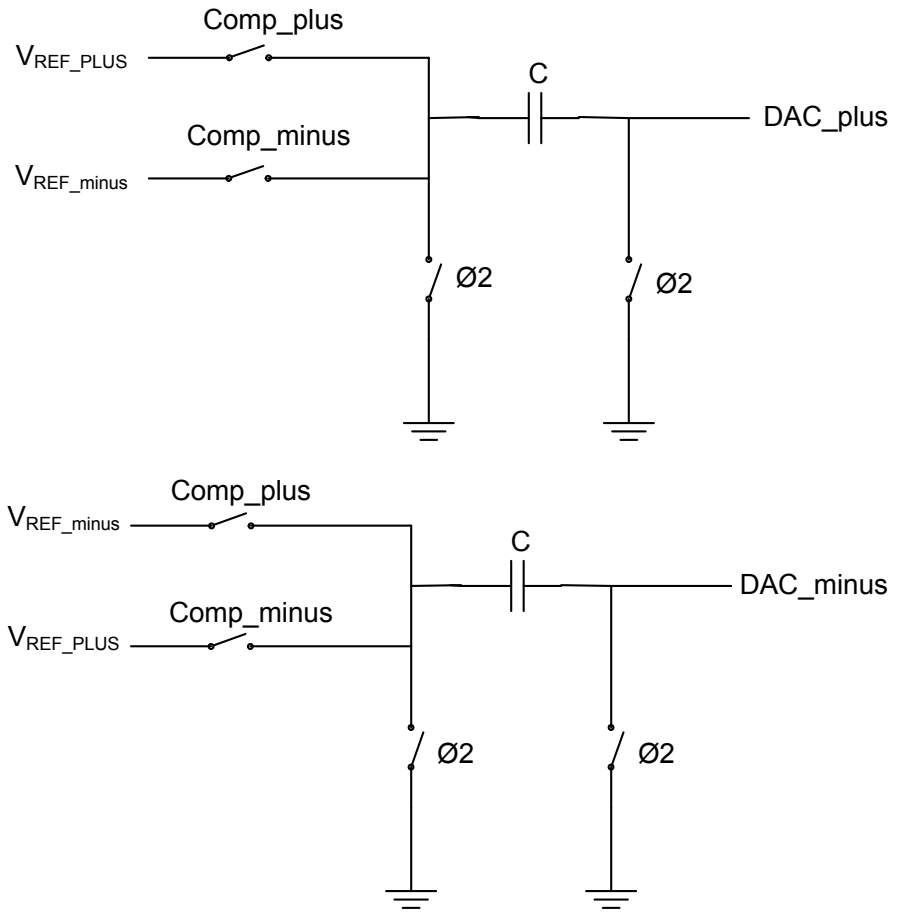

Figure 3.6: DAC unit cell

The switches that connect the bottom plate of the capacitor to the reference voltages are transmission gates (rather than a single FET). This is necessary to pass both high and low voltages easily. The FETs comprising the switches are

made wider in order to achieve a fast settling time in the DAC. However, the 'reset' switch used during $Ø_2$ is a single NFET with minimum area so as to decrease the effect of charge injection on the DAC and to minimize the parasitic capacitance on the DAC output nodes. The DAC output voltages are very sensitive to parasitic capacitance on the output node. Figure 3.7 illustrates the DAC_plus and DAC_minus outputs' ramp response.

The transfer characteristics of the DAC can be seen in Figure 3.8. As illustrated in the figure, the DAC_plus and DAC_minus settle to their final value within 20 nanoseconds. The plots presented below are characteristics of DAC when it was simulated using the typical process corner.

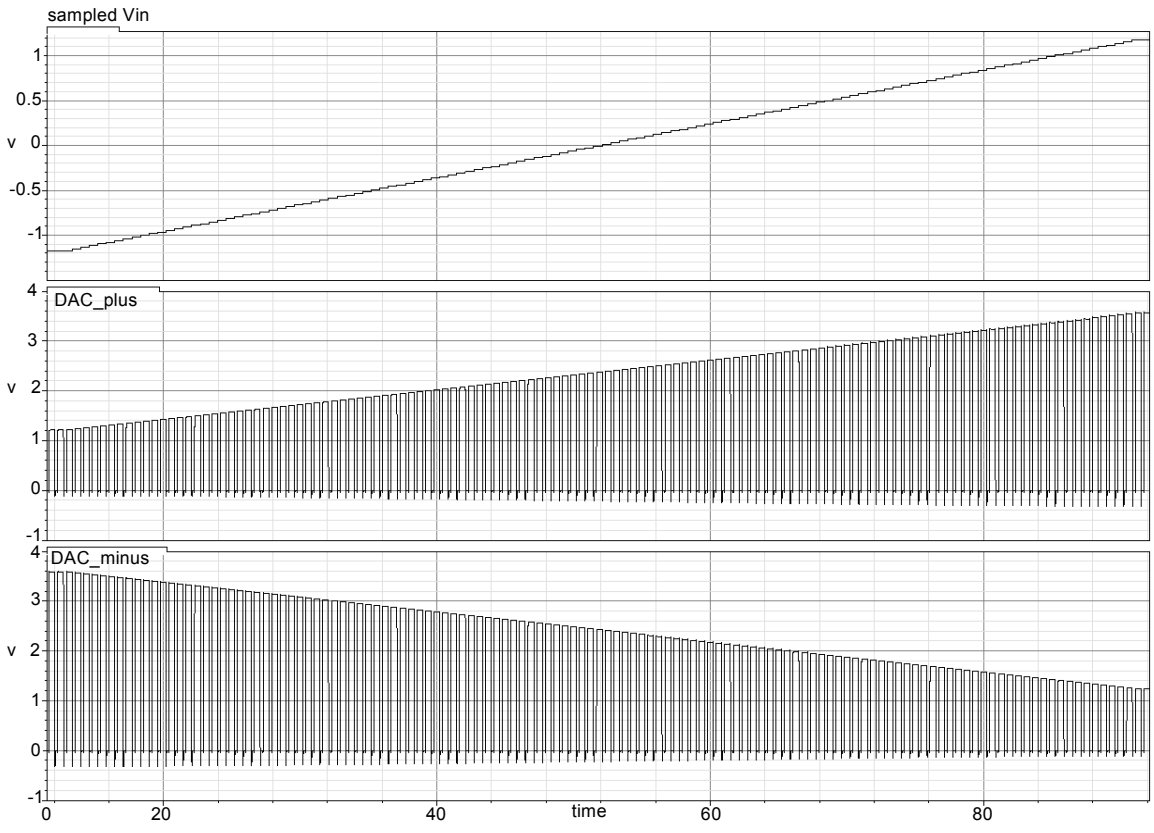

Figure 3.7: DAC_plus and DAC_minus outputs of a ramp input

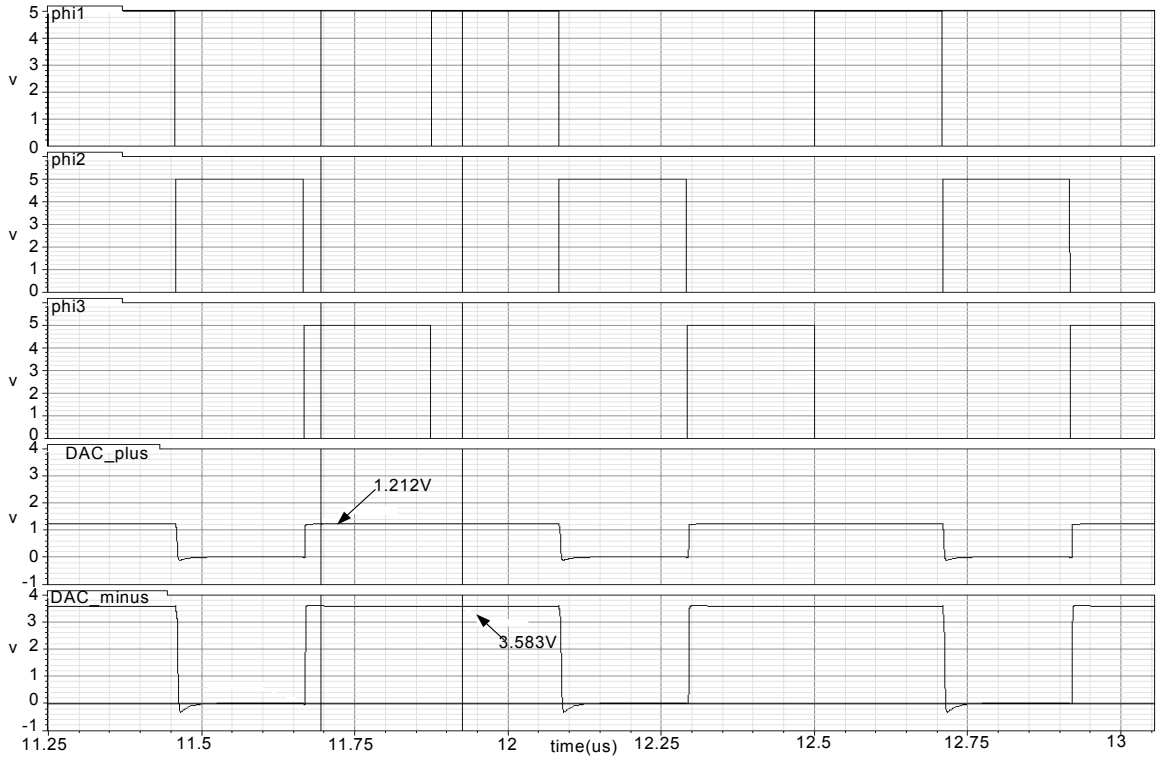

Figure 3.8: DAC transfer characteristic

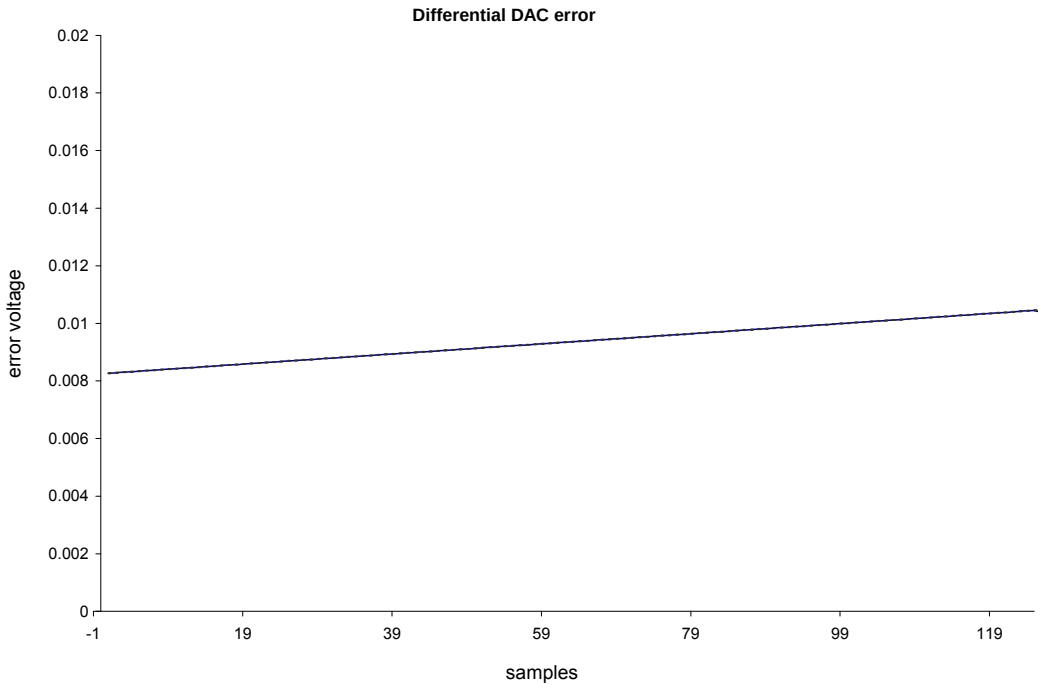

Figure 3.9: Differential DAC error plot

Figure 3.9 shows the differential DAC error simulated with the typical process corner model. The differential DAC error is the difference between the ideal DAC_plus output minus the obtained DAC_plus output and ideal DAC_minus output minus the obtained DAC_minus output.

Note that the DAC differential error is almost constant, with a maximum variation of +/-1mV due to non-ideal effects; for example, charge injection. It is larger than desired and efforts are still underway to reduce it. The use of larger unit capacitors (currently the unit capacitor is 1 pF) is being tried.

Residue Generator

The residue generator is used to obtain the difference between the analog input voltage V_{in} and the analog voltage generated by the DAC. This difference voltage is referred to as the 'residue'. Figure 3.10 depicts the residue generator circuit. The circuit includes offset-cancellation unlike the subtractor used in [Raz:92]. The capacitors in the figure are one-half the size of the unit capacitors in the DAC *i.e.* 0.5 pF. The residue generator is implemented in a fully differential manner; therefore, it produces Residue_plus and Residue_minus outputs which as stated are the difference between V_{in_plus} and DAC_plus and V_{in_minus} and DAC_minus respectively.

The transient response of the residue generator depends on the OTA (Operational Transconductance Amplifier) performance used in its implementation. The input voltages V_{in_plus} and V_{in_minus} are sampled in during $Ø_1$. The DAC_plus and DAC_minus voltages are sampled during $Ø_3$ of the previous clock period (recall the use of pipelining described in the previous chapter). The residue that is generated during $Ø_1$ is then held during $Ø_2$.

The OTA used in the residue generator is a folded cascade amplifier with switched-capacitor common-mode feedback. The capacitors in the common-mode feedback all have a value of 1 pF. The OTA schematic is illustrated in Figure 3.11. The bias current flowing in device M_{24} is 300 μA.

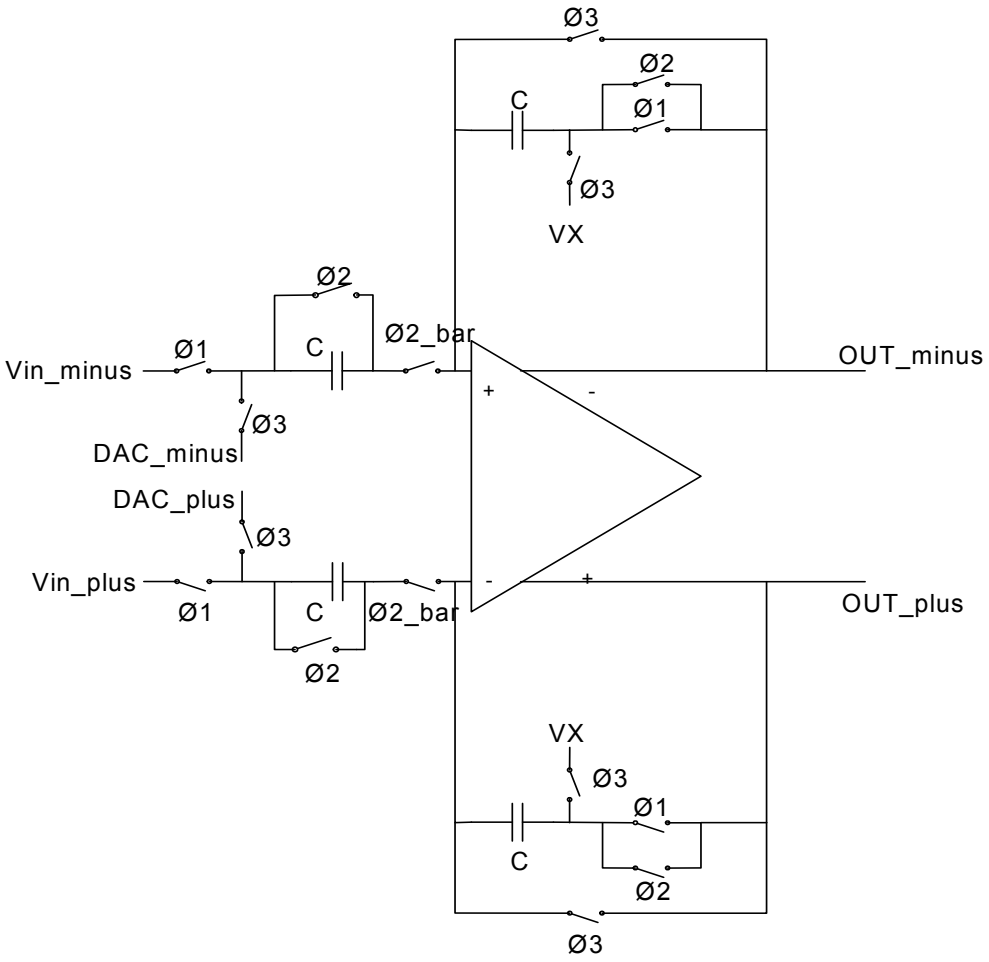

Figure 3.10: Residue generator circuit

The OTA described above meets the following specifications:

- Input common mode range of 2.25 V to 2.75 V
- Operate from a supply voltage of 4.75 V to 5.25 V
- Slewing time of 10 ns and a linear settling time of 90 ns

- Drive load capacitances between 1 pF and 5 pF
- Phase Margin of 60 degrees across all corners
- Low frequency open loop gain of 70 dB across all corners
- Total input referred integrated noise less than 100 μV
- Input offset voltage less than 6 mV
- Common Mode Rejection Ration of 60 dB
- Output voltage swing of +/- 200 mV

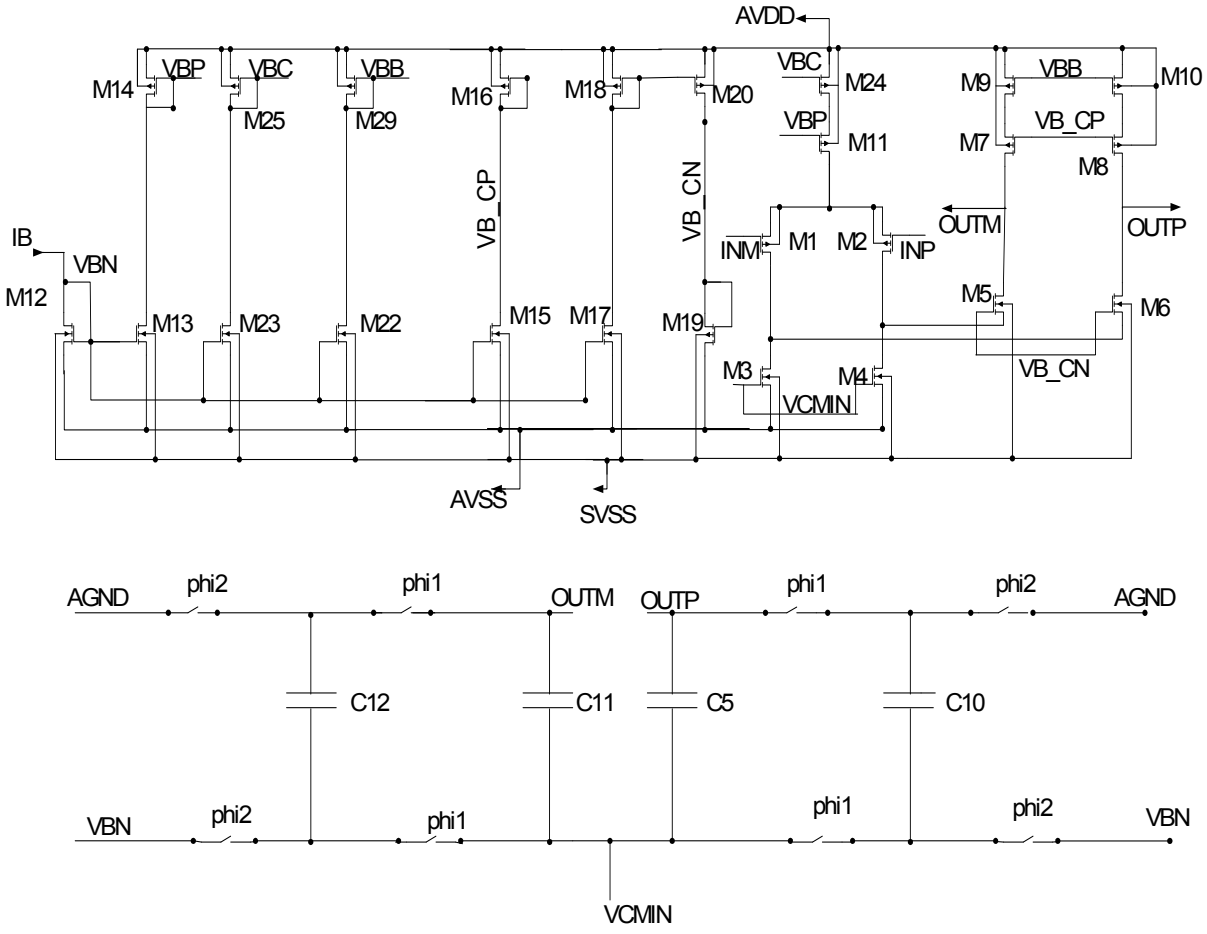

Figure 3.11: OTA schematic

The OTA frequency response using the typical process corner is as shown in Figure 3.12. As seen in figure, the low-frequency open-loop gain is 71 dB. The OTA

has a GBW of 30 MHz with a phase margin of 60 degrees when driving a 5 pF load. Table 3.2 gives the Gain and phase margin for multiple process corners and loads.

Load = 1 pF	Typical	Worst case speed	Worst case power
Phase margin	59.1	58	60
Gain	71.9 dB	71.9 dB	72
Bandwidth	75 MHz	81 MHz	81 MHz
Load = 5 pF			
Phase Margin	58.50	58.2	58.5
Gain	71.9 dB	71.9 dB	71.8 dB
Bandwidth	29.4 MHz	28.2 MHz	31.7 MHz

Table 3.2: Gain and phase margin of OTA for multiple process corners

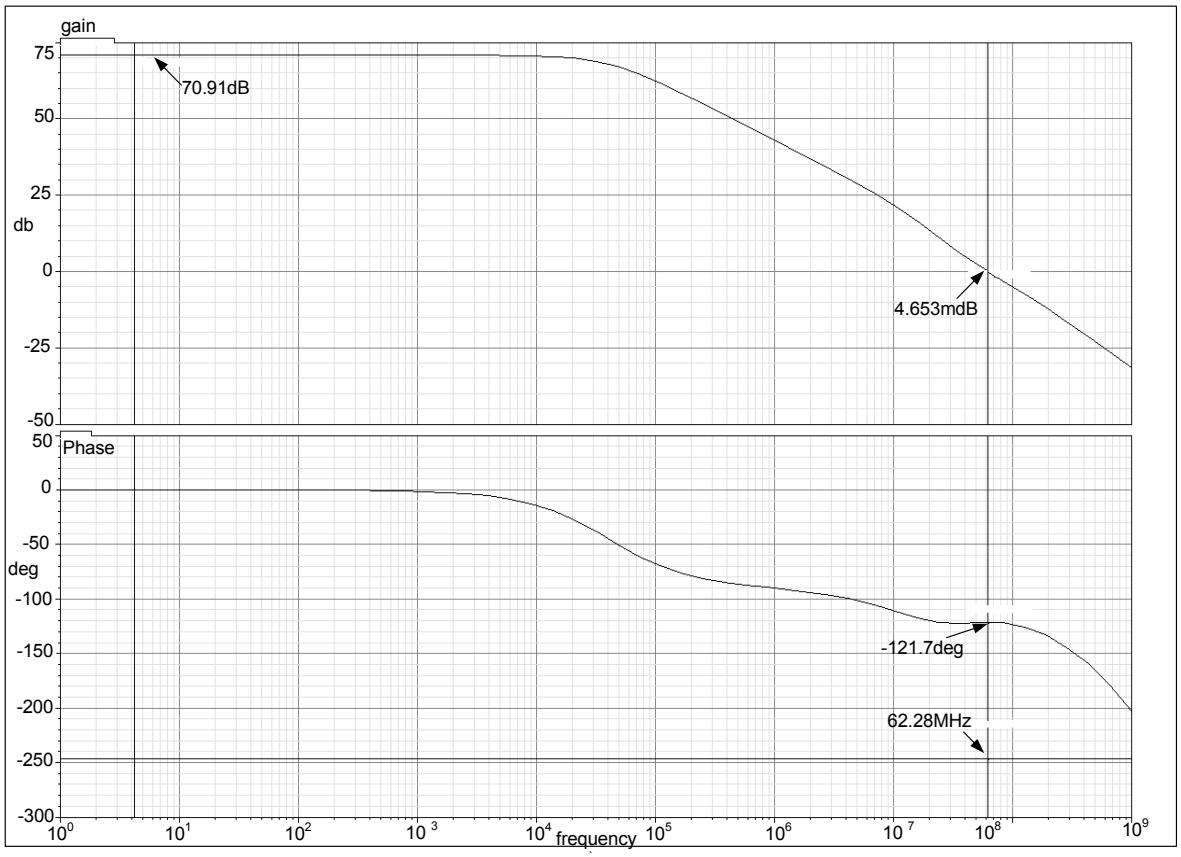

Figure 3.12: OTA frequency response

The OTA meets all the above specifications across all tested (typical, worst-case speed, and worst-case power). The input differential pair in the OTA possesses a large transconductance which is the key feature responsible the fast response time of the residue generator. The sizes of all the transistors used in the OTA schematic are as shown in Table 3.3.

Transistor	Type	Width(μm)	Length(μm)	Multiplier
M1	p	50	0.6	4
M2	p	50	0.6	4
M3	n	4	10	9
M4	n	4	10	9
M5	n	40	2.2	4
M6	n	40	2.2	4
M7	p	63	1.1	4
M8	p	63	1.1	4
M9	p	33.6	9	2
M10	p	33.6	9	2
M11	p	66	0.6	4
M12	n	4	10	2
M13	n	4	10	6
M14	p	6	0.6	1
M15	n	4	10	6
M16	p	24.8	9.2	2
M17	n	4	10	2
M18	p	50.4	10	2
M19	n	14.5	7.5	1
M20	P	50.4	10	6
M22	n	4	10	6
M23	n	4	10	6
M24	p	24	1.5	3
M25	p	24	1.5	3
M29	p	33.6	9	2

Table 3.3: Transistor sizes for OTA schematic

Figure 3.13 shows a pair of inputs to the residue generator and its output. Figure 3.14 shows the settling behavior of the residue generator. It can be seen that the residue generator settles to its final value within 20 nanoseconds.

The residue generator offset voltage does not affect the linearity of the ADC as long as it does not drive the input to the second stage out of range covered by the digital correction. The residue generator is implemented in a fully differential configuration and offset-cancellation is performed so the residual offset is primarily due to charge injection mismatch between the switches and capacitor mismatches.

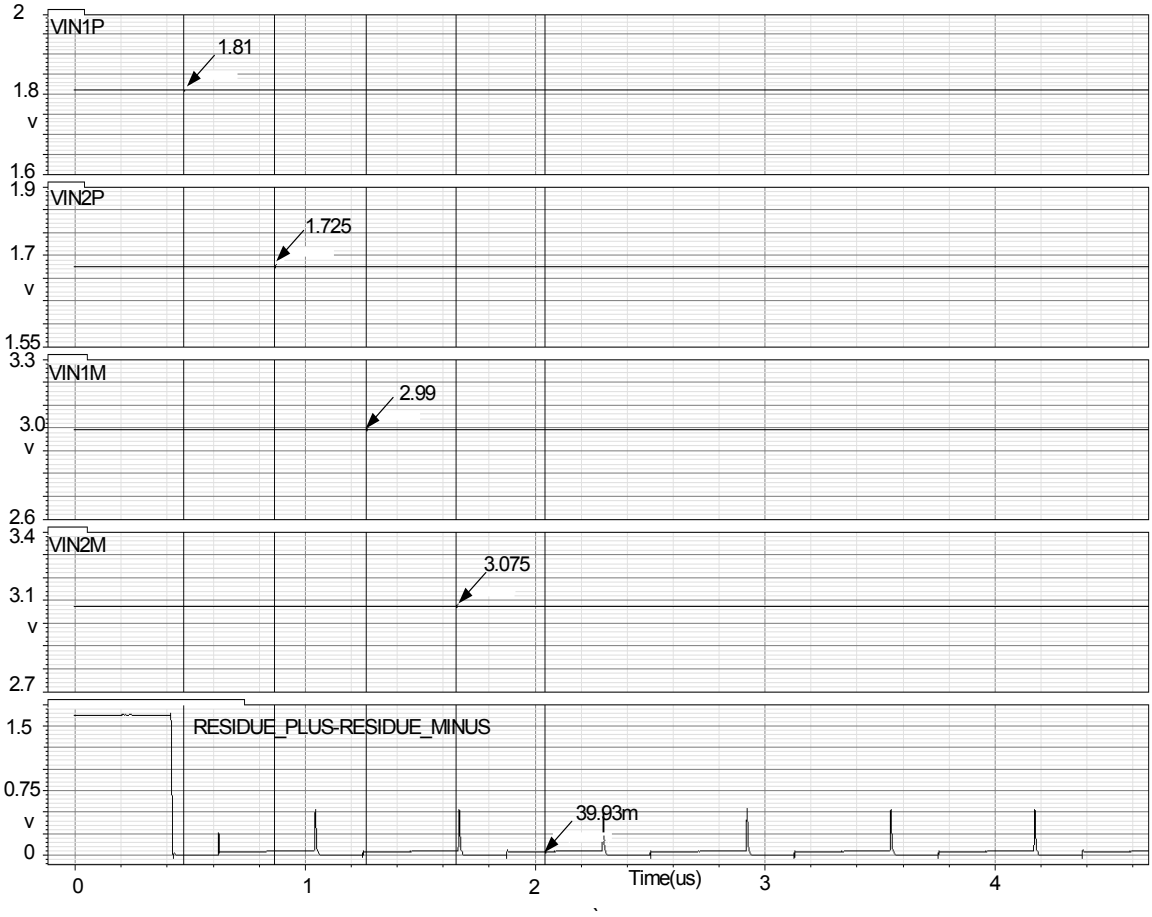

Figure 3.13: Residue generator output

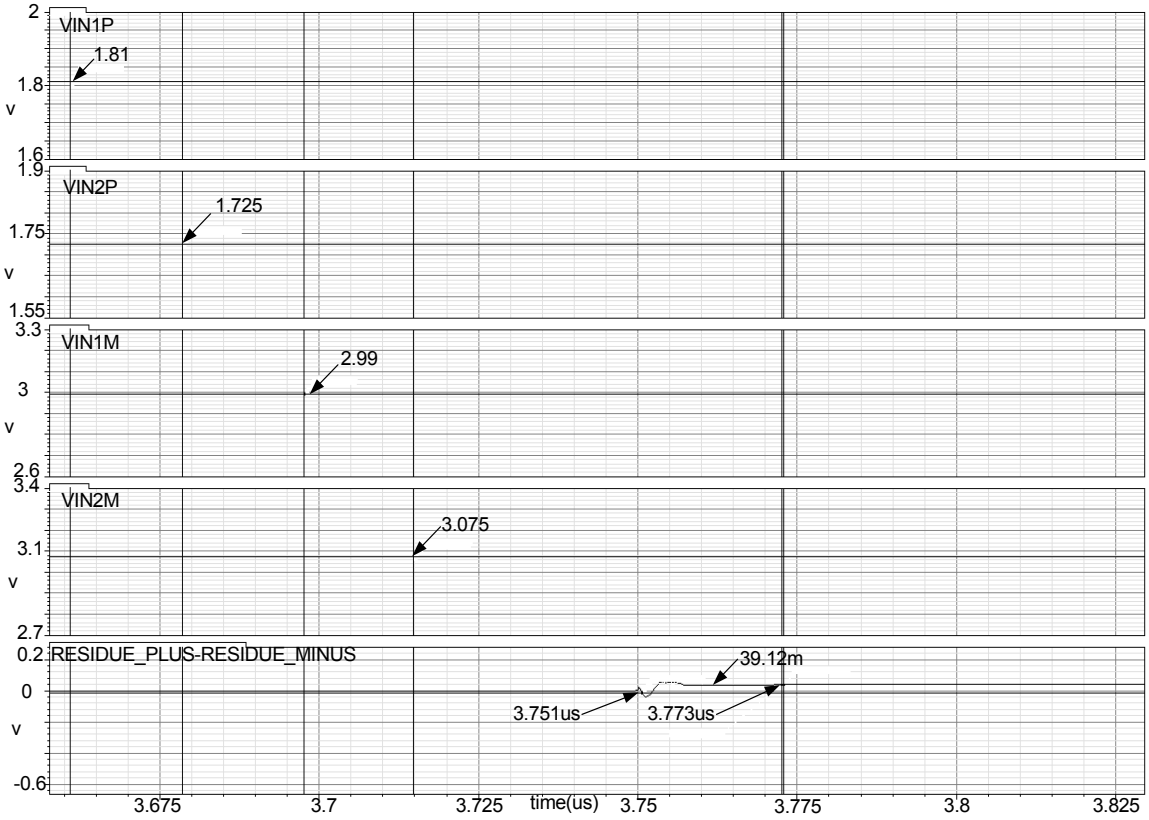

Figure 3.14: Settling behavior of residue generator

Second Stage Ladder and Ladder Correction Circuit

The differential reference voltages in the second stage are generated using the second-stage ladder. The first-stage ladder divides the bandgap voltage (V_{ref_plus}-V_{Ref_minus}) into 64 equal segments. The second-stage ladder divides one of these segments into 64 sub segments each 1 LSB wide. The second stage ladder thus provides differential reference voltages from 1 to 64 LSB. The segment of the first-stage ladder that is divided into 64 sub-segments is at the midpoint of the first-stage ladder so that the common-mode voltage of the differential reference voltage is near AGND (2.4 Volts). As shown in Figure 3.15, each resistor in the second-stage ladder is constructed from "NY" poly.

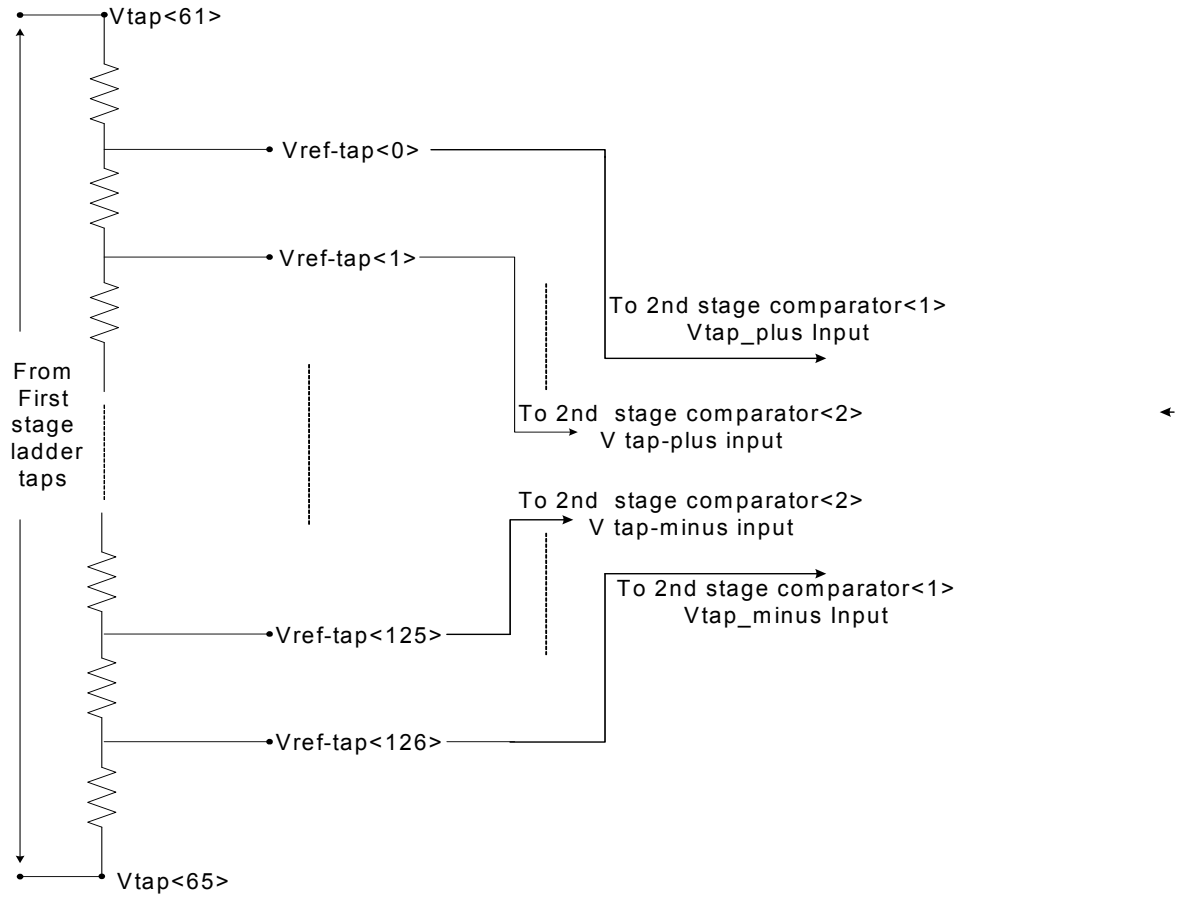

Figure 3.15: Second-stage ladder

As in the first-stage ladder, a resistance of 40Ω is sufficient for matching purposes. Thus a length of 10 μm and a width of 12.5 μm is used for each NY resistor in the ladder. The taps from the first-stage ladder are labeled as Vtap's and second stage taps are labeled as Vref_tap's. Figure 3.15 illustrates how the differential tap voltages are applied to the second-stage comparators.

The loading on the first-stage ladder caused by the addition of the second-stage ladder, leads to a systematic error in the differential voltages generated by the first stage ladder. This results in comparators firing wrongly in the first stage. To avoid this, currents drawn by the second-stage ladder from the first-stage ladder are cancelled using a ladder loading correction circuit [Raz:92]. As shown

in Figure 3.16, the correction circuit injects currents I_1 and I_2 at the junction nodes of the two ladders. The magnitude of the currents equal that of currents drawn by second-stage ladder.

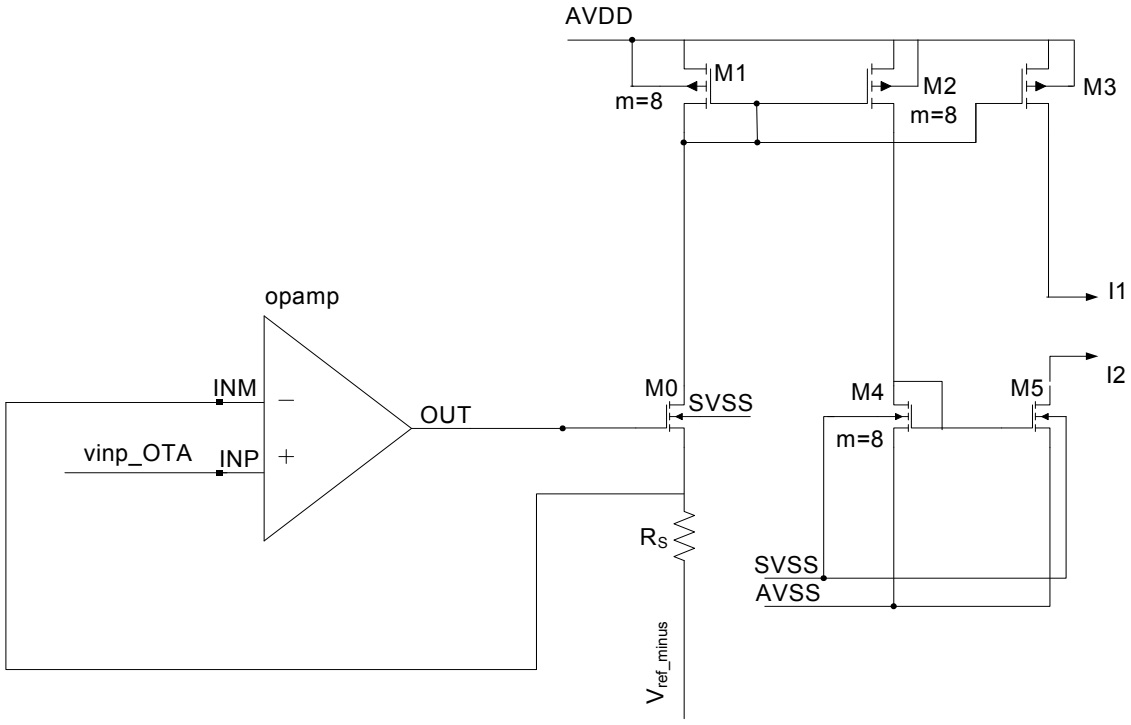

Figure 3.16: Ladder correction circuit

We observe that

$I_1 = I_2$ = (voltage across second stage ladder)/(total resistance of ladder)

Therefore,

$I_1 = I2 = (128LSB)/(128R_u) = 14.64\ \mu A.$

where R_u is the unit resistor in the second stage ladder.

The ladder loading correction circuit consists of a voltage-to-current converter and current mirror circuits. The voltage-to-current converter is made up of the operational amplifier, resistor $R_S(=8R_u)$ and transistor M_0. It produces a current of $(64LSB)/8R_u$. Transistors M_1-M_5 divide this current by a factor of 8 to generate I_1 and I_2. Currents I_1 and I_2 track R_u thus maintaining the loading

correction over variations in temperature and resistor values. An op amp [Pro:07] which was originally designed for the PSD8C chip was used in the circuit of Figure 3.16. Table 3.4 lists the sizes of all the transistors used in the ladder correction circuit.

Transistor	Type	Width	Length	Multiplier
M0	n	31.7	0.6	10
M1	p	12	10	8
M2	p	12	10	8
M3	p	12	10	1
M4	n	10	5	8
M4	n	10	5	1

Table 3.4: Transistor sizes for ladder correction circuit

Second Stage Comparator

The second-stage comparator must compare the differential output of the residue generator with the differential referential voltages from the second-stage ladder. The residue from the residue generator is sampled by the second-stage comparator during $Ø_1$, and comparator offset cancellation also takes place during $Ø_1$. The reference voltages from the second-stage ladder are sampled during $Ø_2$. The second stage comparator is as shown in Figure 3.17 in block diagram form.

Unlike the design by Wooley et. al., we opted not to try to offset-compensate the latch used in the comparator, Rather, we decided to use the first-stage comparator in the second-stage design Since the reference voltages that are sampled from second-stage ladder are in the range of 600 μV, we needed to precede the first-stage comparator with another pre-amplifier, A_1 in Figure 3.17. In fact, Wooley also used this additional pre-amp but with a gain of three. Since we opted

not to offset-compensate the latch, the gain of our pre-amplifier must be much larger *i.e.* in the range of 15 - 20.

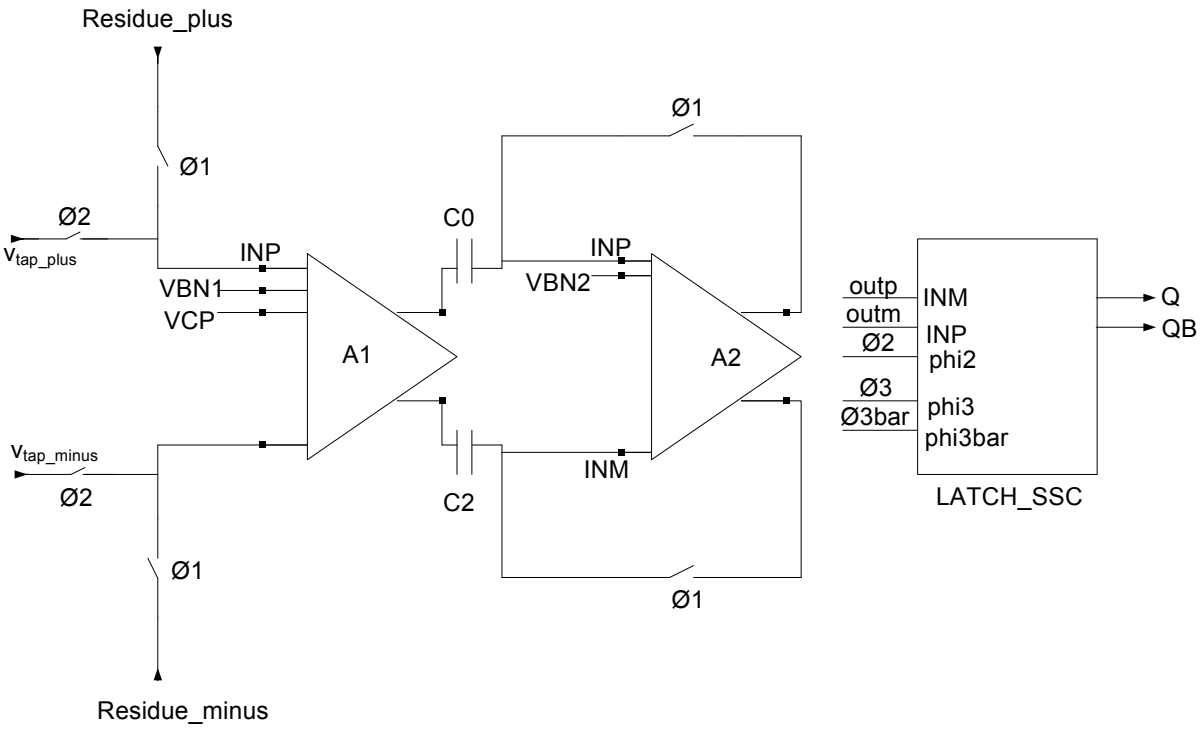

Figure 3.17: Second-stage comparator block diagram

The preamplifier A_1 must never saturate if the offset cancellation scheme is to function correctly. Therefore, it was important that the gain of pre-amplifier A_1 be well-controlled. Too much gain would cause the output to saturate and too little gain would not reduce the input-referred offset to an acceptable level. The schematic for preamplifier A_1 schematic is presented in Figure 3.18. Table 3.5 gives the sizes of the transistors used in the preamplifier A_1. PFETs M_3 and M_4 are operated in the resistive region, and they serve as load devices. The effective resistance presented by these devices is controlled by voltage, V_{CP}. As voltage V_{CP} is decreased, the resistance presented by the PFET loads decreases. Increasing the voltage V_{CP} will increase the equivalent resistance.

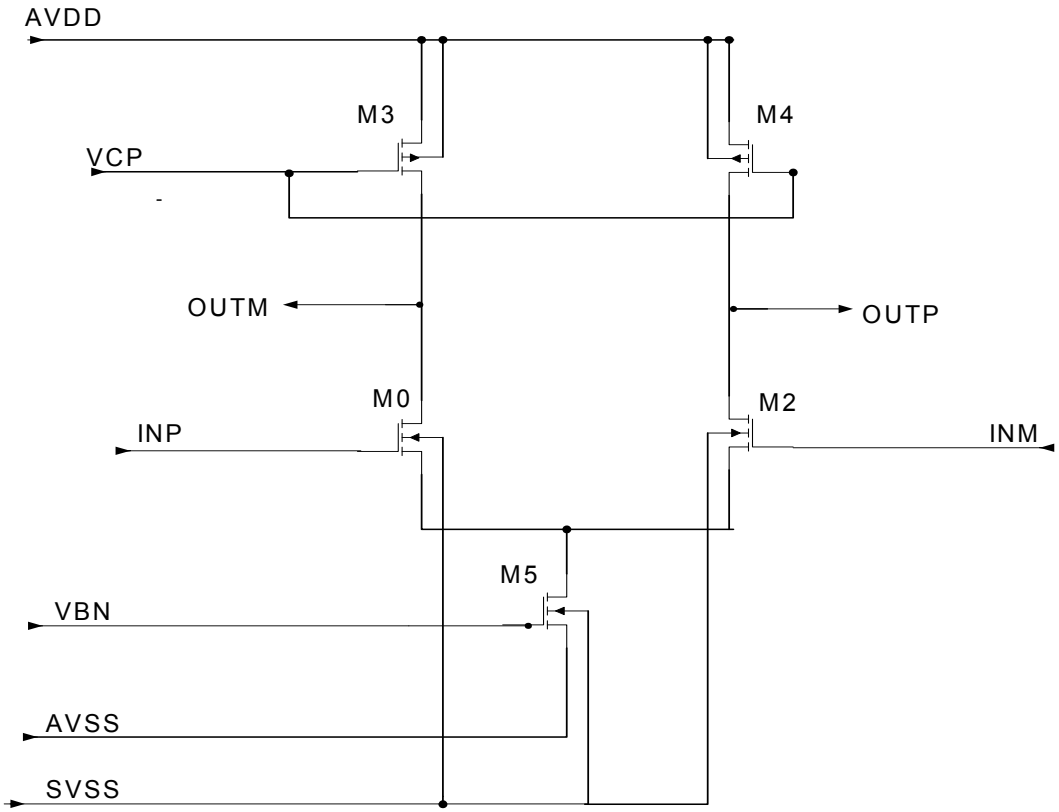

Figure 3.18: Preamplifier A1schematic

Transistor	Type	Width	Length	Multiplier
M0	n	36	0.6	2
M2	n	36	0.6	2
M3	p	5	12	1
M4	p	5	12	1
M5	n	10.2	2	1

Table 3.5: Transistor sizes for preamplifier A1

The gain of the preamplifier A_1 is given as $A_O=g_{m1}*R_{PFET}$ where R_{PFET} is the resistance of device M_3 or M_4. For a moderately or weakly inverted input FET, the input device transconductance, g_{m1}, is proportional to the bias current (which is 50 μA in our design). This implies that the gain of the amplifier in Figure 3.18 is

proportional to the quiescent voltage across the resistive PFET (M_3 or M_4). It is easy to show that when the DC voltage drop across the resistive FET is 1 Volt, the desired gain of about 15 (23.5 dB) will be achieved. Therefore, if the quiescent voltage across the resistive FETs were stabilized, the gain of the preamplifier could be made insensitive to process corner.

A circuit for automatically tuning the gain to the desired value is illustrated in Figure 3.19. One additional pre-amp circuit along with an OTA that is used in the reference generator circuit discussed in an earlier section) must be added. The circuit services all of the second-stage comparator A_1 preamplifiers.

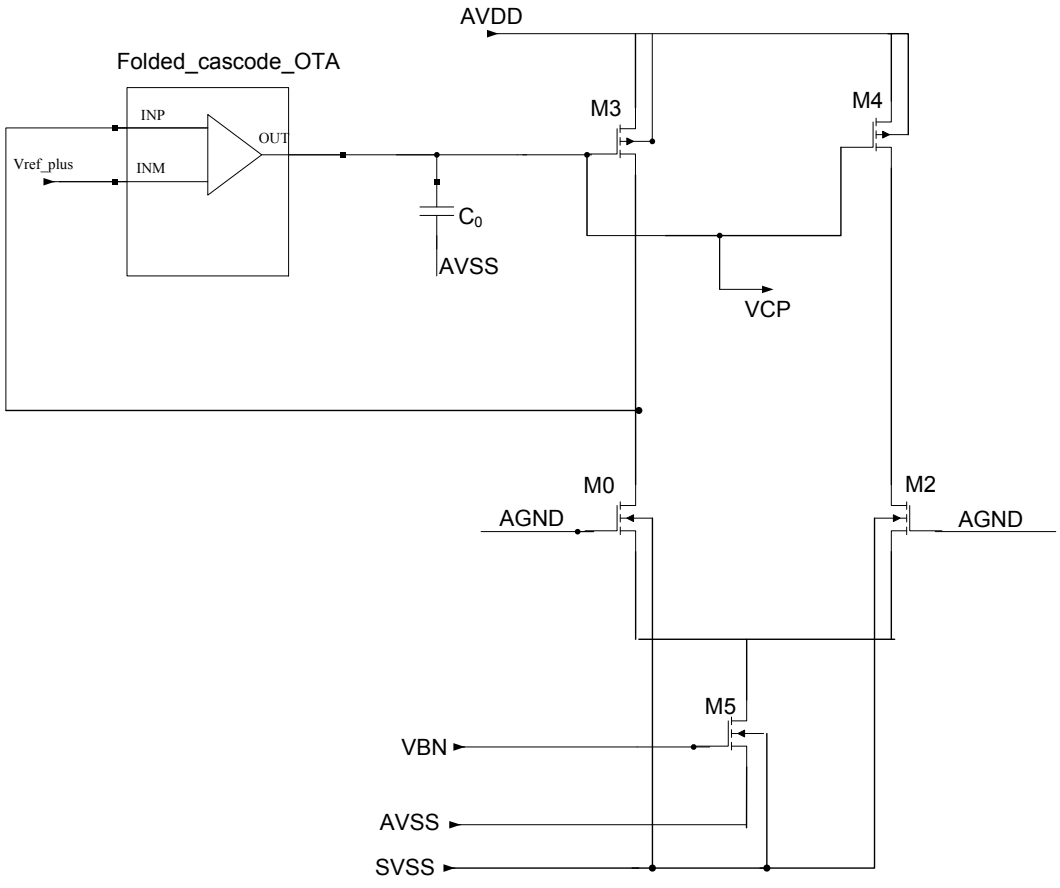

Figure 3.19: Gain control circuit for preamplifier A1

The inputs to preamp circuit of Figure 3.19 are connected to AGND because the residue generator has an output common-mode voltage of AGND. Since we desire the drop across the PFET loads to be 1 Volt, we drive the inverting input of the OTA with 4 Volts. Due to the negative feedback, the OTA will adjust its output voltage, V_{CP}, until the inverting and non-inverting inputs of the OTA are at the same value *i.e.* 4 Volts. In this way regardless of process corner or temperature, the load resistance is adjusted so as to produce the desired gain.

The Bode plot of preamplifier A_1 is presented in Figure 3.20. Note that the values shown in the plot are obtained when the circuit is simulated across typical process corner.

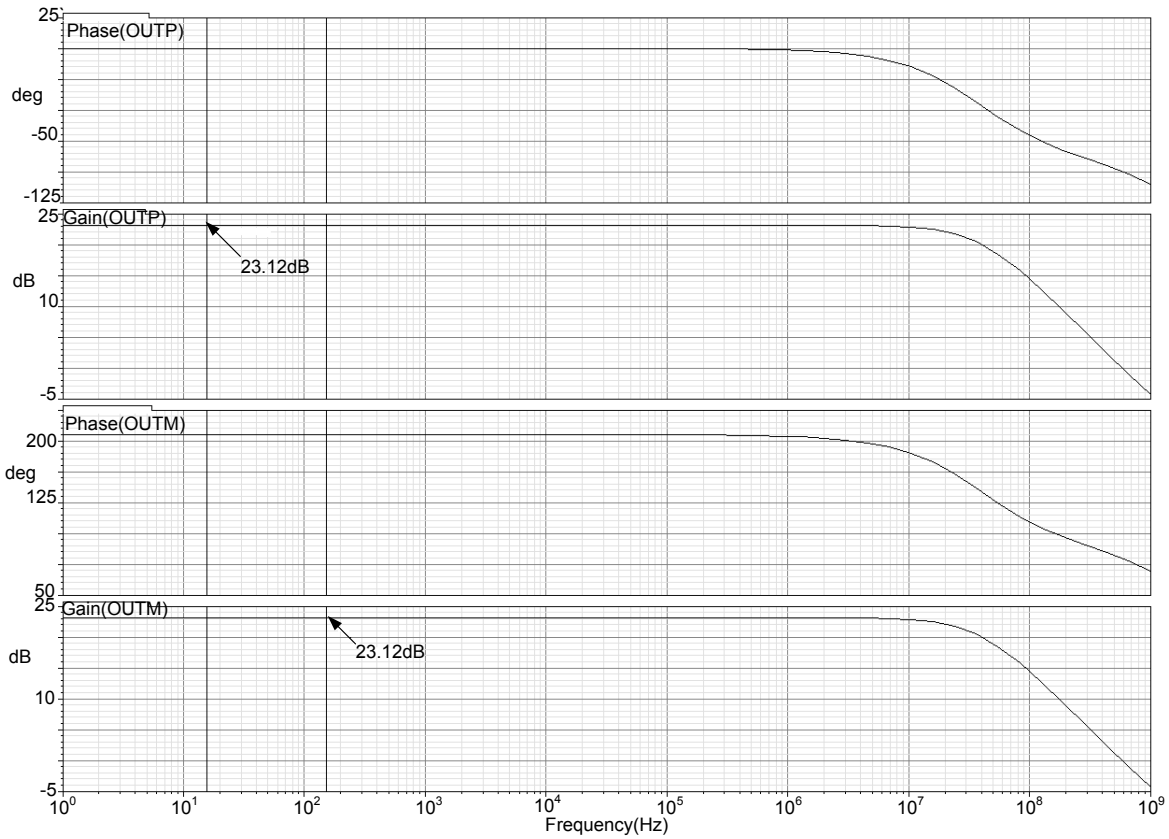

Figure 3.20: Bode plot for preamplifier A1

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Table 3.6 summarizes the gain of preamplifier A_1 as a function of process corner. As expected, we see only 1 or 2 dB of variation in the gain as the process corner is changed.

Corner	Gain(OUTP)	Gain(OUTM)
Typical	23.11dB	23.11dB
Worst case speed	24.94dB	24.94dB
Worst case power	21.28dB	21.28dB

Table 3.6: Gain of preamplifier A1 as function of process corner

Thermometer-to-Binary Encoder

The thermometer-to-binary encoder logic is used to convert the thermometer code output of the comparators into a binary output. This binary output is then sent to the digital correction circuit where the binary outputs of the two stages are combined using the algorithm discussed in Chapter 2 to produce the final 12-bit ADC output. The thermometer-to-binary encoder logic is as shown in Figure 3.21; however, for the electrical simulations described in Chapter 4, a VerilogA model of the logic was used. As shown in Figure 3.21 the thermometer to binary logic consists of a series of AND gates. The figure shows the logic used for converting the first stage comparator outputs. Note that the first of the three inputs to each of the AND gate is negated before being applied to the AND gate.

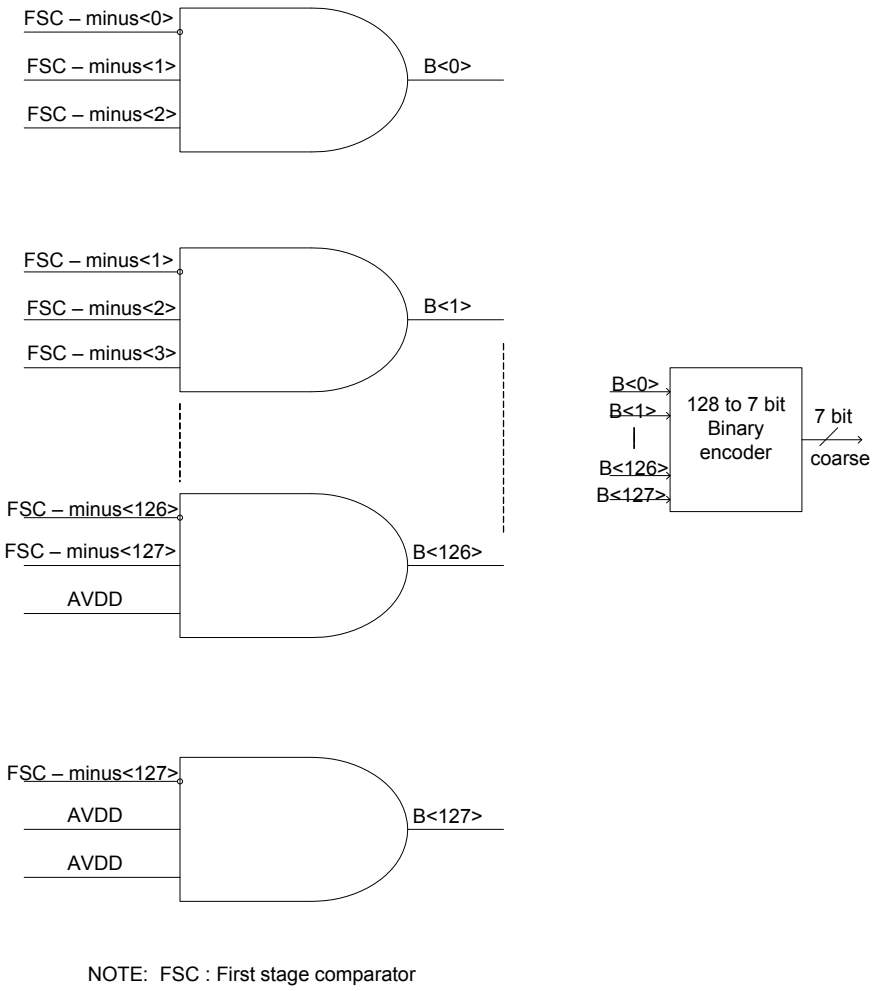

Figure 3.21: Thermometer-to-binary encoder logic

The circuit's function is basically to find the one to zero transition in thermometer code. The outputs of the AND gates are applied to a 128-to-7 bit encoder to obtain the 7-bit "coarse" value. Note that even though the figure represents the logic for converting the first stage comparators, we can still use it to convert the second stage comparator outputs also; the only change in this case would be that instead of using a 128-to-7 bit encoder, we use a 64-to-6 bit encoder.

Digital Correction Logic

The final part of the ADC design is the digital correction [Das:07]. The digital correction is necessary because offset voltages in the first stage comparators can cause the residue to be shifted upward or downward. By allowing an additional bit of resolution in the fine stage, we can compensate for the first stage offset error. This compensation can be done by the following equation:

$Y = A*(2^{N-1}) - 2^{N-2} + B$

Where $A = \{a_{M-1}, a_{M-2}.,. ., a_N, a_{N-1}\}$ =Result from "coarse" stage

$B = \{b_{N-1}, b_{N-2}, \ldots, b_1, b_0\}$ = Result from "fine" stage

Y = Output value of ADC

This equation, however, does not work correctly if the lowest and highest values. For input voltages that are below the lowest tap voltage, the DAC output is not shifted downward. Therefore, we will need to forego subtracting 2N-2 in the above equation for this case. Also, if the value of Y happens to overflow, then one needs to saturate the output and return an overflow flag.

In order to implement the digital correction in an efficient manner, we suggest using a Carry Save Adder (CSA) followed by a carry propagate adder (ripple carry, carry-look-ahead, *etc.*) as shown in Figure 3.22. This allows one to add the three numbers efficiently. Also depicted in the figure is the logic necessary to handle the special case when the "coarse" value is 0 and to detect overflow. Overflow can be detected by looking at the case where the coarse ADC is at its highest value (A = all l's), and the two most significant bits of the fine ADC are 1's.

Design at the circuit-level for the digital correction still needs to be completed. A VerilogA behavioral model of the digital correction algorithm was used in the simulations of the ADC presented in the next chapter.

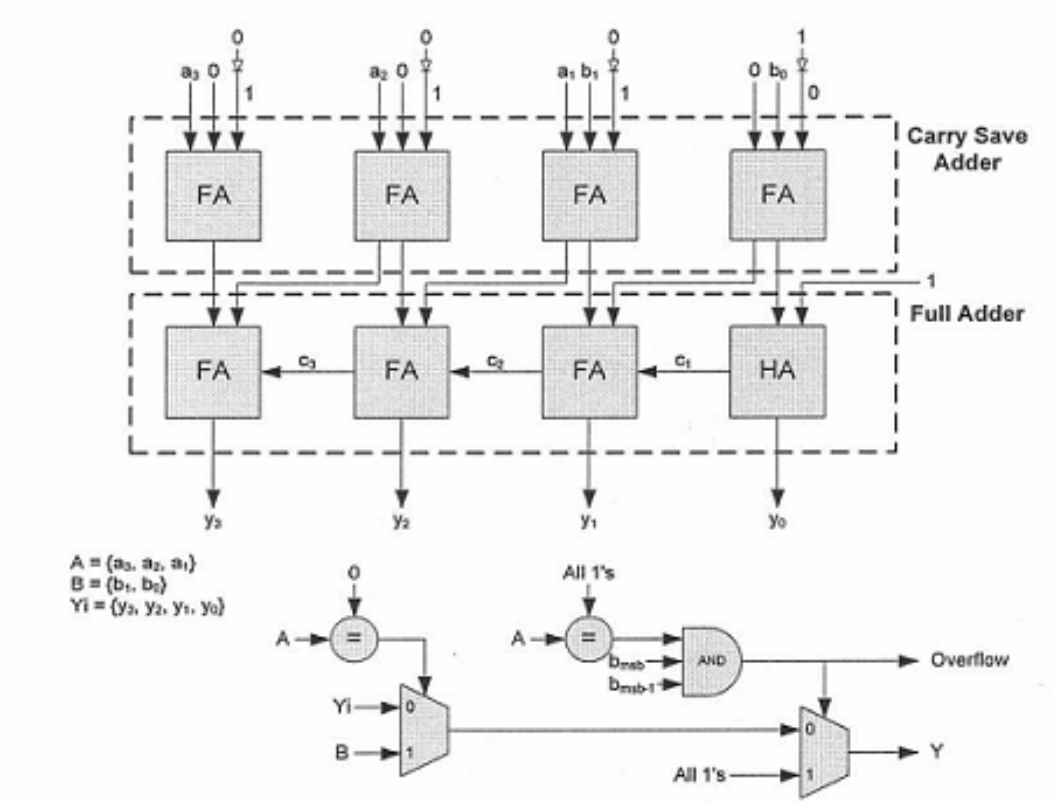

Figure 3.22: Digital correction logic

CHAPTER 4

SIMULATED PERFORMANCE OF ADC

Chapter 4 presents the results of simulations performed on the ADC. The ADC has been verified through a series of behavioral-level and electrical-level simulations. The random offsets and mismatches that would be present in the ADC if it were fabricated are not accounted for in the electrical simulations performed using Cadence's Spectre® program. However, analyses were performed in MathCAD® to estimate the effects of random offsets and element mismatches. The results of these analyses are also presented.

Verification of Two-Step Algorithm

The verification of the two-step flash algorithm presented in Chapter 2 was performed by using a comprehensive simulator developed using MathCAD®. Every effort was made for the MathCAD simulations to emulate the operation of the ADC at the *circuit level*. The simulator code is included in Appendix B. The mismatches associated with the resistor ladders, the DAC capacitor mismatches, first-stage comparator offsets, residue generator gain error, and the second-stage comparator offsets have all been modeled in the MATHCAD® simulator.

Initially, the 12-bit two-step flash ADC was modeled without non-ideal effects. All of the parameters in the MathCAD simulation associated with non-ideal effects were set to "ideal" values which would make the effects negligible. Like MATLAB®, MathCAD is vector and matrix oriented. A vector of 100,000 analog inputs was generated. The input voltages were uniformly distributed between -1.1 Volts and +1.1 Volts (referenced to AGND). Voltages near the references were

avoided since overflow detection is yet to be implemented in the digital correction logic.

The analog inputs were digitized using the two-step flash algorithm (emulating circuit-level operation). The resulting digital output vector was then converted back to vector of analog output voltages using an ideal DAC function. The analog input voltage vector was then subtracted from the analog output voltage vector to form the error vector. The mean and standard deviation of this error vector were computed. It is well-known [All:03] that the standard deviation of the error associated with a linear quantizer is δ/sqrt(12) where δ is the effective step size. In other words, δ = sqrt(12) * standard deviation. The effective number of bits (ENOB) can then be computed using the equation ENOB = log(FS/δ) / log(2) where FS is the full-scale range of the converter (in this design 2.4Volts). With the non-ideal effect negligible, the ENOB was 12.0 bits as expected.

The analog input vector was sorted and then the quantization error was plotted as a function of input level. The error plot is presented in Figure 4.1. Note, the error is not zero mean. This implies that the ADC had a DC gain error of about 5 mV which is not important in our application.

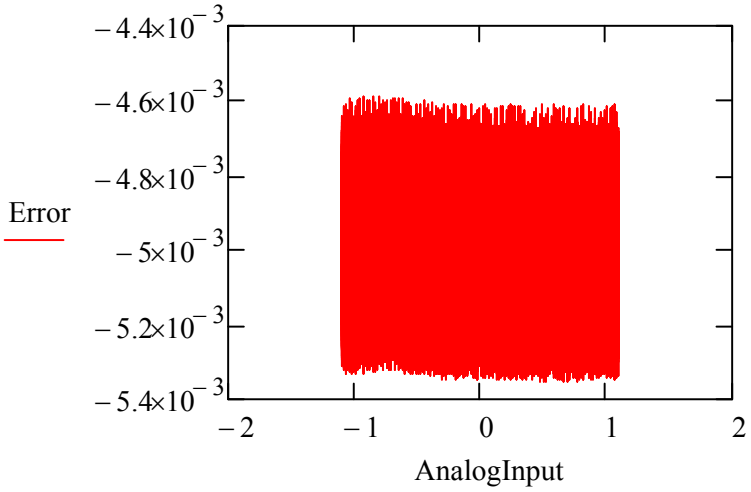

Figure 4.1: Error plot of ideal 12 bit ADC

The influence of non-ideal effects on the performance of ADC

In order to observe the effect of a particular non-ideal effect on the performance of the ADC, we changed the parameter associated with the effect over some reasonable range while keeping the parameters associated with all of the other effects at their ideal values.

Let us consider the effect of resistor mismatch (in the two ladders) on the performance of the ADC. We observe in Figure 4.2 that as the percentage of mismatch between the resistors approaches 4 % the ENOB decreases. It is not difficult to achieve resistor matching of 0.5% or even 0.25%. We conclude that resistor matching is not a significant effect in this design.

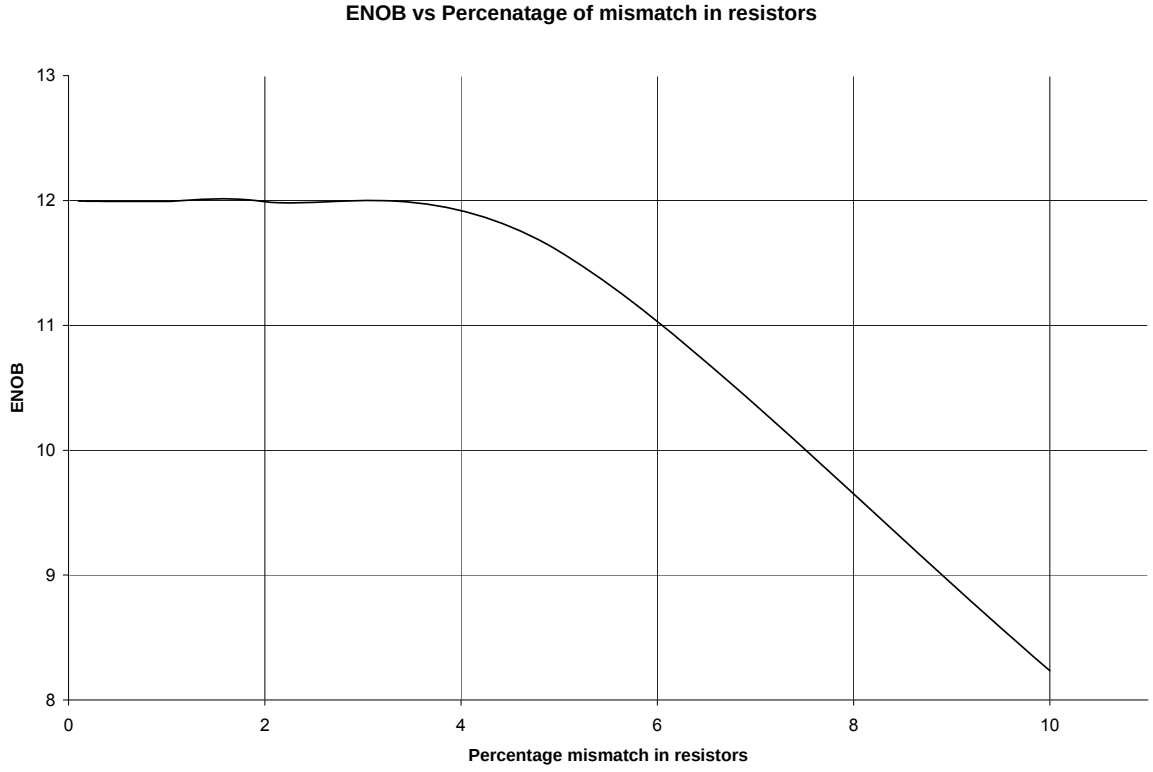

Figure 4.2: ENOB versus percentage of mismatch in resistors.

The ENOB is calculated for variations in the residue generator gain and a plot of ENOB versus the gain variations is as shown in Figure 4.3. We can observe that the effect of gain variation on the ENOB is minimal and the ENOB remains almost constant.

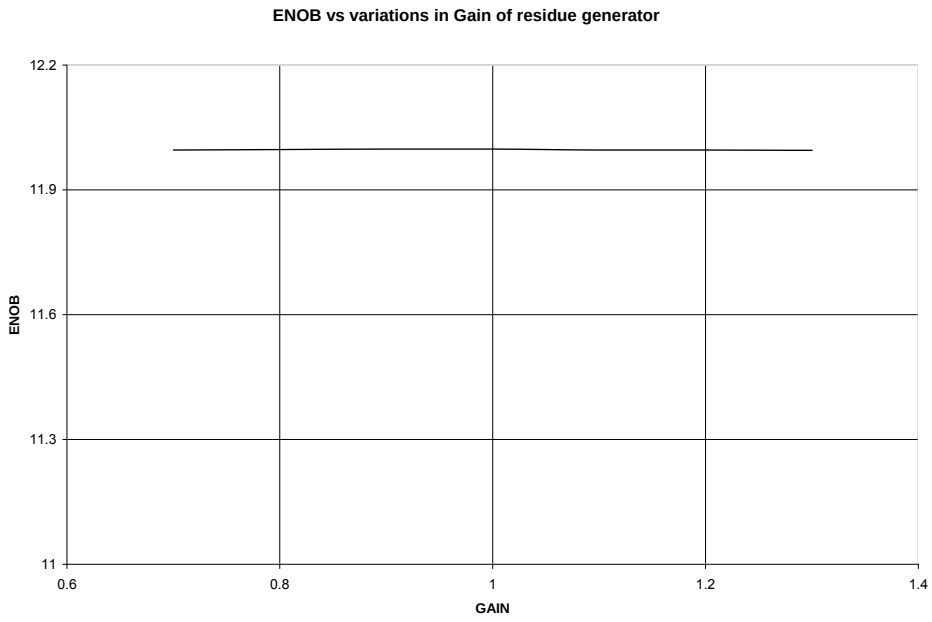

Figure 4.3: ENOB versus variation in Gain of residue generator

We now consider the effect of capacitor mismatch on the performance of the 12-bit ADC. The value for the unit capacitor was modeled as a Gaussian random variable with a mean determined by the nominal value and a standard deviation computed from empirical formulas found in the literature. The standard deviation is inversely proportional the square root of the capacitor value. It should be noted however that the area occupied by the capacitor depends on the value of the capacitor in a linear fashion. Therefore, as the capacitor value is increased we would expect an improvement in the ENOB but this comes as the cost of increased area.

The ENOB is calculated for a range of possible unit capacitor (used in DAC) values. We observe from Figure 4.4 that as the capacitor size is increased, the ENOB increases as predicted. We conclude that using unit capacitors larger than 2 pF has minimal advantages.

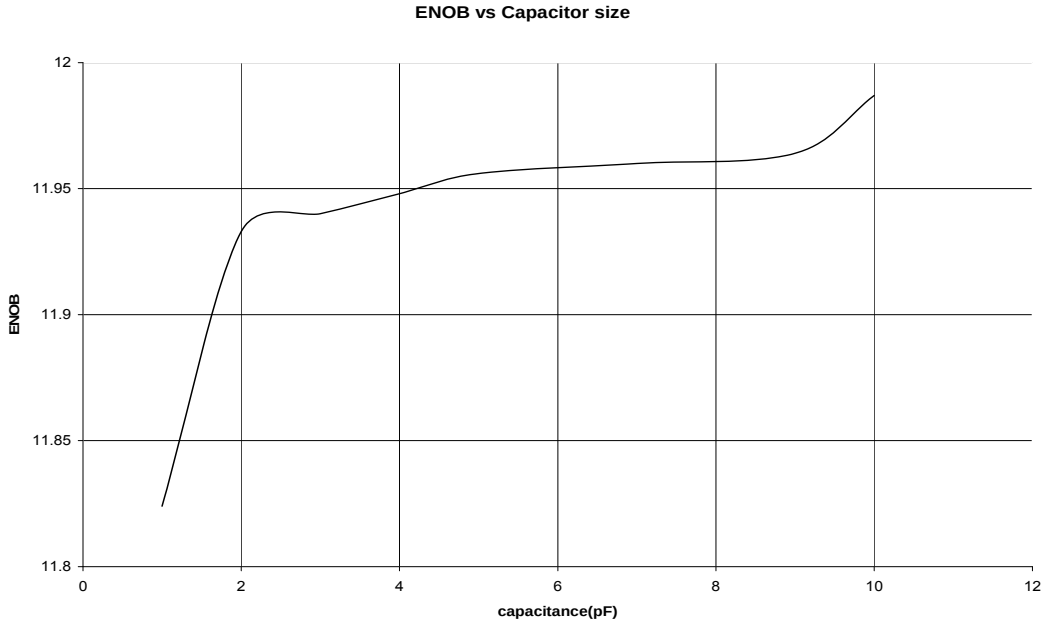

Figure 4.4: ENOB versus mismatch in capacitors

First-stage comparator offsets also affect the performance of the12-bit ADC. Figure 4.5 shows the ENOB as a function of the first-stage comparator offset voltages. The offset voltage was modeled as a Gaussian random variable with a zero mean and with a standard deviation predicted using empirical formulas. As was the case with capacitor matching, the standard deviation of the offset voltage is inversely proportional to the square root of the area occupied by the devices used in the comparator. Note that as long as the offset voltages are within the range of digital correction the EONB remains constant. Recall that for Gaussian distributions we would expect for the offset voltages (99.7% of them) to lie in the

range between -3σ and +3σ. We are plotting s on the x-axis in Figure 4.5. We conclude that the standard deviation associated with the first-stage offsets should be less than 3 mV.

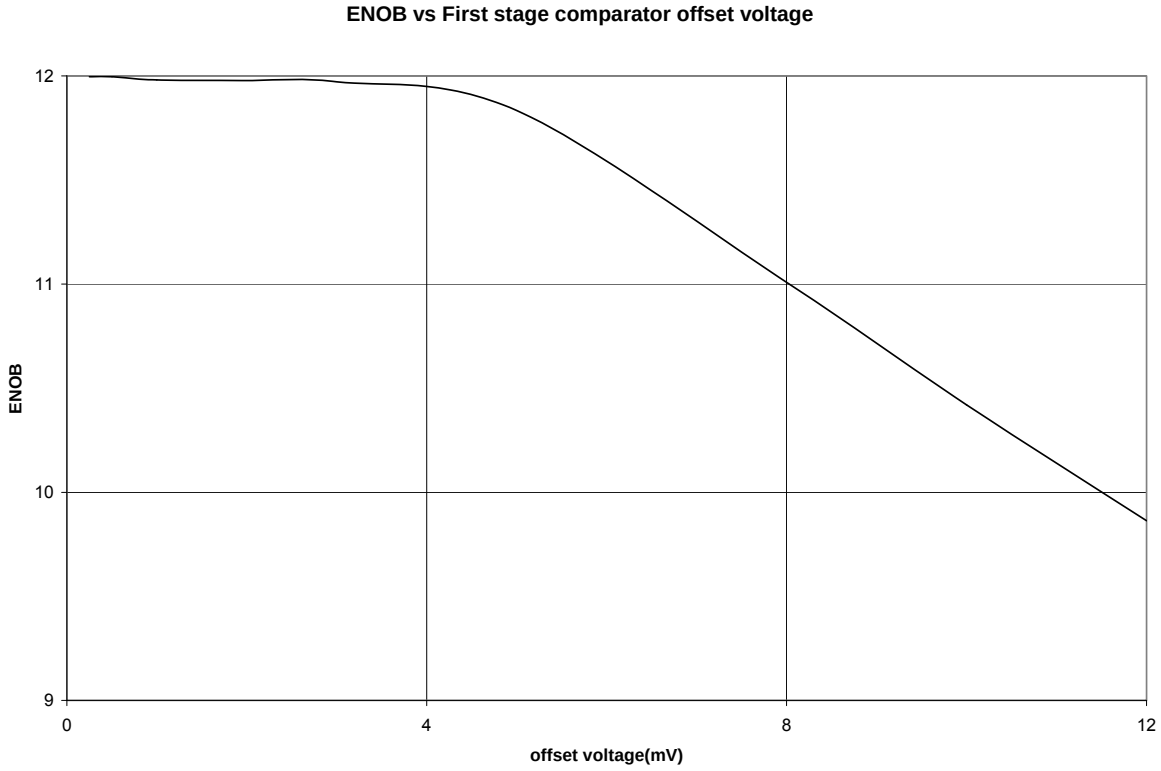

Figure 4.5: ENOB versus first-stage comparator offset voltages

We now consider the effects of second-stage offsets on performance. The second-stage offsets are a function of both the gain of preamplifier A_1 and the magnitude of the first-stage comparator offsets. The second-stage offsets are obtained by dividing the first-stage offsets by the gain of preamplifier A_1. Recall that the second-stage comparator was implemented by taking the first-stage comparator and preceding it with preamplifier A_1. Figure 4.11 shows the ENOB as a function of the gain of preamplifier A_1 for various first-stage offset voltages (FSOS).

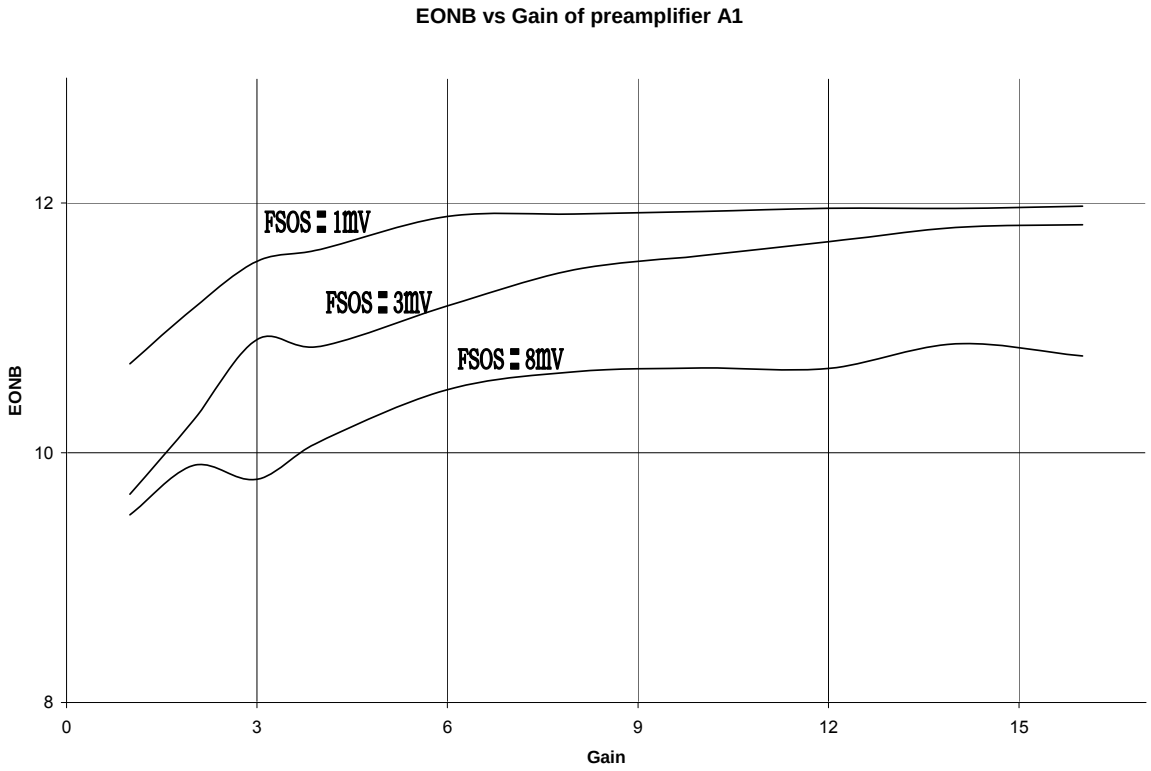

Figure 4.6: ENOB versus gain of preamplifier A1

From Figure 4.6 we observe that for a given first-stage offset [FSOS) the ENOB decreases as the gain of preamplifier decreases. For a low value of FSOS the ENOB reaches 12 bits as the gain is increased but as the FSOS values are increased the ENOB does not reach 12 even though the gain is increased by a large number.

Thus if we keep the FSOS values in the 1 mV - 3 mV range, then the gain of the preamplifier need not be very large (*i.e.* the value of 15 we selected suffices) for obtaining the required ENOB. Figure 4.7 shows the error plot of the ADC when the ADC was simulated with a first stage offset voltage (standard deviation) of 8mV. Note the differences of this plot from Figure 4.1. The 'spikes' in the error plot is a result of a handful of comparators possessing offsets which are larger than what

can be handled by the digital correction algorithm. With a standard deviation of 8 mV, some comparators could easily have offset voltages in the 15-20 mV range.

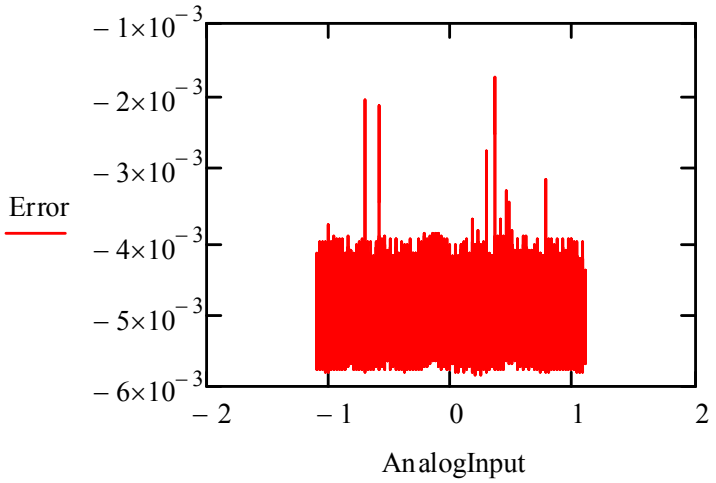

Figure 4.7: Error plot of the ADC with a first stage offset of 8mV

The ADC was tested using Spectre® (electrical-level simulation) with 1000 uniformly distributed random inputs ranging from -1.1 Volts to +1.1 Volts just like what was done in the MathCAD simulations. The error plot for the ADC is presented in Figure 4.8. No random offsets or element mismatches were simulated so one would expect the ENOB to be 12 bits, but the value computed was 11 bits. This value is misleading, however, as we shall now explain.

The error plot in Figure 4.8 clearly contains a systematic error. The systematic error does not raise the quantization noise floor but rather introduces a non-linearity. Observe that the error plot follows the systematic error of the DAC illustrated in Figure 3.9. If the DAC error were reduced, there is every reason to believe that the systematic error we observe in Figure 4.8 would also be reduced. If one were to look at the integral or differential linearity characteristics of the ADC then the systematic error would be significant

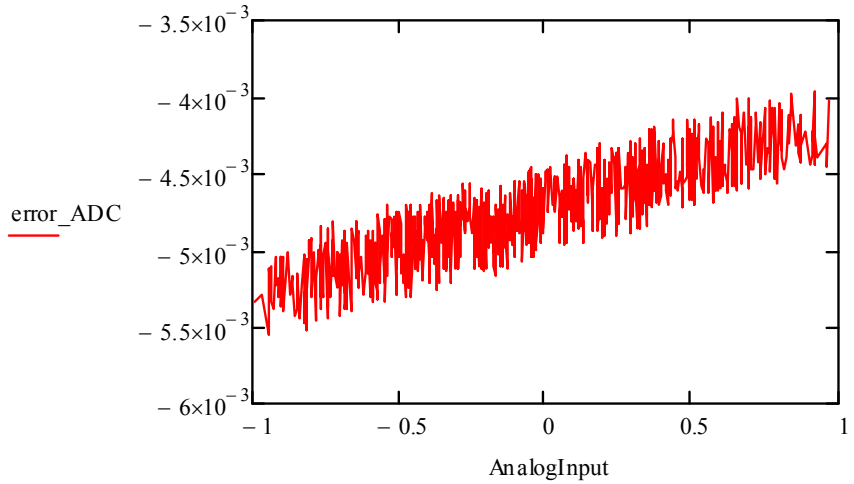

Figure 4.8: Error plot of the ADC simulated using Spectre®

In the proposed applications the linearity performance of the converter is of lesser concern because extensive calibrations are always performed before the experiments are conducted. Non-linearities (provided they are not too large) are easily correctible. Since we are much more concerned with the quantization noise characteristics, we performed a linear regression analysis. The systematic error was then removed from the plot of Figure 4.8 and the plot presented in Figure 4.9 was the result.

The plot is similar to the error plot of the ideal ADC. The ENOB was computed as expected was 12 bits. We conclude that the noise performance of the design presented in this thesis in consistent with that of a 12-bit ADC. When non-ideal effects due to expected matching and offset errors are accounted for the noise performance is at the 11.8 bit level.

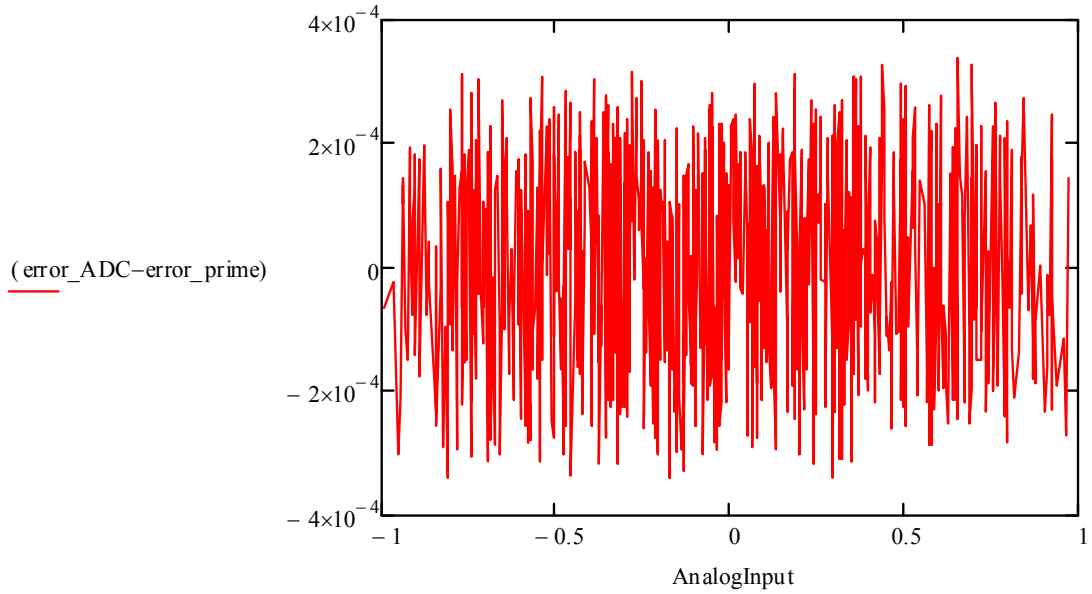

Figure 4.9: Error plot of Figure 4.8 with systematic error removed

Electrical Simulations of ADC Driven by Ramp Input

The ADC was also tested by driving it with a ramp input. The ramp input ranges from -1.1V to 1.1V. A portion of the ADC response is as highlighted in Figure 4.10. The ADC output D<11:0> matches with the output of the MATCAD® simulator. The above figure consists of the most significant (D<6> to D<11>) bits of the ADC when simulated with a ramp input.

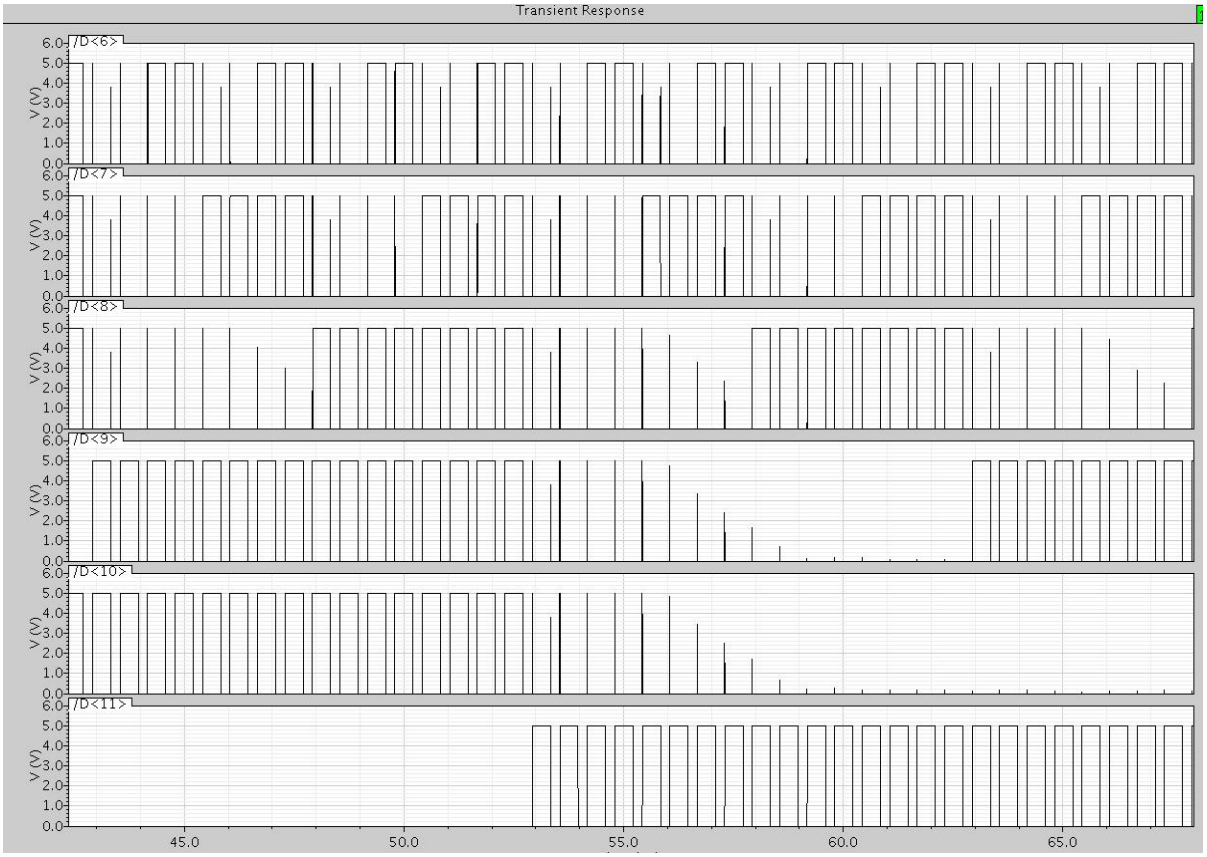

Figure 4.10: ADC response to ramp input

CHAPTER 5

SUMMARY/FUTURE WORK

Summary

This thesis presented the design and simulation of a 12-bit, 2 MSample/sec Analog-to-Digital Converter (ADC). The ADC is intended for use in a family of integrated circuits (ICs) used in the detection of ionizing radiation. The current chip designs provide for analog outputs. Storing data in a digital format on-chip before transmittal to a host computer over an "I2C-like" interface will result in improved system performance since the transmission of digital data is much less susceptible to interference form environmental noise sources.

The ADC design described here will be implemented, sometime in the future, in a 5-Volt AMIS 0.5 μm, double-poly, tri-metal CMOS process (C5N). The converter described employs a two-step flash technique with digital error correction and is configured as a fully-differential circuit. The converter performs a 7-bit "coarse" flash conversion followed by 6-bit "fine" flash conversion, the results of which are then combined through a digital correction algorithm to produce the desired 12-bit output. The "coarse" and "fine" stages are pipelined.

Electrical simulations using Cadence's Spectre® program indicate that in the absence of offsets and mismatch errors the effective number of bits (ENOB) for the converter is 12 bits if only quantization noise performance is considered. Behavioral simulations using MathCAD predict performance of 11.8 or 11.9 bits when expected offset and mismatches are included. Since the DAC used in the "coarse" stage displays a non-linear error characteristic, the over all ADC performance also exhibits some small non-linearities. While the integral and differential linearity characteristics where not explicitly investigated, there is

evidence to suggest that converter's performance is more consistent with that of an 11 bit device. Non-linearities in the converter are of lesser concern in the proposed applications because of the calibrations that much be performed periodically during the course of an experiment. Systematic errors can be easily corrected.

Future Work

The ADC will be sent out for fabrication on a test chip sometime during summer 2009 and will then be integrated into the PSD8C chip in late 2009. Before the IC is submitted to MOSIS (MOS Implementation Services), there are still a number of simulations that need to be performed. While the ADC simulates correctly at the typical process corner, simulations at the "worst-case-power" and the "worst-case-speed" process corners are yet to be performed. Most importantly the source of the systematic error (which we believe is related to the DAC error seen in Figure 3.9) must be confirmed and remedied if possible.

The electrical simulations presented in the thesis were performed with input and reference voltages applied to the ADC from the VerilogA drivers and not from the reference voltage generator and the input voltage drivers discussed in Chapter 3. The operational amplifier used in the single-ended-to-differential converter and reference generator circuits need to be modified so that they settle more quickly. The modified operational amplifier must be integrated with the other components to check for any loading effects.

The ADC is presently being simulated at 1.7 Samples/sec, but no effort was expended to determine its maximum operating frequency. There is evidence that suggests that with some minor modifications that it will be capable of rates approaching 5 MSamples/sec.

After all of the remaining design and associated simulations are completed, the ADC must be physically laid out (no small task), verified against schematic, and design rule verified. The ADC must also be combined with the on-chip RAM and I2C interface briefly discussed in Chapter1. Finally all of these components need to be integrated onto the PSD-8C chip shown in Figure 5.1.

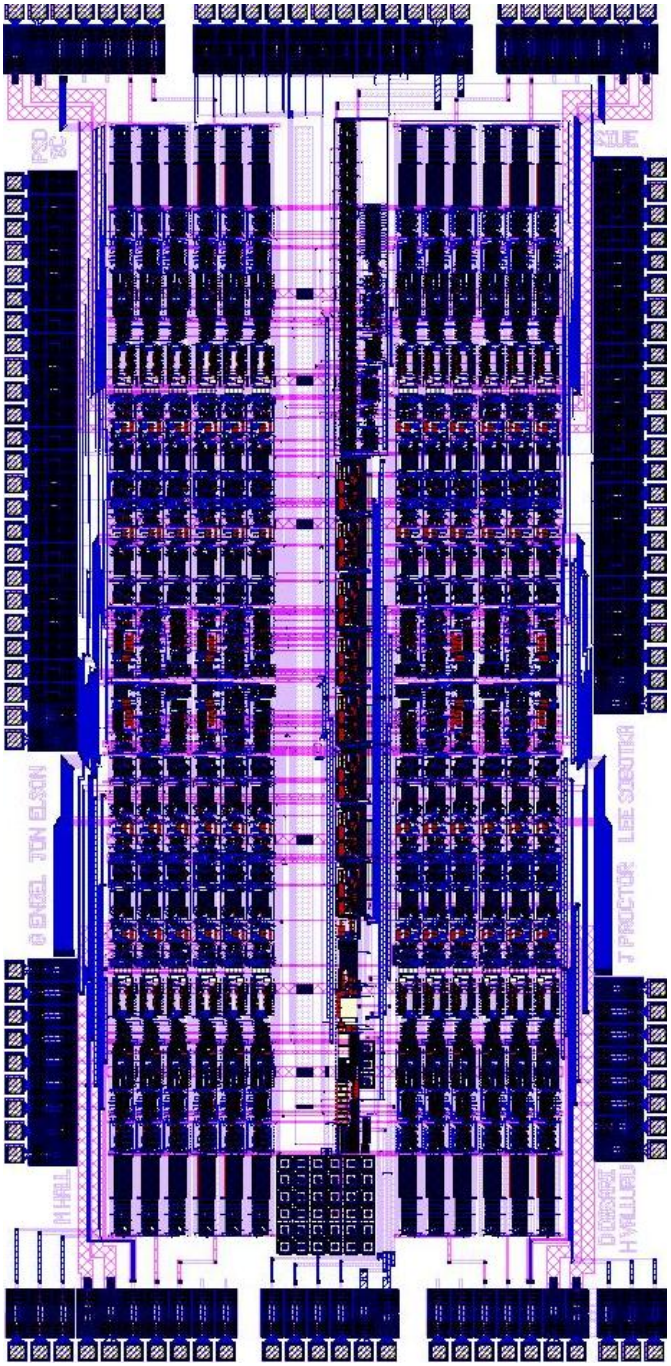

Figure 5.1: PSD chip layout

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APPENDIX A
VerilogA Code

Digital correction logic

```
// VerilogA for ADCdkdLib, decoder_logic_128bit, veriloga

`include "constants.vams"
`include "disciplines.vams"

module decoder_logic_128bit(dout, FSC, SSC);
output [11:0] dout;
electrical [11:0] dout;
input [127:0] FSC;
electrical [127:0] FSC;
input [63:0] SSC;
electrical [63:0] SSC;

//
// Set logic threshold at 0.5 * Vdd or 2.5 Volts
// Set fullscale output to 4095 for 12 bits
//
   parameter real LogicHigh = 5.0 ;
   parameter real LogicLow = 0.0 ;
   parameter real LogicThreshold = 2.5 ;
   parameter real fullscale = 4095.0 ;
//
// Propagation delay and rise/fall times on digital output bus
//
   parameter real tpd = 0 ;
   parameter real trf = 1.0n ;
//
// Read the first stage and second stage comparator buses
// into real-valued arrays for easy manipulation
//
   real  FSCreal  [127:0] ;
   real  SSCreal  [63:0] ;
//
// Digital output word as a real value.
// The real variable "half" is used in computation of the electrical
// output bus
//
   real  half ;
   real  dword ;
   real  coarse ;
   real  fine ;
   real  DigitalOutput ;
//
// Define for loop variable i
//
   integer i ;
//
// Behavioral description of thermomoter to binary conversion
// followed by digital correction logic.  The digital word as a
// real-value is then converted to a bus of electrical nodes.
//
   analog begin
//
// Convert "electrical" buses to real-valued array
//
      generate j (0, 127) FSCreal[j] = V(FSC[j]) ;
      generate j (0, 63) SSCreal[j] = V(SSC[j]) ;
//
// Compute "coarse" value by counting ones in the FSCreal array.
//
      coarse = 0.0 ;
      for (i = 0; i < 127; i = i + 1) begin
         if(FSCreal[i] < LogicThreshold) coarse = coarse ;
         else coarse = coarse + 1 ;
      end
//
// Compute "fine" value by counting ones in the SSCreal array.
```

```
//
     fine = 0.0 ;
     for (i = 0; i < 63; i = i + 1) begin
        if(SSCreal[i] < LogicThreshold) fine = fine ;
        else fine = fine + 1 ;
     end
//
// Compute the digital word
//
      if (coarse == 0) dword = coarse * pow(2,5) + fine ;
      else dword = coarse * pow(2,5) - pow(2,4) + fine ;
//
// Convert "dword" to an electrical bus
//
      half = fullscale / 2.0 ;
      generate j (11, 0) begin
         if (dword > half) DigitalOutput = LogicHigh ;
         else DigitalOutput = LogicLow ;
         V(dout[j]) <+ transition(DigitalOutput, tpd, trf) ;
         if (dword > half) dword = dword - half ;
         dword = 2.0 * dword ;
      end
   end
endmodule
```

ADC data collector

```
// VerilogA for ADCdkdLibTest, ADC_DATA_COLLECTOR_128bit, veriloga

`include "constants.vams"
`include "disciplines.vams"

module ADC_DATA_COLLECTOR_128bit(DAC_OUT_MINUS, DAC_OUT_PLUS, DIGITAL_WORD, FSC,
RESIDUE_MINUS, RESIDUE_PLUS, SSC, VSH);
input DAC_OUT_MINUS;
electrical DAC_OUT_MINUS;
input DAC_OUT_PLUS;
electrical DAC_OUT_PLUS;
input [11:0] DIGITAL_WORD;
electrical [11:0] DIGITAL_WORD;
input [127:0] FSC;
electrical [127:0] FSC;
input RESIDUE_MINUS;
electrical RESIDUE_MINUS;
input RESIDUE_PLUS;
electrical RESIDUE_PLUS;
input [63:0] SSC;
electrical [63:0] SSC;
input VSH;
electrical VSH;

parameter Ts = 625e-9;   // entire 3 phase clock period .
parameter delay_time=12.708e-6;
integer ADC12, DAC_P12,DAC_M12,RES_P12,RES_M12 ;
integer i,j;

analog begin
  @(initial_step)
   begin
   ADC12  = $fopen("/home/nuclear/ADCSIM_128bit/ADC_DATA.txt");
   DAC_P12 = $fopen("/home/nuclear/ADCSIM_128bit/DAC_PLUS_DATA.txt");
   DAC_M12 = $fopen("/home/nuclear/ADCSIM_128bit/DAC_MINUS_DATA.txt");
   RES_P12 = $fopen("/home/nuclear/ADCSIM_128bit/RES_PLUS_DATA.txt");
   RES_M12 = $fopen("/home/nuclear/ADCSIM_128bit/RES_MINUS_DATA.txt");
   end


      @(timer(delay_time,Ts))
       begin
       $fstrobe(ADC12,"VSH = %f",V(VSH));
       end
```

```
      @(timer(delay_time+(0.85*Ts),Ts))
        begin
        $fstrobe(ADC12,"DAC_OUT_PLUS = %f",V(DAC_OUT_PLUS));
        $fstrobe(ADC12,"DAC_OUT_MINUS = %f",V(DAC_OUT_MINUS));
        $fstrobe(DAC_P12,"DAC_OUT_PLUS = %f",V(DAC_OUT_PLUS));    //these are for recording
only DAC voltages//
        $fstrobe(DAC_M12,"DAC_OUT_MINUS = %f",V(DAC_OUT_MINUS));
        end


      @(timer(delay_time+(0.85*Ts),Ts))
         begin
         $fstrobe(ADC12,"RESIDUE_PLUS = %f",V(RESIDUE_PLUS));
         $fstrobe(ADC12,"RESIDUE_MINUS = %f",V(RESIDUE_MINUS));
         $fstrobe(RES_P12,"RES_PLUS = %f",V(RESIDUE_PLUS));    //these are for recording only
RESIDUE voltages//
         $fstrobe(RES_M12,"RES_MINUS = %f",V(RESIDUE_MINUS));
         end



      @(timer(delay_time+(1.35*Ts),Ts))
       begin
       generate i (0,127,1)begin
       $fstrobe(ADC12,"i = %d",i);
       $fstrobe(ADC12,"FSC = %f",V(FSC[i]));
                          end
       $fstrobe(ADC12,"*__________________*");
       end


      @(timer(delay_time+(1.5*Ts),Ts))
      begin
      generate j (0,63,1)begin
      $fstrobe(ADC12,"i = %d",j);
      $fstrobe(ADC12,"SSC = %f",V(SSC[j]));
                        end
      $fstrobe(ADC12,"*__________________*");
      end


      @(timer(delay_time+(1.5*Ts),Ts))
      begin
      generate j (0,11,1)begin
      $fstrobe(ADC12,"i = %d",11-j);
      $fstrobe(ADC12,"DIGITAL_WORD = %f",V(DIGITAL_WORD[11-j]));
                        end


$fstrobe(ADC12,"**********************************************************************
****");

      end

      end
endmodule
```

Three phase clock generator

```
// VerilogA for ADCdkdLib, FSC_three_phase_clock, veriloga

`include "constants.vams"
`include "disciplines.vams"

module FSC_three_phase_clock(Phi1, Phi1bar, Phi2, Phi2bar, Phi3, Phi3bar);
output Phi1;
electrical Phi1;
output Phi1bar;
electrical Phi1bar;
output Phi2;
electrical Phi2;
```

```
output Phi2bar;
electrical Phi2bar;
output Phi3;
electrical Phi3;
output Phi3bar;
electrical Phi3bar;


parameter real Fs = 1.6M from (0:inf);              // Clock frequency
parameter real tr = 100p from (0:inf);              // Rise time of clock
parameter real tf = 100p from (0:inf);              // Fall time of clock

parameter real VDD = 5;
parameter real VSS = 0;

parameter real Ts = 1/Fs;
parameter real td12 = 10e-9;

integer Phi1_val;
integer Phi2_val;
integer Phi3_val;

analog begin

@(initial_step) begin
               Phi1_val = 1;
               Phi2_val = 0;
               Phi3_val = 0;

               end

               // Create phi 1 & 2 logic signals using timers
               @(timer(0,Ts))
                      Phi1_val = 1;
               @(timer((Ts/3)-0.1*td12,Ts))
                      Phi1_val = 0;

               @(timer(0,Ts))
                      Phi2_val = 0;
               @(timer((Ts/3),Ts))
                      Phi2_val = 1;
               @(timer((2*Ts/3)-0.1*(td12),Ts))
                      Phi2_val = 0;
               @(timer(0,Ts))
                      Phi3_val=0;
               @(timer(2*Ts/3,Ts))
                      Phi3_val=1;
               @(timer((Ts)-(0.1*td12),Ts))
                      Phi3_val=0;

               // Convert those logic signals to voltages and apply a smooth transition.
               V(Phi1) <+ transition((Phi1_val ? VDD : VSS), 0, tr, tf);
               V(Phi2) <+ transition((Phi2_val ? VDD : VSS), 0, tr, tf);
               V(Phi1bar) <+ transition ((Phi1_val ? VSS : VDD), 0, tr, tf);
               V(Phi2bar) <+ transition ((Phi2_val ? VSS : VDD), 0, tr, tf);
               V(Phi3) <+ transition ((Phi3_val ? VDD : VSS), 0, tr, tf);
               V(Phi3bar) <+ transition ((Phi3_val ? VSS : VDD), 0, tr, tf);

       end


endmodule
```

APPENDIX B

MathCAD® Code

This appendix contains the MatLAB code for the simulator discussed in Chapter 4 of the thesis.

ADC simulator model parameters

Number of bits will be N.

$N := 12$

Reference voltage

$V_R := 1.2V$

Analog signal ground.

$V_{AGND} := 2 \cdot V_R = 2.4\,V$

Standard deviation of first stage offsets.

$FSosVal := 1mV$

$R_{nom} := 40$

$\varepsilon_{res} := 0.0025$

Predict capacitor matching characteristics.

$k_c := 1.28\mu m$

$C_{pp} := 0.0009 \frac{pF}{\mu m^2}$

$n := 1$

$\varepsilon_C(C) := \frac{4k_c \cdot C_{pp}^{\frac{1}{2}} \cdot n^{\frac{1}{6}}}{\sqrt{C}}$

$C_u := 2$

Relative error in unit DAC capacitor.

$\varepsilon_{cap} := 0.01\,\varepsilon_C\left(C_u \cdot 1pF\right) = 1.086 \times 10^{-3}$

Standard deviation of second stage offsets.

$A1 := 14$

Gain of subtractor.

$SubtractorGain := 1$

Compute digital output of N-bit ADC.

$ADC\left(v_{in}\right) := round\left[\left(\frac{v_{in}}{V_R}\right) \cdot 2^{N-1} + 2^{N-1}\right]$

$\Delta := \frac{2 \cdot V_R}{2^N} = 5.859 \times 10^{-4}\,V$

M is the number of bits in the second stage (aka the fine step).

$M := \frac{N}{2}$

The first or coarse stage has M+1 bits.

Size of step in first stage ladder is

$$\Delta_1 := \frac{2 \cdot V_R}{2^{M+1}} = 0.019\,V$$

$$i := 0, 1 .. 2^{(M+1)}$$

Generate resistors in first-stage resistive ladder.

$$FSresistors := rnorm\left(2^{M+1}, R_{nom}, \varepsilon_{res} \cdot R_{nom}\right)$$

$$RFS\_TOTAL := \sum FSresistors = 5.12 \times 10^3$$

$$FSLrange := 2 \cdot V_R = 2.4\,V$$

$$FSL_i := \left| \begin{array}{l} out \leftarrow V_R \quad \text{if } i = 0 \\ out \leftarrow FSL_{i-1} + \dfrac{FSLrange \cdot FSresistors_i}{RFS\_TOTAL} \quad \text{if } \left(i \neq 0 \wedge i \neq 2^{M+1}\right) \\ out \leftarrow 3 \cdot V_R \quad \text{if } i = 2^{M+1} \\ \text{return } out \end{array} \right.$$

Compute tap voltages using resistor ladder.

$$FSL\_PLUS := FSL$$

$$FSL\_MINUS := 4 \cdot V_R - FSL$$

Compute the DAC voltages using charge conservation equations.

$$i := 0, 1 .. 2^{(M+1)}$$

$$CapArray := rnorm\left(2^{M+1}, C_u, \varepsilon_{cap} \cdot C_u\right)$$

$$CapArray_0 := \frac{1}{2} \cdot CapArray_0 = 1$$

$$C_{TOTAL} := \sum CapArray = 254.978$$

$$k := 0, 1 .. 2^{M+1} - 1$$

$$SUMK_k := \left| \begin{array}{l} out \leftarrow 0 \\ \text{for } i \in 0 .. k - 1 \\ \quad \left| \begin{array}{l} \text{continue} \quad \text{if } k = 0 \\ out \leftarrow out + CapArray_i \end{array} \right. \\ \text{return } out \end{array} \right.$$

$$DAC\_PLUS_k := \frac{2 \cdot V_R \cdot SUMK_k + V_R \cdot C_{TOTAL} + V_{AGND} \cdot \left(\frac{C_u}{2}\right)}{C_{TOTAL} + \left(\frac{C_u}{2}\right)}$$

$$DAC\_MINUS_k := \frac{-2\cdot V_R\cdot SUMK_k + 3\cdot V_R\cdot C_{TOTAL} + V_{AGND}\cdot\left(\frac{C_u}{2}\right)}{C_{TOTAL} + \left(\frac{C_u}{2}\right)}$$

Size of step in second stage ladder

$$\Delta_2 := \frac{\Delta_1}{2^{M-1}} = 5.859\times 10^{-4}\,V$$

$$k := 0, 1 .. 2^M$$

$$SSresistors := rnorm\left(2^{M+1}, R_{nom}, \varepsilon_{res}\cdot R_{nom}\right)$$

$$RSS\_TOTAL := \sum SSresistors = 5.119\times 10^3$$

$$CenterTapIndex := \frac{2^{M+1}}{2} = 64$$

$$SSVPindex := CenterTapIndex + 2 = 66$$

$$SSVMindex := CenterTapIndex - 2 = 62$$

$$SSLrange := FSL_{SSVPindex} - FSL_{SSVMindex} = 0.075\,V$$

$SSL_i :=$

- out ← $FSL_{SSVMindex}$ if $i = 0$
- out ← $SSL_{i-1} + \frac{SSLrange\cdot SSresistors_i}{RSS\_TOTAL}$ if $\left(i \neq 0 \wedge i \neq 2^{M+1}\right)$
- out ← $FSL_{SSVPindex}$ if $i = 2^{M+1}$
- return out

Compute tap voltages using resistor ladder.

$$j := 1, 2 .. 2^M$$

$$SSL\_MINUS_j := SSL_{CenterTapIndex - j}$$

$$SSL\_PLUS_j := SSL_{CenterTapIndex + j}$$

Compute random first and second stage random offsets.

$$FSVectorLength := 2^{M+1} + 1$$

$$FSos := 1V\,rnorm\left(FSVectorLength, 0, \frac{FSosVal}{1V}\right)$$

$$temp := Stdev(FSos) = 1.082\times 10^{-3}\,V$$

$$SSVectorLength := 2^M + 1$$

$$SSos := 1V\,rnorm\left(SSVectorLength, 0, \frac{SSosVal}{1V}\right)$$

$$temp := Stdev(SSos) = 6.642 \times 10^{-5}\,V$$

Create a function that can compute the digital word using our two-step algorithm.

$$TwoStepADC(v_{in}) :=$$
$$VIN\_PLUS \leftarrow V_{AGND} + v_{in}$$
$$VIN\_MINUS \leftarrow V_{AGND} - v_{in}$$
$$VIN\_DIFF \leftarrow VIN\_PLUS - VIN\_MINUS$$
$$Coarse \leftarrow 0$$
$$\text{for } i \in 1, 2 .. 2^{M+1}$$
$$\quad diff \leftarrow VIN\_DIFF - (FSL\_PLUS_i - FSL\_MINUS_i)$$
$$\quad diff \leftarrow diff + FSos_i$$
$$\quad Coarse \leftarrow Coarse + 1 \text{ if } diff \geq 0$$
$$DAC\_DIFF \leftarrow DAC\_PLUS_{Coarse} - DAC\_MINUS_{Coarse}$$
$$RES\_DIFF \leftarrow VIN\_DIFF - DAC\_DIFF$$
$$Fine \leftarrow 0$$
$$\text{for } j \in 1, 2 .. 2^{M}$$
$$\quad diff \leftarrow RES\_DIFF - (SSL\_PLUS_j - SSL\_MINUS_j)$$
$$\quad diff \leftarrow SubtractorGain \cdot diff$$
$$\quad diff \leftarrow diff + SSos_j$$
$$\quad Fine \leftarrow Fine + 1 \text{ if } diff \geq 0$$
$$out \leftarrow Coarse \cdot 2^{(M-1)} + Fine \text{ if } Coarse = 0$$
$$out \leftarrow Coarse \cdot 2^{(M-1)} - 2^{M-2} + Fine \text{ if } Coarse > 0$$
$$\text{return } out$$

We need to define a N-bit DAC so we reconstruct the digital sample.

$$DAC(word) := \frac{2 \cdot V_R \cdot word}{2^N} - V_R$$

Generate NUM voltage samples uniformly distributed

$$NUM := 100000$$

$$j := 0, 1 .. NUM - 1$$

$$AnalogInput := runif\left(NUM, \frac{-V_R + 100mV}{1V}, \frac{V_R - 100mV}{1V}\right) \cdot 1V$$

$$AnalogInput := sort(AnalogInput)$$

The vector analog inputs are then quantized.

$$DigitalEquivalent_j :=$$
$$DigitalValue \leftarrow TwoStepADC(AnalogInput_j)$$
$$\text{return } DigitalValue$$

Use an ideal DAC to convert the digital values back to an analog voltage.

$$\text{AnalogOutput}_j := \left| \begin{array}{l} \text{AnalogValue} \leftarrow \text{DAC}\left(\text{DigitalEquivalent}_j\right) \\ \text{return AnalogValue} \end{array} \right.$$

Compute the error voltage.

$$\text{Error}_j := \left| \begin{array}{l} \varepsilon \leftarrow \text{AnalogOutput}_j - \text{AnalogInput}_j \\ \text{return } \varepsilon \end{array} \right.$$

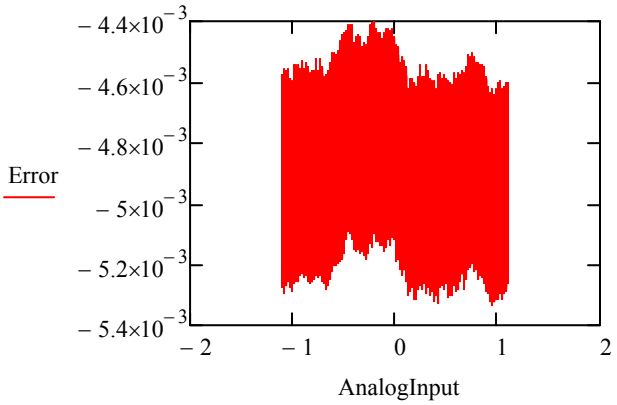
$$\text{AverageError} := \text{mean}(\text{Error}) = -4.889 \times 10^{-3}\ \text{V}$$

$$\text{StandardDeviation} := \text{Stdev}(\text{Error}) = 1.835 \times 10^{-4}\ \text{V}$$

$$\text{Expected} := \frac{\Delta}{\sqrt{12}} = 1.691 \times 10^{-4}\ \text{V}$$

Compute the effective number of bits.

$$\delta := \sqrt{12} \cdot \text{StandardDeviation} = 6.357 \times 10^{-4}\ \text{V}$$



$$\text{ENOB} := \frac{\log\left(\frac{2 \cdot V_R}{\delta}\right)}{\log(2)} = 11.883$$